FAIRCHILD

SEMICONDUCTOR ™

74LCXH16244
Low Voltage 16-Bit Buffer/Line Driver with Bushold

General Description

The LCXH16244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The LCXH16244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The LCXH16244 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCXH16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant control inputs and outputs

■ 2.3V–3.6V V_{CC} specifications provided

■ 4.5 ns t_{PD} max (V_{CC} = 3.0V), 20 µA I_{CC} max

■ Bushold on inputs eliminates the need for external pull-up/pull-down resistors

■ Power down high impedance inputs and outputs

■ ±24 mA output drive (V_{CC} = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:

    Human body model > 2000V

    Machine model > 200V

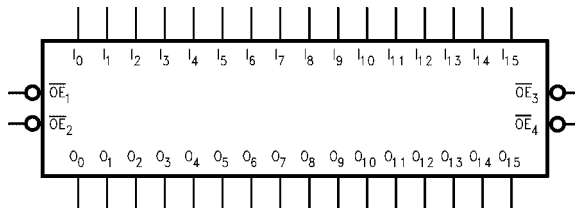■ Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

Order Number	Package Number	Package Description
74LCXH16244G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCXH16244MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCXH16244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

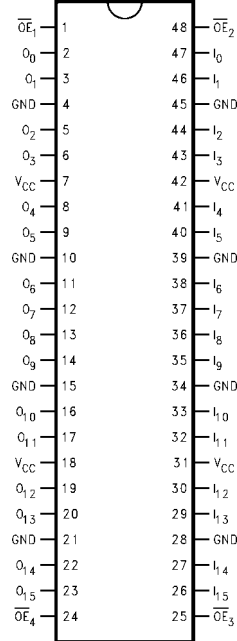**Note 1:** Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
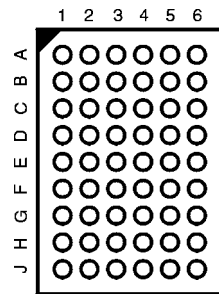
Logic Symbol

DS500248

Connection Diagrams

Pin Assignment for SSOP and TSSOP

$\overline{OE}_1$	1		48	$\overline{OE}_2$
O_0	2		47	I_0
O_1	3		46	I_1
GND	4		45	GND
O_2	5		44	I_2
O_3	6		43	I_3
V_{CC}	7		42	V_{CC}
O_4	8		41	I_4
O_5	9		40	I_5
GND	10		39	GND
O_6	11		38	I_6
O_7	12		37	I_7
O_8	13		36	I_8
O_9	14		35	I_9
GND	15		34	GND
O_{10}	16		33	I_{10}
O_{11}	17		32	I_{11}
V_{CC}	18		31	V_{CC}
O_{12}	19		30	I_{12}
O_{13}	20		29	I_{13}
GND	21		28	GND
O_{14}	22		27	I_{14}
O_{15}	23		26	I_{15}
$\overline{OE}_4$	24		25	$\overline{OE}_3$

Pin Assignment for FBGA

```
      1 2 3 4 5 6
   A  O O O O O O
   B  O O O O O O
   C  O O O O O O
   D  O O O O O O
   E  O O O O O O
   F  O O O O O O
   G  O O O O O O
   H  O O O O O O
   J  O O O O O O
```

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0–I_{15}$	Inputs
$O_0–O_{15}$	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	I_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0–I_3$	$O_0–O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4–I_7$	$O_4–O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8–I_{11}$	$O_8–O_{11}$
L	L	L
L	H	H
H	X	Z

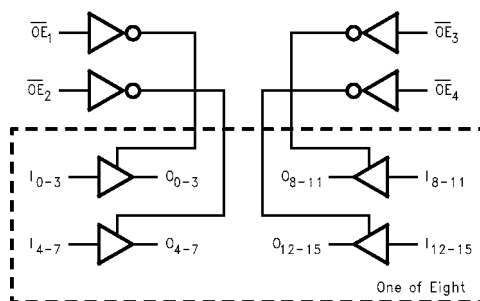| Inputs		Outputs
$\overline{OE}_4$	$I_{12}–I_{15}$	$O_{12}–O_{15}$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level   X = Immaterial
L = LOW Voltage Level   Z = High Impedance

Functional Description

The LCXH16244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram

One of Eight

Absolute Maximum Ratings(Note 3)

Symbol	Parameter		Value	Conditions	Units
V_{CC}	Supply Voltage		−0.5 to +7.0		V
V_I	DC Input Voltage	$\overline{OE}$	−0.5 to +7.0		V
		$I_0 - I_{15}$	−0.5 to V_{CC} + 0.5		
V_O	DC Output Voltage		−0.5 to +7.0	Output in 3-STATE	V
			−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current		−50	V_I < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
			+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}	DC Supply Current per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Recommended Operating Conditions (Note 5)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	
		V_{CC} = 2.7V – 3.0V		±12	mA
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = −40°C to +85°C		Units
					Min	Max	
V_{IH}	HIGH Level Input Voltage			2.3 – 2.7	1.7		V
				2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage			2.3 – 2.7		0.7	V
				2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA		2.3 – 3.6	V_{CC} – 0.2		V
		I_{OH} = −8 mA		2.3	1.8		
		I_{OH} = −12 mA		2.7	2.2		
		I_{OH} = −18 mA		3.0	2.4		
		I_{OH} = −24 mA		3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA		2.3 – 3.6		0.2	V
		I_{OL} = 8 mA		2.3		0.6	
		I_{OL} = 12 mA		2.7		0.4	
		I_{OL} = 16 mA		3.0		0.4	
		I_{OL} = 24 mA		3.0		0.55	
I_I	Input Leakage Current	Data	V_I = V_{CC} or GND	2.3 – 3.6		±5.0	µA
		Control	0 ≤ V_I ≤ 5.5	2.3 – 3.6		±5.0	

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C Min	Max	Units

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	V_{IN} = 0.7V	2.3	45		μA
		V_{IN} = 1.7V		−45		
		V_{IN} = 0.8V	3.0	75		
		V_{IN} = 2.0V		−75		
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State	(Note 6)	2.7	300		μA
		(Note 7)		−300		
		(Note 6)	3.6	450		
		(Note 7)		−450		
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} -0.6V$	2.3 – 3.6		500	μA

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Electrical Characteristics

		$T_A = -40°C$ to $+85°C$, $R_L = 500\ \Omega$						
Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$ C_L = 50 pF		$V_{CC} = 2.7V$ C_L = 50 pF		$V_{CC} = 2.5V \pm 0.2V$ C_L = 30 pF		Units
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	4.5	1.0	5.2	1.0	5.4	ns
t_{PLH}	Data to Output	1.0	4.5	1.0	5.2	1.0	5.4	
t_{PZL}	Output Enable Time	1.0	5.5	1.0	6.3	1.0	7.2	ns
t_{PZH}		1.0	5.5	1.0	6.3	1.0	7.2	
t_{PLZ}	Output Disable Time	1.0	5.4	1.0	5.7	1.0	6.5	ns
t_{PHZ}		1.0	5.4	1.0	5.7	1.0	6.5	
t_{OSHL}	Output to Output Skew (Note 8)		1.0					ns
t_{OSLH}			1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	−0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	−0.6	

Capacitance

| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)
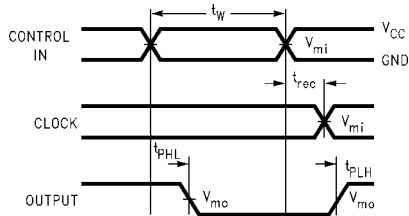
V_I	C_L
6V for V_{CC} = 3.3V, 2.7V	50 pF
V_{CC} * 2 for V_{CC} = 2.5V	30 pF
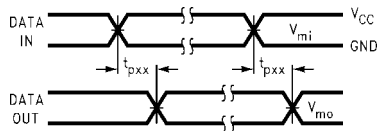
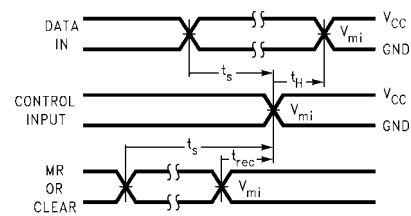
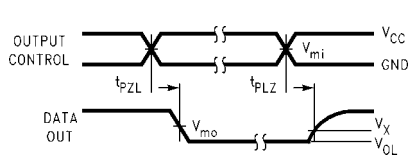Waveform for Inverting and Non-Inverting Functions
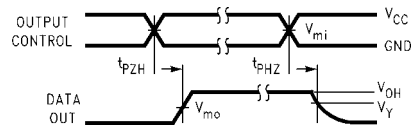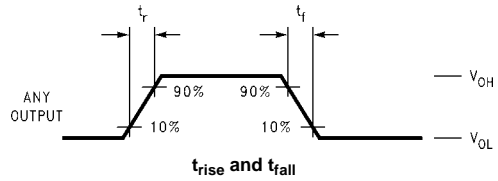

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic

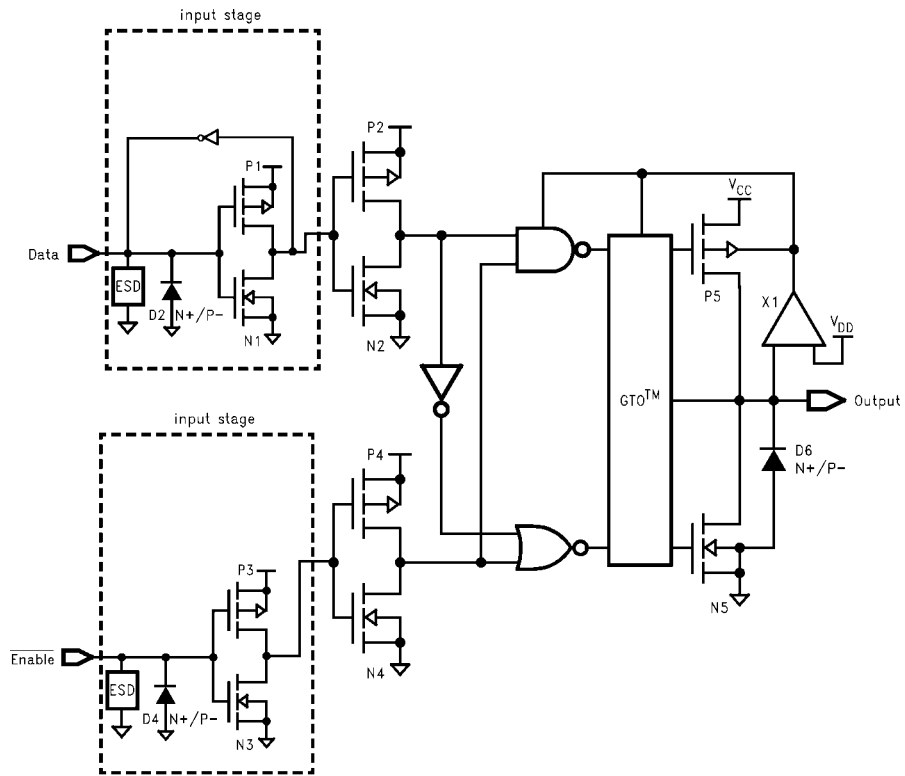3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

FIGURE 2. Waveforms
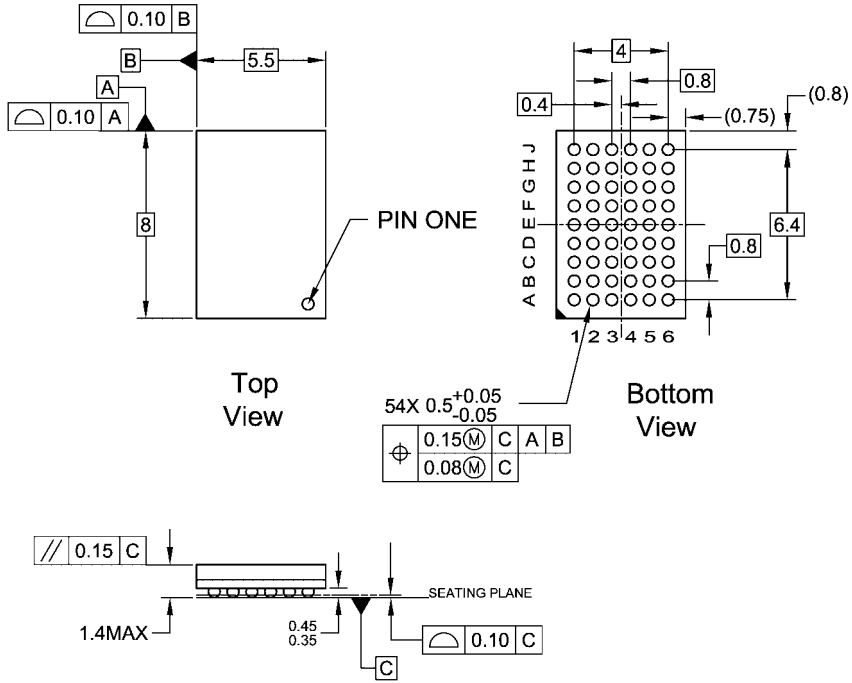(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	2.7V	2.5V $\pm$ 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCXH Family

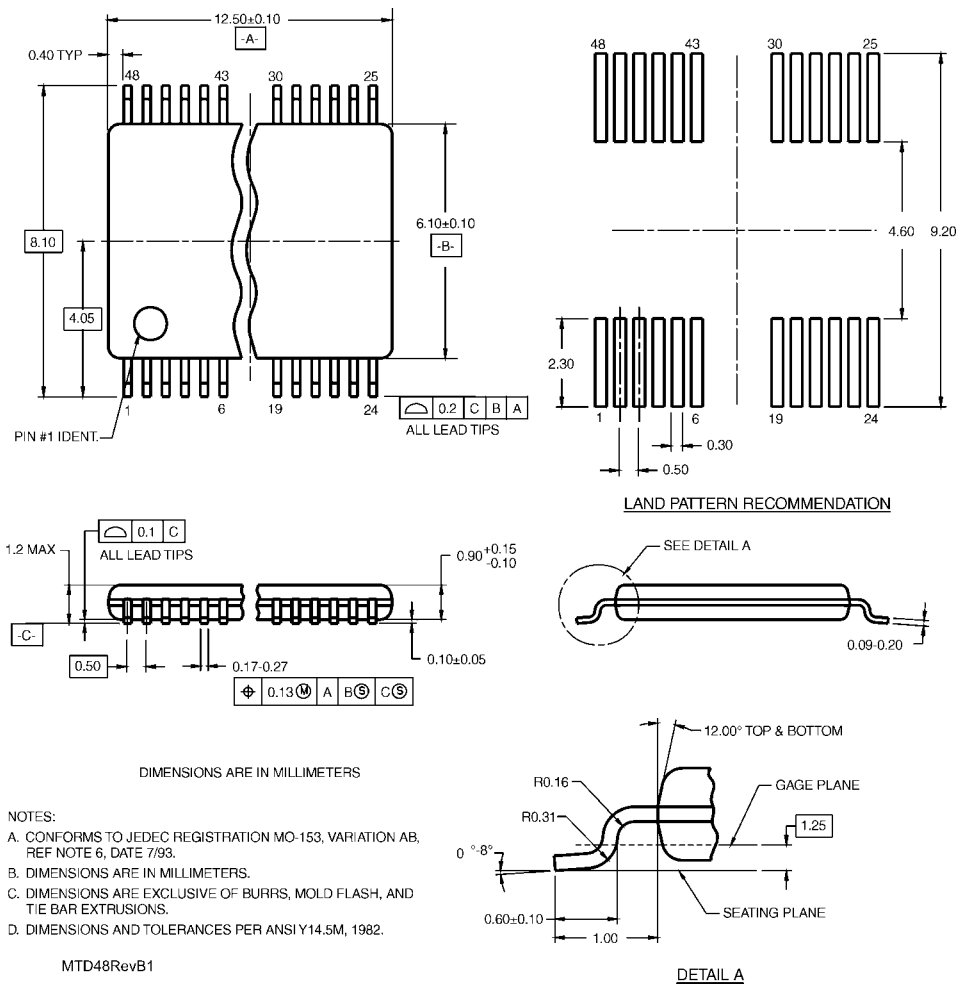## Physical Dimensions inches (millimeters) unless otherwise noted

⌓ 0.10 B

B ◄── 5.5

A

⌓ 0.10 A

8

PIN ONE

Top View

54X 0.5 +0.05 −0.05

⊕ | 0.15Ⓜ | C | A | B
0.08Ⓜ | C

4

0.8

0.4

(0.8)

(0.75)

A B C D E F G H J

6.4

0.8

1 2 3 4 5 6

Bottom View

⫽ 0.15 C

SEATING PLANE

1.4MAX

0.45
0.35

C

⌓ 0.10 C

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

⌀ | 0.010[0.25] | C | B Ⓢ | A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

0.020±0.003
[0.51 ± 0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⌀ | 0.0031[0.08] Ⓜ | C | A Ⓢ | B Ⓢ

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –

– C –

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° – 8° TYP

△ | 0.004[0.10]

MS48A (REV E)

48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

LAND PATTERN RECOMMENDATION

SEE DETAIL A

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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