SN74LS192

PRESETTABLE BCD/DECADE UP/DOWN COUNTER PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

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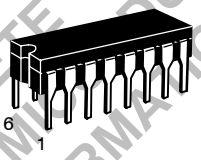
The SN54/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

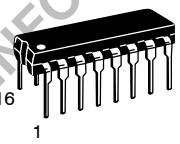
Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided

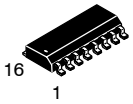
PRESETTABLE BCD/DECADE UP/DOWN COUNTER PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09

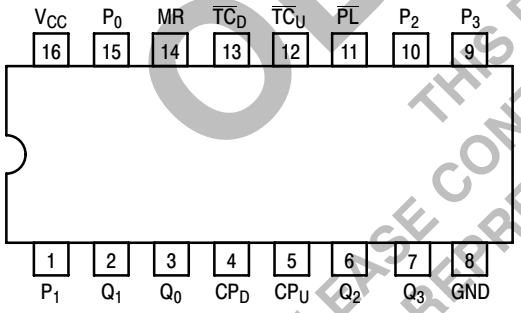


N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ORDERING INFORMATION

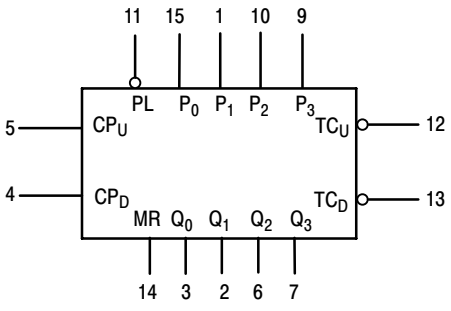
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5 (2.5) U.L.

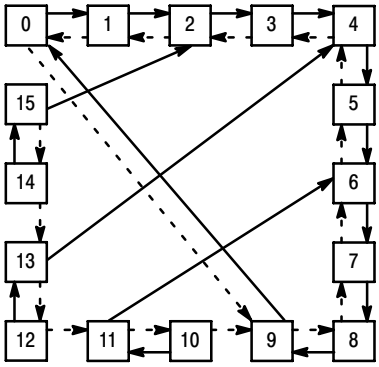
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

STATE DIAGRAMS



LS192

Figure 2. LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

Figure 1.

Figure 3.

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP_U}$

$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$

Figure 4. LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

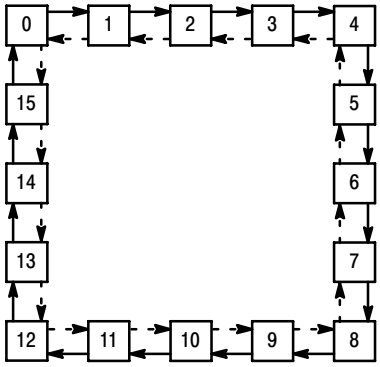
Figure 5.

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$

$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$

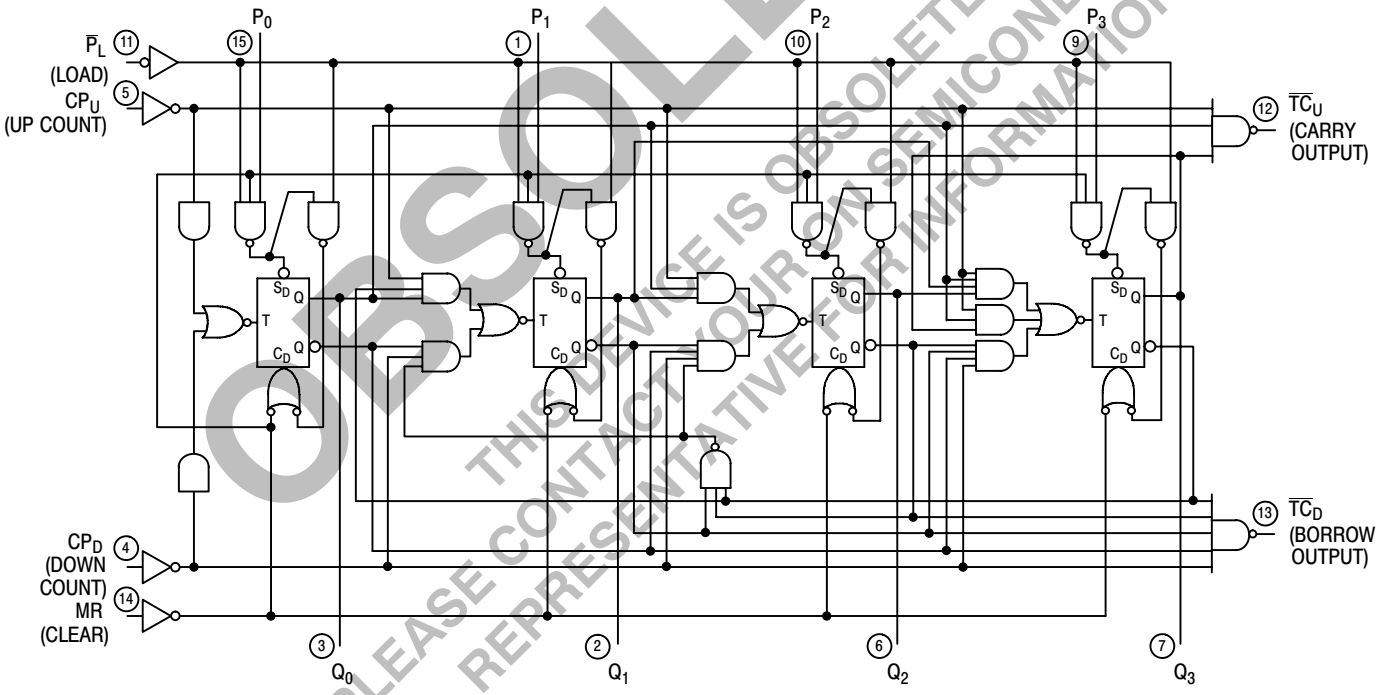
Count Up ——

Count Down - - - - - -



LS193

LOGIC DIAGRAMS

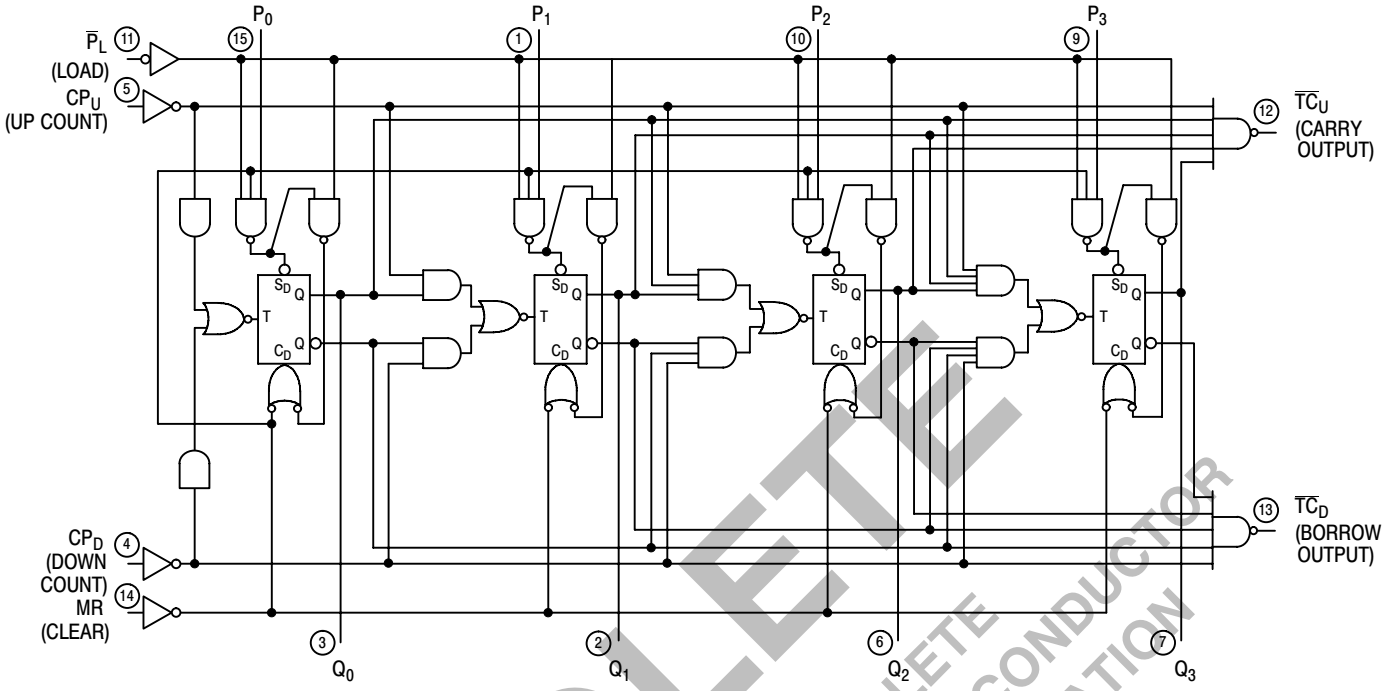


LS192

VCC = PIN 16
GND = PIN 8

◯ = PIN NUMBERS

LOGIC DIAGRAMS (continued)



LS193

V_{CC} = PIN 16
GND = PIN 8

◯ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	CP_U Input to $\overline{TC}_U$ Output		17 18	26 24	ns	
t_{PLH} t_{PHL}	CP_D Input to $\overline{TC}_D$ Output		16 15	24 24	ns	
t_{PLH} t_{PHL}	Clock to Q		27 30	38 47	ns	
t_{PLH} t_{PHL}	$\overline{PL}$ to Q		24 25	40 40	ns	
t_{PHL}	MR Input to Any Output		23	35	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Any Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	40			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{PL}$ transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

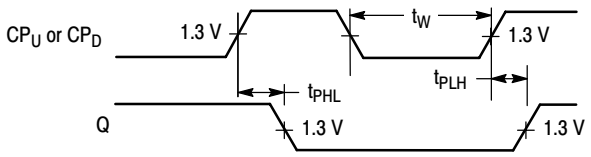


Figure 1

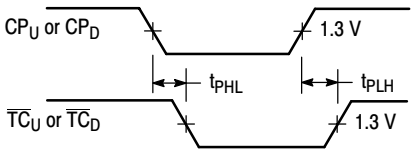
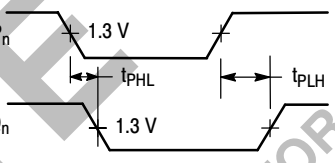


Figure 2



NOTE: $\overline{PL}$ = LOW

Figure 3

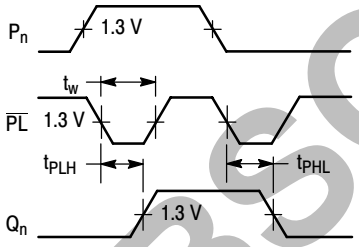


Figure 4

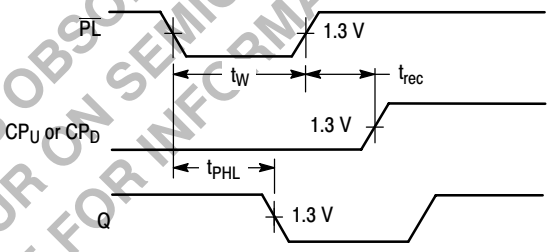
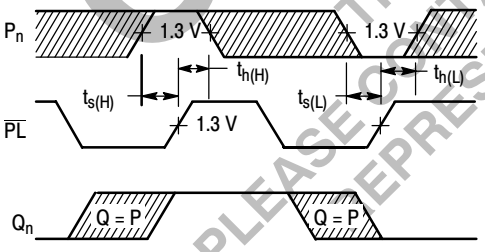


Figure 5



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 6

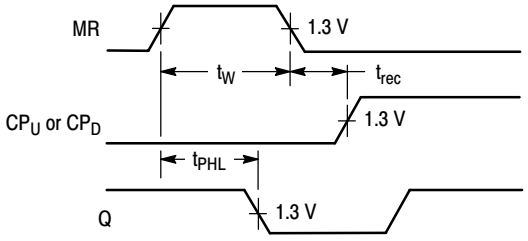


Figure 7

PUBLICATION ORDERING INFORMATION

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