74LVC594A 8-bit shift register with output register Rev. 3 – 20 July 2017

Product data sheet

1 General description

The 74LVC594A is an 8-bit serial-in/serial or parallel-out shift register with a storage register. Separate clock and reset inputs are provided on both shift and storage registers.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The shift register has a serial input (DS) and a serial output (Q7S) for cascading purposes. Data is shifted on the positive-going transitions of the SHCP input. The data in the shift register is transferred to the storage register on a positive-going transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. A LOW level on one of the two register reset pins (SHR and STR) will clear the corresponding register.

2 Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- · Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3 Applications

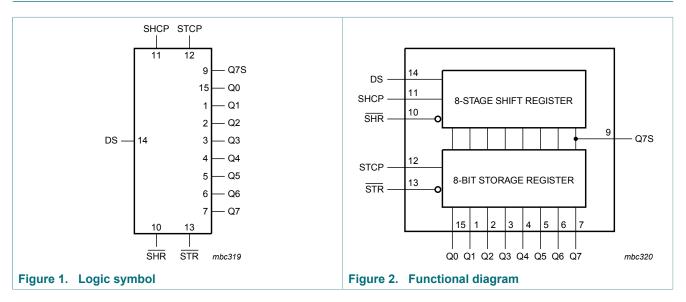
- Serial-to-parallel data conversion
- Remote control holding register



4 Ordering information

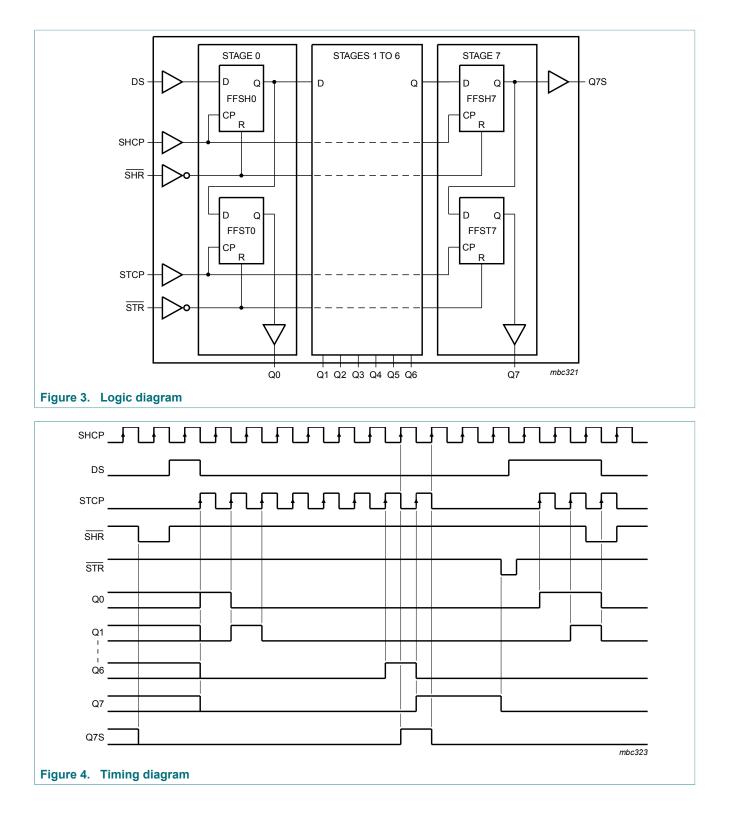
Table 1. Ordering in	Table 1. Ordering information								
Type number	Package								
	Temperature range	Name	Description	Version					
74LVC594AD	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1					
74LVC594APW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1					
74LVC594ABQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	SOT763-1					

5 Functional diagram



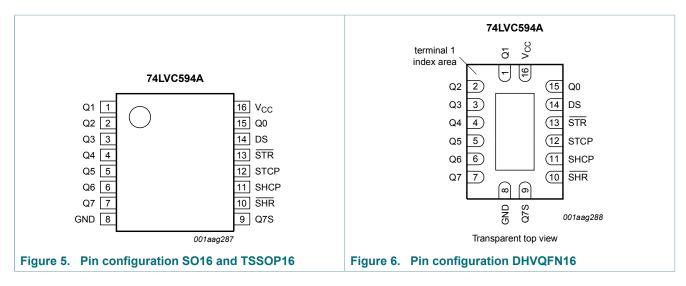
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8-bit shift register with output register



6 Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description							
Symbol	Pin	Description					
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output					
GND	8	ground (0 V)					
Q7S	9	serial data output					
SHR	10	shift register reset (active LOW)					
SHCP	11	shift register clock input					
STCP	12	storage register clock input					
STR	13	storage register reset (active LOW)					
DS	14	serial data input					
V _{CC}	16	supply voltage					

8-bit shift register with output register

Functional description 7

Table 3.	Functio	on table	ə ^[1]				
Input					Outpu	ut	Function
SHCP	STCP	SHR	STR	DS	Q7S	Qn	
х	Х	L	Х	Х	L	NC	a LOW-state on SHR only affects the shift register
Х	Х	Х	L	Х	NC	L	a LOW-state on STR only affects the storage register
Х	1	L	Н	Х	L	L	empty shift register loaded into storage register
1	x	Н	X	Η	Q6S	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)
х	↑	Н	Н	Х	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	Ť	Η	Η	Х	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

[1] H = HIGH voltage state; L = LOW voltage state; \uparrow = LOW-to-HIGH transition; X = don't care; NC = no change.

Limiting values 8

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Мах	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V ₁ < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_{\rm O}$ > $V_{\rm CC}$ or $V_{\rm O}$ < 0 V		-	±50	mA
Vo	output voltage	3-state	[1]	-0.5	6.5	V
		output HIGH or LOW state	[1]	-0.5	V _{CC} + 0.5	V
I _O	output current	V_{O} = 0 V to V_{CC}		-	±50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	500	mW

The input and output voltage ratings may be exceeded if the input and output current ratings are observed. [1]

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

For TSSOP16 packages: above 60 °C the value of Ptot derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9 Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
	functional	functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	3-state	0	-	5.5	V
		output HIGH or LOW state	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

Table 5. Recommended operating conditions

10 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ ^[1]	Max	Min	Мах	
VIH	HIGH-level input	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
	voltage	V _{CC} = 1.65 V to 1.95 V	$0.65V_{CC}$	-	-	0.65V _{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
	voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35V_{CC}$	-	0.35V _{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	voltage	I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} -0.2	-	-	V _{CC} -0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_0 = -12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V

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Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit V V V
			Min	Typ ^[1]	Max	Min	Мах	
V _{OL}	LOW-level output	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	voltage	I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
lı	input leakage current	V_{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{OFF}	power-off leakage current	V_{CC} = 0 V; V ₁ or V ₀ = 5.5 V	-	0.1	10	-	20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; $V_{CC} = 1.65 V \text{ to } 3.6 V;$ $V_I = V_{CC} - 0.6 V; I_O = 0 A$	-	5	500	-	5000	μA
Cı	input capacitance	V_{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

11 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ ^[1]	Мах	Min	Мах	
t _{pd}	propagation delay	SHCP to Q7S; see Figure 7 [2] [3]						
		V _{CC} = 1.2 V	-	17.5	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	5.2	15.8	2.0	18.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.2	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.5	3.5	7.6	1.5	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.1	6.7	1.5	7.7	ns
		STCP to Qn; see Figure 8 [2]						
		V _{CC} = 1.2 V	-	19.3	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	7.6	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.8	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.5	5.2	7.6	1.5	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	4.5	6.7	1.2	7.7	ns
t _{PHL}	HIGH to LOW	SHR to Q7S; see Figure 11						
	propagation delay	V _{CC} = 1.2 V	-	12.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	5.0	15.8	2.0	18.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.8	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.2	3.9	7.6	1.2	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	3.3	6.7	1.2	7.7	ns
		STR to Qn; see Figure 12						
		V _{CC} = 1.2 V	-	20.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	7.7	15.8	2.0	18.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	5.0	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.2	5.3	7.6	1.2	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	4.4	6.7	1.2	7.7	ns

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8-bit shift register with output register

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	o +125 °C	Unit
			Min	Typ ^[1]	Max	Min	Max	
t _W	pulse width	SHCP, STCP HIGH or LOW; see Figure 7 and Figure 8						
		V _{CC} = 1.65 V to 1.95 V	6.0	2.5	-	7.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.0	-	5.5	-	ns
		V _{CC} = 2.7 V	4.5	1.5	-	5.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	4.0	1.5	-	4.5	-	ns
		SHR, STR LOW; see <u>Figure 11</u> and <u>Figure 12</u>						
		V _{CC} = 1.65 V to 1.95 V	6.0	2.5	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	2.0	-	4.5	-	ns
		V _{CC} = 2.7 V	2.5	1.5	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	1.5	-	3.0	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	5.0	1.0	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	0.8	-	4.5	-	ns
		V _{CC} = 2.7 V	2.0	0.6	-	2.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	0.6	-	2.5	-	ns
		SHR to STCP; see Figure 10						
		V_{CC} = 1.65 V to 1.95 V	8.0	3.5	-	8.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.1	-	5.5	-	ns
		V _{CC} = 2.7 V	4.0	1.8	-	4.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	4.0	1.7	-	4.5	-	ns
		SHCP to STCP; see Figure 8						
		V _{CC} = 1.65 V to 1.95 V	8.0	3.5	-	8.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.1	-	5.5	-	ns
		V _{CC} = 2.7 V	4.0	1.8	-	4.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	4.0	1.7	-	4.5	-	ns
t _h	hold time	DS to SHCP; see Figure 9 ^[3]						
		V _{CC} = 1.65 V to 1.95 V	1.5	0.2	-	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	0.1	-	2.0	-	ns
		V _{CC} = 2.7 V	1.5	-0.1	-	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	-0.2	-	1.5	-	ns

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8-bit shift register with output register

Symbol	Parameter	Conditions	-4(°C to +8	5 °C	-40 °C to	o +125 ℃	Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{rec}	recovery time	SHR to SHCP, STR to STCP; see Figure 11 and Figure 12						
		V _{CC} = 1.65 V to 1.95 V	5.0	-2.7	-	5.5	-	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	-1.5	-	4.5	-	ns
		V _{CC} = 2.7 V	2.0	-1.0	-	2.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	-1.0	-	2.5	-	ns
f _{max}	maximum frequency	SHCP or STCP; see Figure 7 and Figure 8						
		V _{CC} = 1.65 V to 1.95 V	80	130	-	70	-	MHz
		V _{CC} = 2.3 V to 2.7 V	100	140	-	90	-	MHz
		V _{CC} = 2.7 V	110	150	-	100	-	MHz
		V _{CC} = 3.0 V to 3.6 V	130	180	-	115	-	MHz
t _{sk(o)}	output skew time	$V_{\rm CC}$ = 3.0 V to 3.6 V ^[4]	·] _	-	1.0	-	1.5	ns
C _{PD}	power dissipation	$V_{I} = GND \text{ to } V_{CC}$	i]					
	capacitance	V _{CC} = 1.65 V to 1.95 V	-	50	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	45	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	44	-	-	-	pF

[1] [2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

 t_{pd} is the same as t_{PLH} and t_{PHL} . Cascadability is guaranteed under identical V_{CC} and temperature conditions.

[3] [4] [5] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design. C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

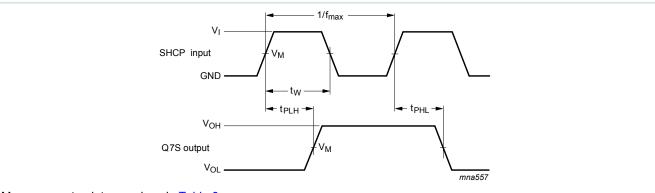
C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs.

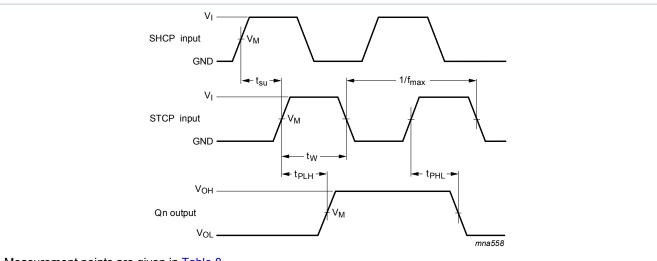
11.1 Waveforms and test circuit



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Figure 7. The shift clock (SHCP) to serial data output (Q7S) propagation delays, the shift clock pulse width and maximum shift clock frequency



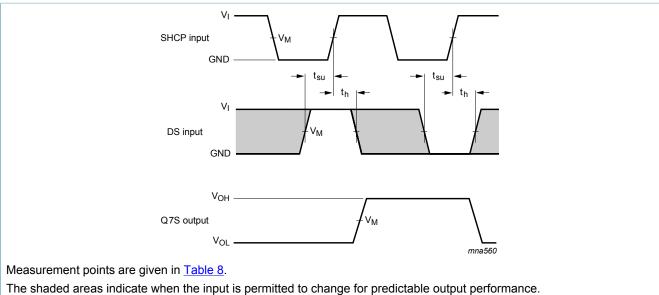
Measurement points are given in <u>Table 8</u>.

 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Figure 8. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time

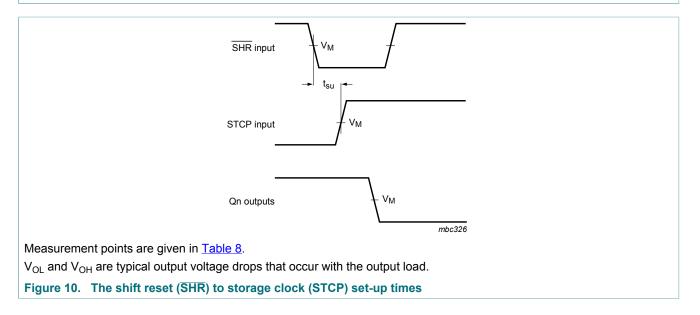
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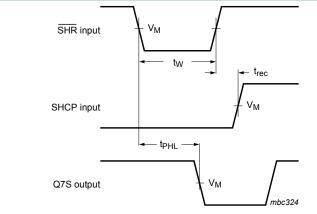
 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Figure 9. The data set-up and hold times for the serial data input (DS)



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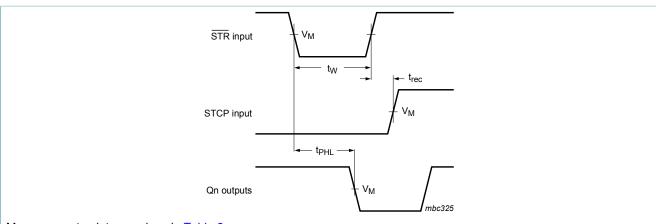
8-bit shift register with output register



Measurement points are given in <u>Table 8</u>.

 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Figure 11. The shift reset (SHR) pulse width, the shift reset to serial data output (Q7S) propagation delays and the shift reset to shift clock (SHCP) recovery time



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Figure 12. The storage reset (STR) pulse width, the storage reset to parallel data output (Qn) propagation delays and the storage reset to storage clock (STCP) recovery time

Table 8. Measurement points

Supply voltage	Input	Output
V _{cc}	V _M	V _M
V _{CC} < 2.7 V	0.5 x V _{CC}	0.5 x V _{CC}
V _{CC} ≥ 2.7 V	1.5 V	1.5 V

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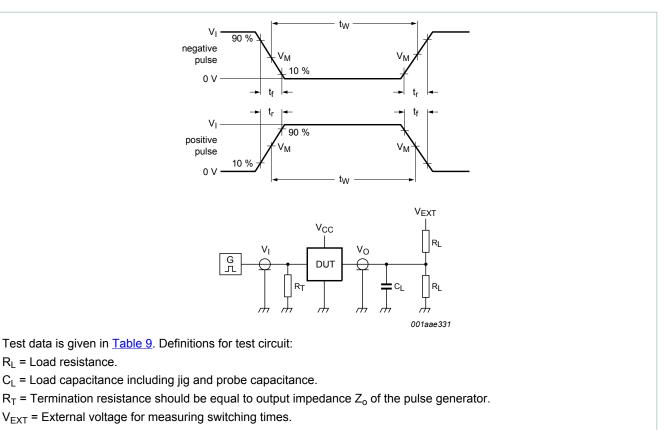
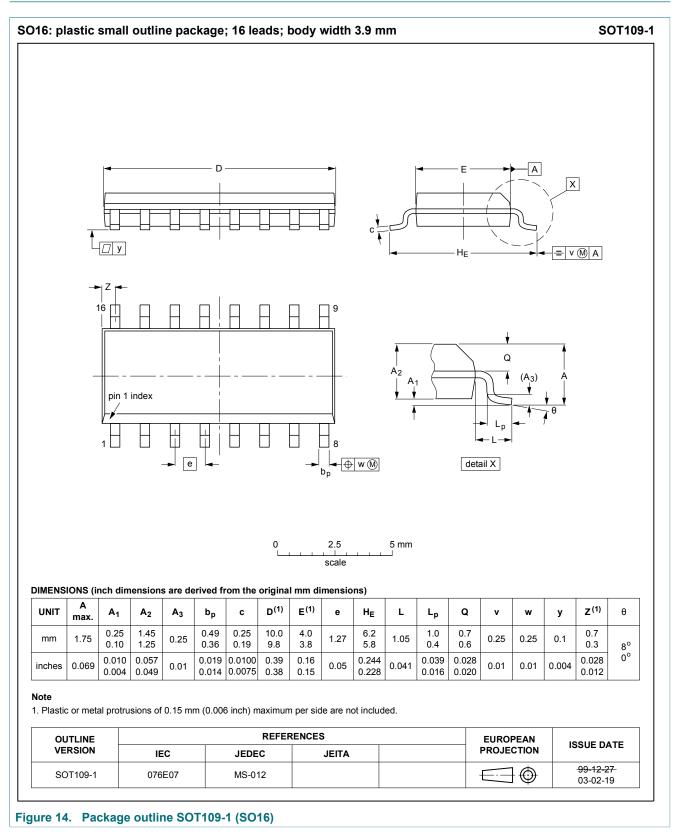


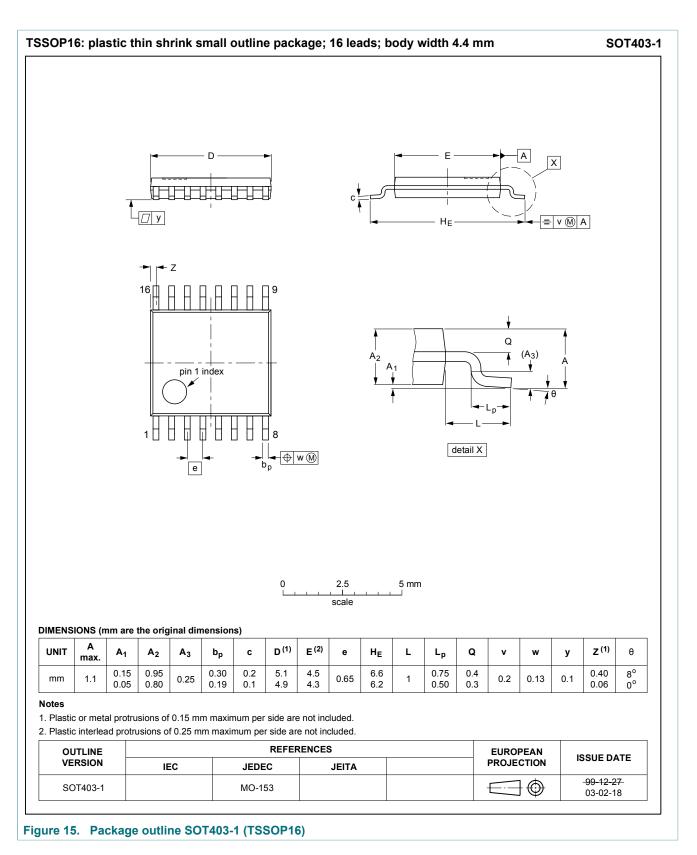
Figure 13. Test circuit for measuring switching times

Supply voltage	Input		Load		V _{EXT}	V _{EXT}		
	VI	t _r , t _f	CL	RL	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}	
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND	
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND	
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND	

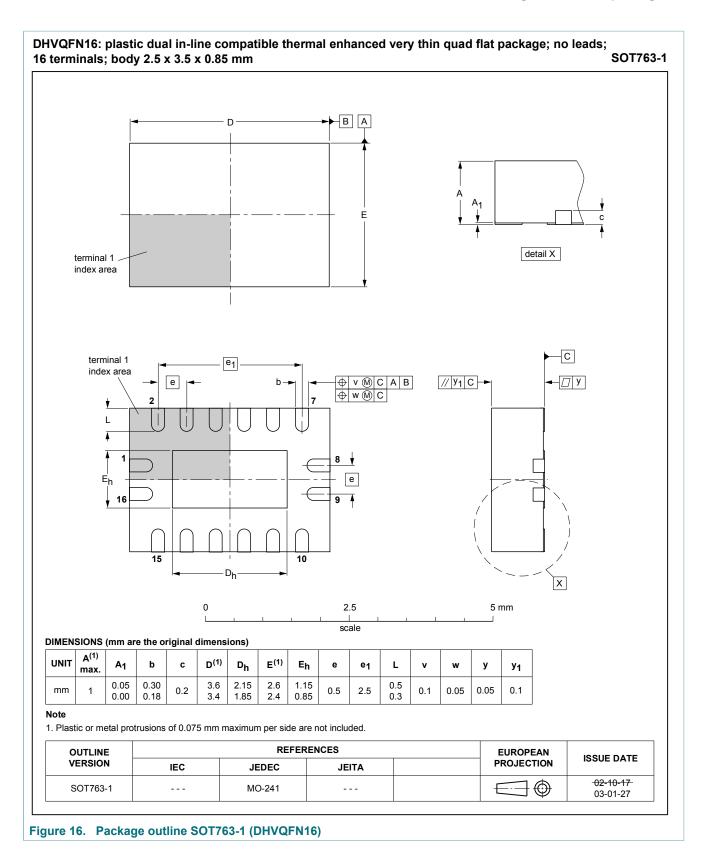
12 Package outline



8-bit shift register with output register



8-bit shift register with output register



13 Abbreviations

Table 10. Abbreviations			
Acronym	Description		
CDM	Charged Device Model		
CMOS	Complementary Metal Oxide Semiconductor		
DUT	Device Under Test		
ESD	ElectroStatic Discharge		
НВМ	Human Body Model		
TTL	Transistor-Transistor Logic		

14 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVC594A v.3	20170720	Product data sheet	-	74LVC594A v.2		
Modifications:	Nexperia. Legal texts hav 	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. <u>Table 7</u>: table note added for cascading purposes. 				
74LVC594A v.2	20131021	Product data sheet	-	74LVC594A v.1		
Modifications:	guidelines of N	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 				
74LVC594A v.1	20070524	Product data sheet	-	-		

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

Please consult the most recently issued document before initiating or completing a design. [1]

The term 'short data sheet' is explained in section "Definitions".

[2] [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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