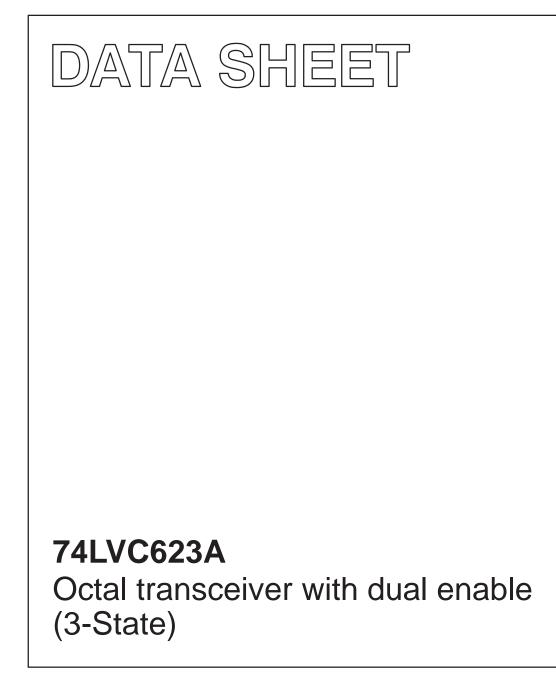
INTEGRATED CIRCUITS



Product specification

1998 Jul 29







74LVC623A

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- Flow-through pin-out architecture
- CMOS low power consumption
- Inputs accept voltages up to 5.5V
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC623A is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC623A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses.

The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels at the enable inputs (OEAB, OEBA). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OEAB and OEBA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The '623A' is identical to the '620A' but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \le 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay An to Bn; Bn to An	$C_L = 50 pF$ $V_{CC} = 3.3V$	3.3	ns
Cl	Input capacitance		5.0	pF
C _{I/O}	Input/output capacitance		10	pF
C _{PD}	Power dissipation capacitance per latch	Notes 1, 2	32	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_{D} in μW)

 $P_D = C_{PD} \times V_{CC}^2 x f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i = \text{input frequency in MHz}; C_L = \text{output load capacity in pF};$ $f_o = \text{output frequency in MHz}; V_{CC} = \text{supply voltage in V};$

 Σ (C_L × V_{CC}² × f_o) = sum of the outputs.

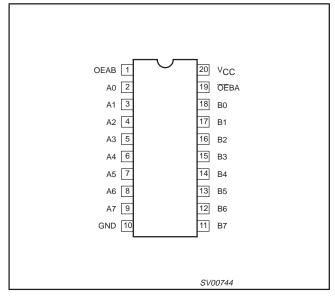
2. The condition is $V_1 = GND$ to V_{CC} .

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	–40°C to +85°C	74LVC623A D	74LVC623A D	SOT163-1
20-Pin Plastic SSOP Type II -40°C to +85°C		74LVC623A DB	74LVC623A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC623A PW	7LVC623APW DH	SOT360-1

74LVC623A

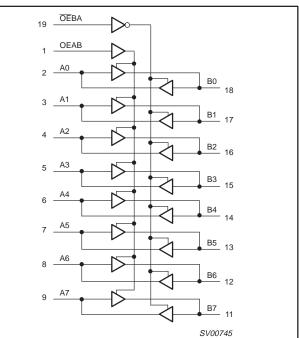
PIN CONFIGURATION



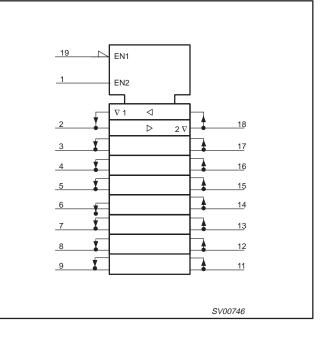
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs
19	OEBA	Output enable input (active LOW)
20	V _{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



74LVC623A

FUNCTION TABLE

INPU	JTS	INPUTS/OUTPUT			
OEAB	OEBA	An	Bn		
L	L	A=B	Inputs		
Н	Н	Inputs	B=A		
L	Н	Z	Z		
Н	L	A=B Inputs	Inputs B=A		

H = High voltage level

L = Low voltage level

Z =High impedance

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIM	UNIT		
STNIDUL	FARAMETER	CONDITIONS	MIN	MAX		
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V	
V _{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V	
VI	DC input voltage range		0	5.5	V	
M	DC output voltage range; output HIGH or LOW state		0	V _{CC}	v	
V _O	DC output voltage range; output 3-State		0	5.5	v	
T _{amb}	Operating free-air temperature range		-40	+85	°C	
t _r , t _f	Input rise and fall times	$V_{CC} = 1.2 \text{ to } 2.7 \text{V}$ $V_{CC} = 2.7 \text{ to } 3.6 \text{V}$	0 0	20 10	ns/V	

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +6.5	V
I _{IK}	DC input diode current	V ₁ < 0	-50	mA
VI	DC input voltage	Note 2	-0.5 to +6.5	V
I _{OK}	DC output diode current	$V_{O} > V_{CC} \text{ or } V_{O} < 0$	± 50	mA
\/	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to V _{CC} +0.5	V
Vo	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	v
Ι _Ο	DC output source or sink current	$V_{O} = 0$ to V_{CC}	± 50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		±100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -					
			MIN	TYP ¹	MAX	1		
M		$V_{CC} = 1.2V$	V _{CC}					
V _{IH}	V _{IH} HIGH level Input voltage	V _{CC} = 2.7 to 3.6V	2.0] `		
M		$V_{CC} = 1.2V$			GND	V		
VIL	LOW level Input voltage	V _{CC} = 2.7 to 3.6V			0.8			
		$V_{CC} = 2.7V; V_I = V_{IH} \text{ or } V_{IL}; I_O = -12mA$	V _{CC} -0.5					
V _{OH} HIGH	HIGH level output voltage	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = -100 \mu A$	$V_{CC} - 0.2$	V _{CC}		v		
	Thornever output voltage	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = -18\text{mA}$	$V_{CC} - 0.6$					
		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = -24mA$	$V_{CC} - 0.8$					
		$V_{CC} = 2.7V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 12mA$			0.40			
V _{OL}	LOW level output voltage	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100 \mu A$		GND	0.20	V		
		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 24\text{mA}$			0.55	1		
l	Input leakage current	$V_{CC} = 3.6V; V_1 = 5.5V \text{ or GND}$		±0.1	±5	μΑ		
I _{OZ}	3-State output OFF-state current	$V_{CC} = 3.6V; V_I = V_{IH} \text{ or } V_{IL}; V_O = 5.5V \text{ or GND}$		0.1	±5	μA		
I _{off}	Power off leakage supply	$V_{CC} = 0.0V; V_{I} \text{ or } V_{O} = 5.5V$		0.1	±10	μA		
I _{CC}	Quiescent supply current	$V_{CC} = 3.6V$; $V_I = V_{CC}$ or GND; $I_O = 0$		0.1	10	μA		
ΔI_{CC}	Additional quiescent supply current per input pin	$V_{CC} = 2.7V$ to 3.6V; $V_I = V_{CC} - 0.6V$; $I_O = 0$		5	500	μΑ		

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; t_r = $t_f\,\leq\,$ 2.5 ns; C_L = 50 pF

					LIMITS			
SYMBOL	PARAMETER	WAVEFORM	V _C	_C = 3.3V ±0	.3V	V _{CC} =	UNIT	
			MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} /t _{PLH}	Propagation delay An to Bn, Bn to An	Figures 1, 4	1.5	2.3	6	1.5	7	ns
t _{PZH} /t _{PZL}	3-State output enable time OEAB to Bn	Figures 3, 4	1.5	4.6	7.6	1.5	8.6	ns
t _{PHZ} /t _{PLZ}	3-State output disable time OEAB to Bn	Figures 3, 4	1.5	4.0	6.5	1.5	7.5	ns
t _{PZH} /t _{PZL}	3-State output enable time OEBA to An	Figures 2, 4	1.5	4.4	7.9	1.5	8.9	ns
t _{PHZ} /t _{PLZ}	3-State output disable time OEBA to An	Figures 2, 4	1.5	3.7	6.5	1.5	7.5	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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AC WAVEFORMS

 V_M = 1.5V at V_{CC} $\geq~2.7V$ V_{M} = 0.5V * V_{CC} at V_{CC} < 2.7V V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load. $V_X = V_{OL} \text{ at } 0.3 V \ge 2.7 V$ $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7 V$ V_{Y} = V_{OH} – 0.3V at $V_{CC}\,\geq\,2.7V$ $V_{Y} = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7 V$ Vi A_n, B_n INPUT Vм GND ^tPHL ^tPLH VOH A_n, B_n OUTPUT Vм VOL SV00747



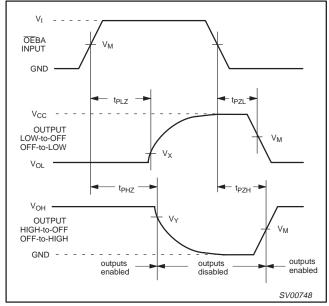


Figure 2. 3-State enable and disable times for $\overline{\text{OEBA}}$ input

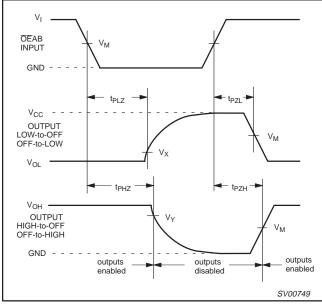


Figure 3. 3-State enable and disable times for OEAB input

TEST CIRCUIT

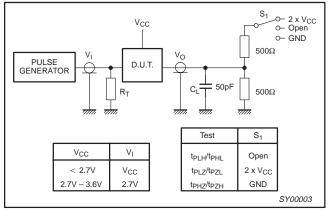
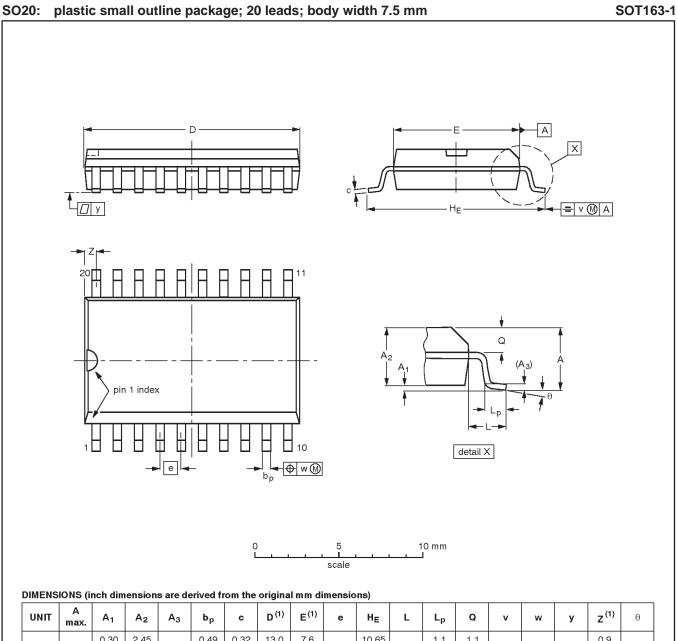


Figure 4. Load circuitry for switching times

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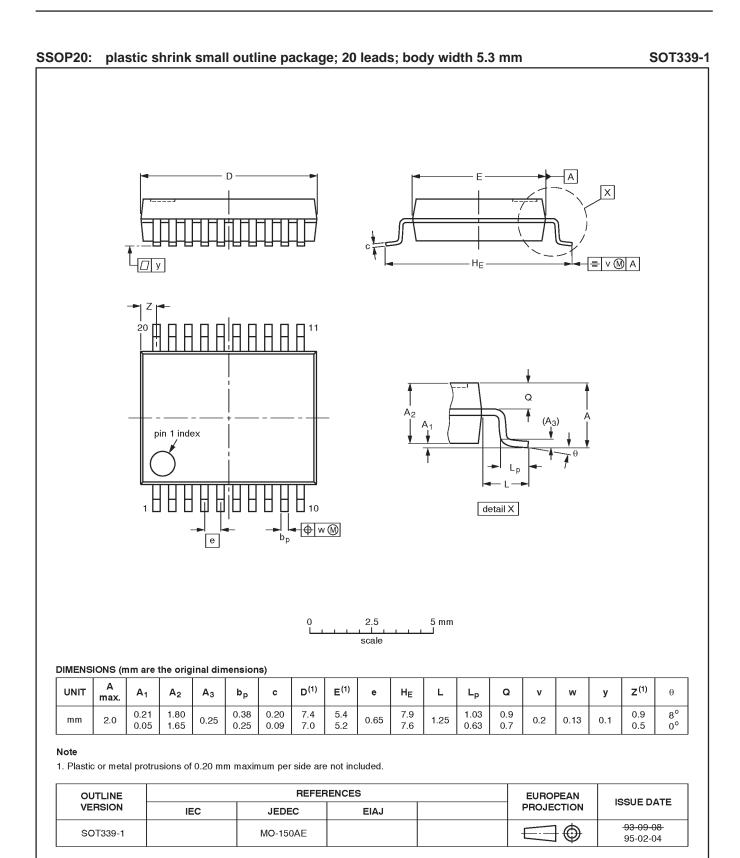
	max.		_	-	٣					_		٣					-	
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

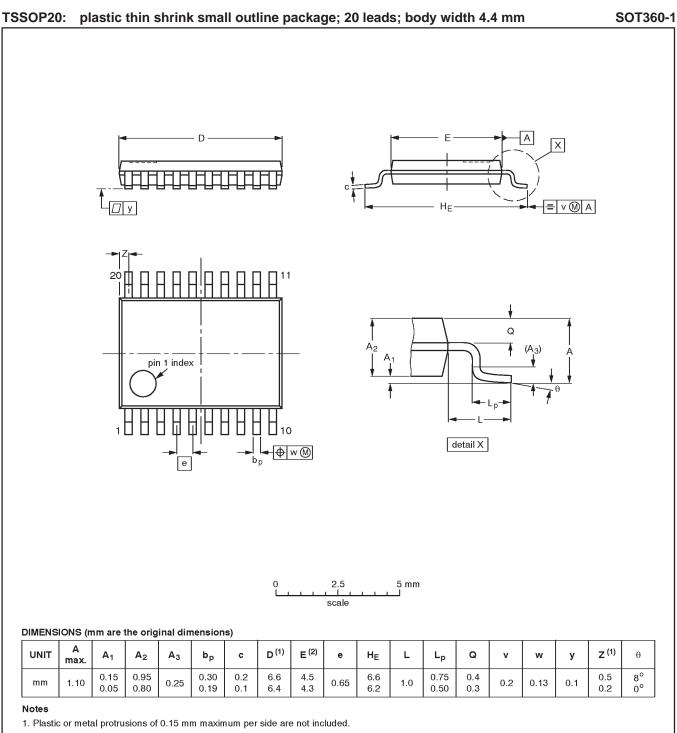
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE				
VERSION	IEC	JEDEC	EIAJ		PROJECTION	PROJECTION		
SOT163-1	075E04	MS-013AC				-92-11-17 95-01-24		

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2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	I ISSUE DATE	
SOT360-1		MO-153AC				-93-06-16 95-02-04	

74LVC623A

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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Limiting values definition - Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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