



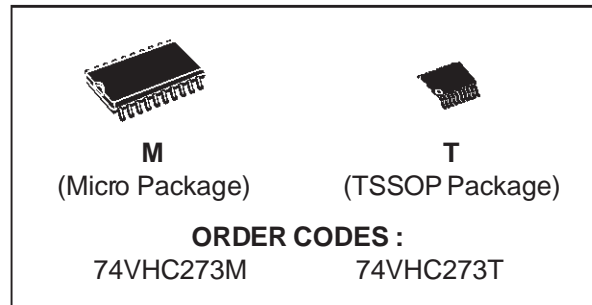
OCTAL D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:
 $f_{MAX} = 165 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 273
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE $V_{OLP} = 0.9\text{V (Max.)}$

DESCRIPTION

The 74VHC273 is an advanced high-speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

PRELIMINARY DATA



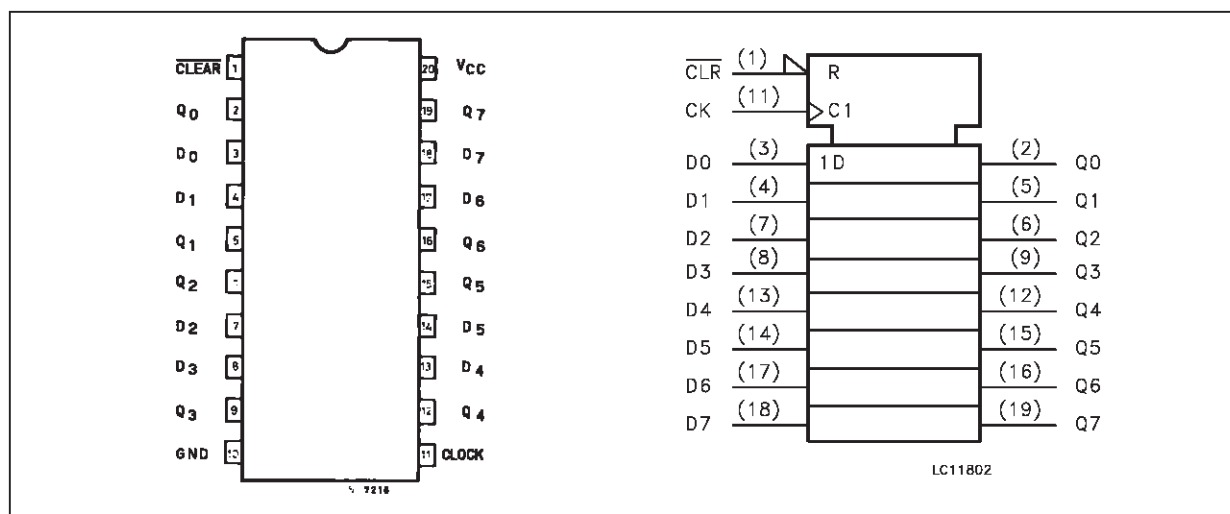
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the CLEAR input is held low, the Q outputs are held low independently of the other inputs .

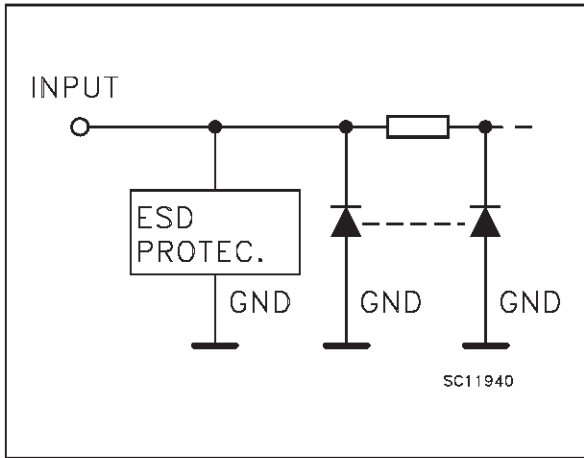
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

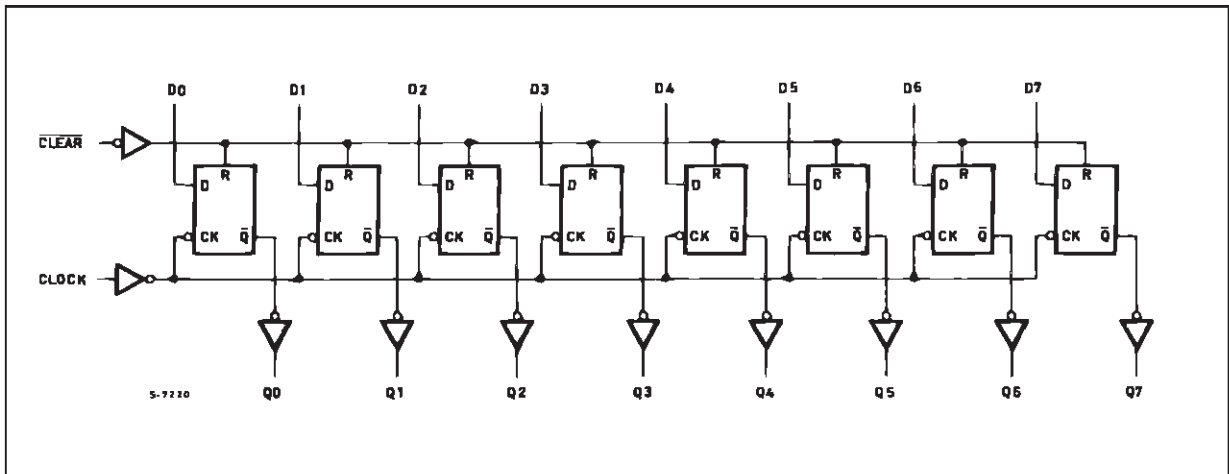
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip-Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW-to-HIGH, Edge-Triggered)
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLEAR}}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q _n	NO CHANGE

X: Don't Care

LOGIC DIAGRAMS



This logic diagram has not been used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 75	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2.0 to 5.5	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 1) (V _{CC} = 3.3 ± 0.3V) (V _{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
				T _A = 25 °C			-40 to 85 °C			
				V _{CC} (V)	Min.	Typ.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		3.0 to 5.5			0.7V _{CC}			0.7V _{CC}		
V _{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		3.0 to 5.5					0.3V _{CC}		0.3V _{CC}	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9			V
		3.0	I _O =-50 μA	2.9	3.0		2.9			
		4.5	I _O =-50 μA	4.4	4.5		4.4			
		3.0	I _O =-4 mA	2.58			2.48			
		4.5	I _O =-8 mA	3.94			3.8			
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		V
		3.0	I _O =50 μA		0.0	0.1		0.1		
		4.5	I _O =50 μA		0.0	0.1		0.1		
		3.0	I _O =4 mA			0.36		0.44		
		4.5	I _O =8 mA			0.36		0.44		
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND				±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND				4		40	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q	3.3 ^(*)	15			8.7	13.6	1.0	16.0	ns
		3.3 ^(*)	50			11.2	17.1	1.0	19.5	
		5.0 ^(**)	15			5.8	9.0	1.0	10.5	
		5.0 ^(**)	50			7.3	11.0	1.0	12.5	
t _{PHL}	Propagation Delay Time CLR to Q	3.3 ^(*)	15			8.9	13.6	1.0	16.0	ns
		3.3 ^(*)	50			11.4	17.1	1.0	19.5	
		5.0 ^(**)	15			5.2	8.5	1.0	10.0	
		5.0 ^(**)	50			6.7	10.5	1.0	12.0	
t _w	CLR pulse Width LOW	3.3 ^(*)					5.0		6.0	ns
		5.0 ^(**)						5.0	5.0	
t _w	CK pulse Width HIGH or LOW	3.3 ^(*)					5.5		6.5	ns
		5.0 ^(**)						5.0	5.0	
t _s	Setup Time D to CK HIGH or LOW	3.3 ^(*)					5.5		6.5	ns
		5.0 ^(**)						4.5	4.5	
t _h	Hold Time D to CK HIGH or LOW	3.3 ^(*)					1.0		1.0	ns
		5.0 ^(**)						1.0	1.0	
t _{REM}	Removal Time CLR to CK	3.3 ^(*)					2.5		2.5	ns
		5.0 ^(**)						2.0	2.0	
f _{MAX}	Maximum Clock Frequency	3.3 ^(*)	15		75	120		65		MHz
		3.3 ^(*)	50		50	75		45		
		5.0 ^(**)	15		120	165		100		
		5.0 ^(**)	50		80	110		70		
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1)	3.3 ^(*)	50				1.5		1.5	ns
		5.0 ^(**)	50					1.0	1.0	

(*) Voltage range is 3.3V ± 0.3V

(**) Voltage range is 5V ± 0.5V

Note 1: Parameter guaranteed by design. t_{soLH} = |t_{pLHm} - t_{pLHr}|, t_{soHL} = |t_{pHLm} - t_{pHLr}|

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T _A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance			4	10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)			31				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(OPR)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/8 (per Flip-Flop)

DYNAMIC SWITCHING CHARACTERISTICS

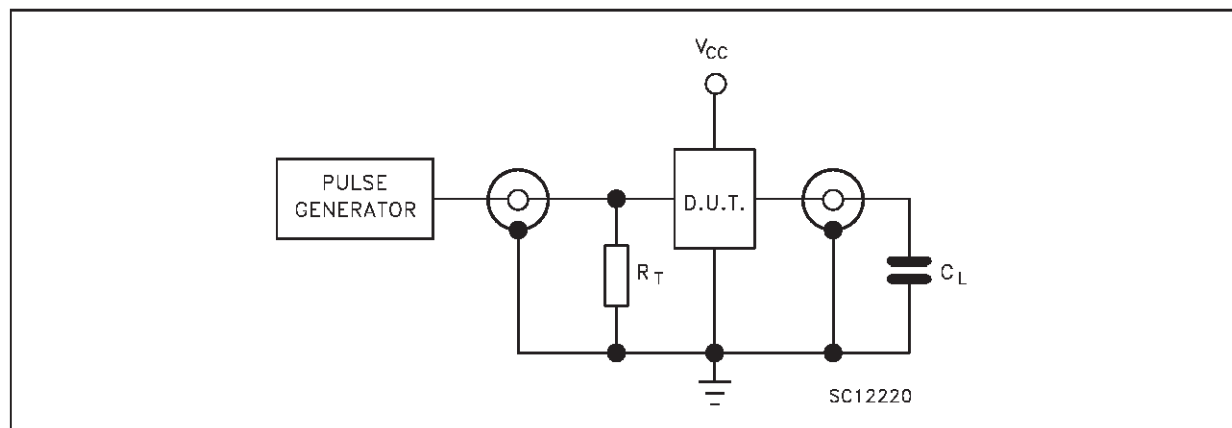
Symbol	Parameter	Test Conditions		Value					Unit
				T _A = 25 °C			-40 to 85 °C		
		V _{CC} (V)		Min.	Typ.	Max.	Min.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.6	0.9			V
V _{OLV}				-0.9	-0.6				
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5					
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5			

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching, (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

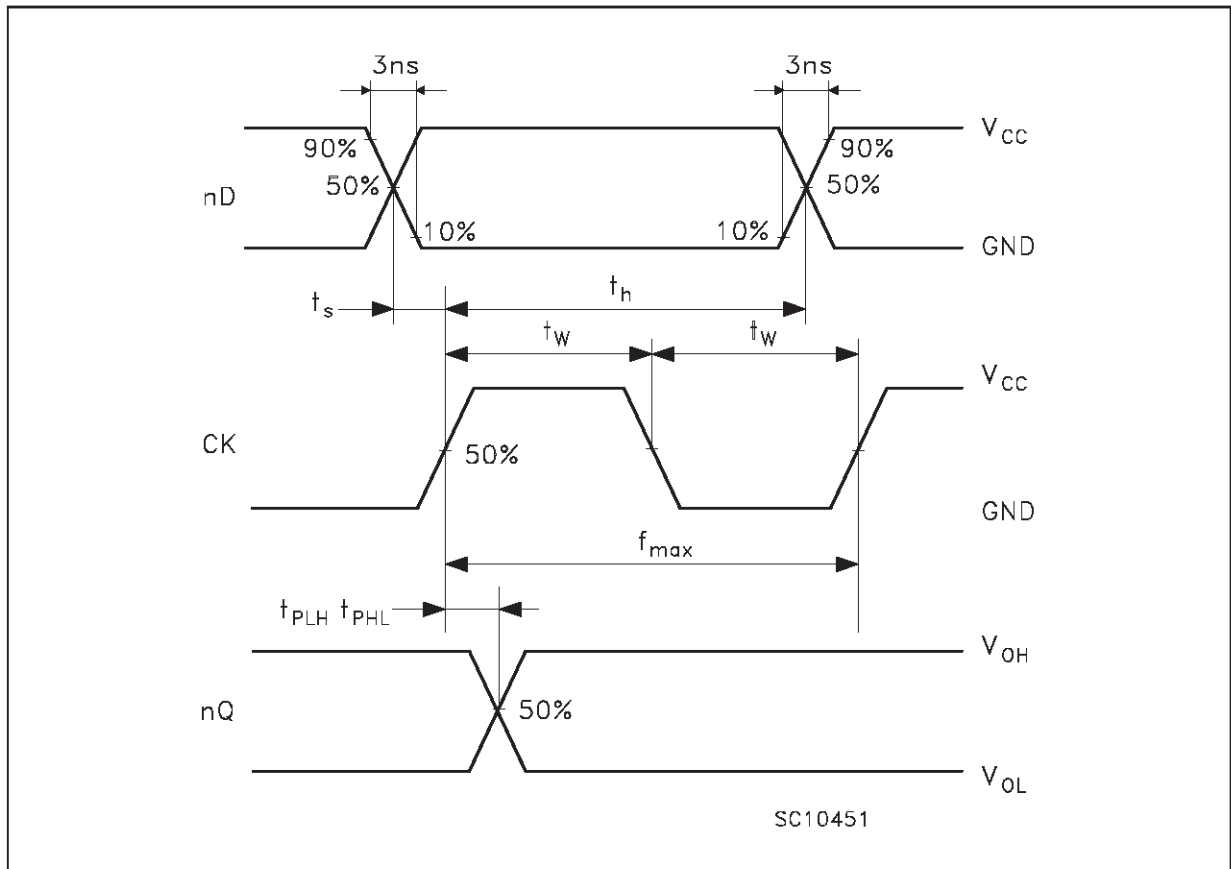
TEST CIRCUIT

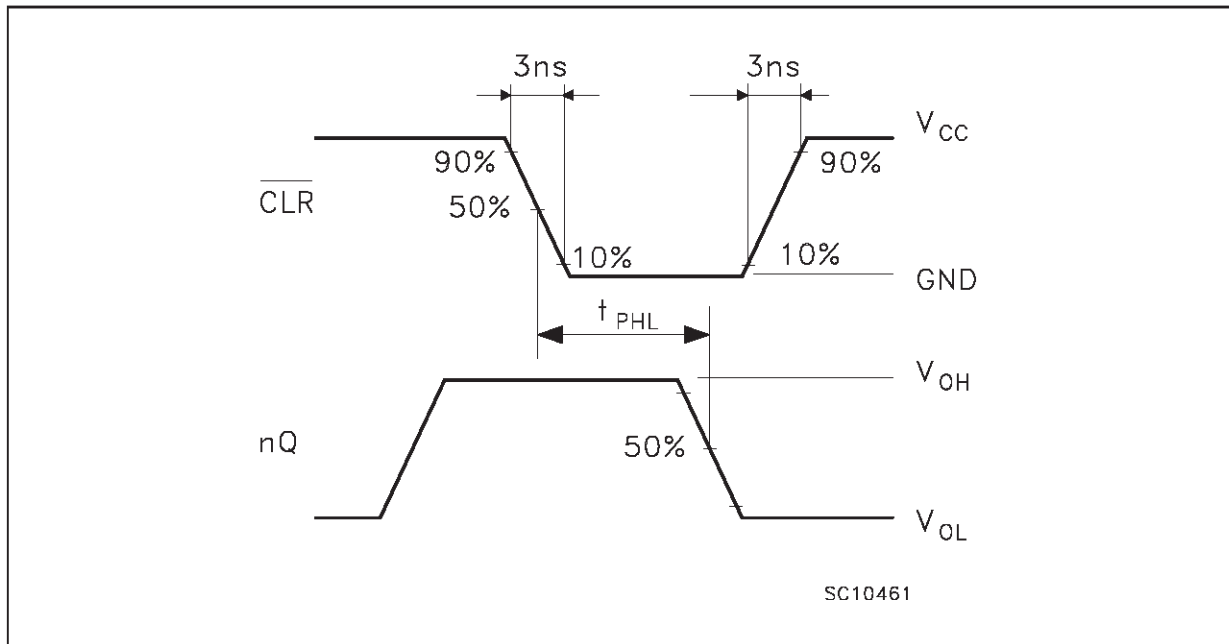
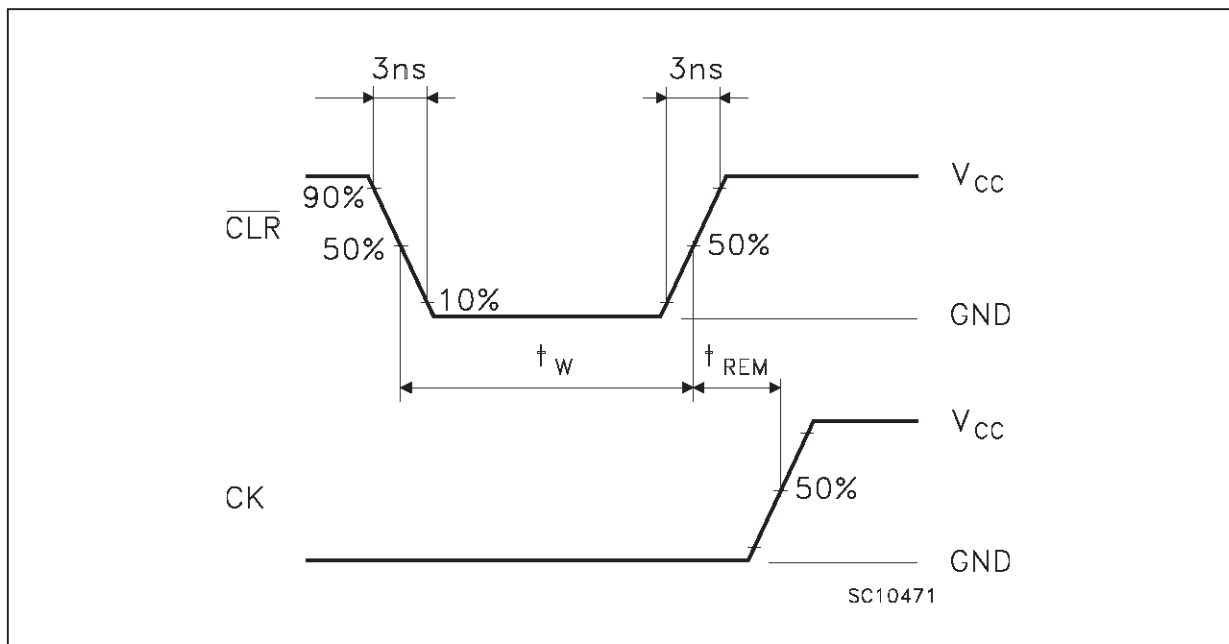


C_L = 15/50 pF or equivalent (includes jig and probe capacitance)

R_T = Z_{OUT} of pulse generator (typically 50Ω)

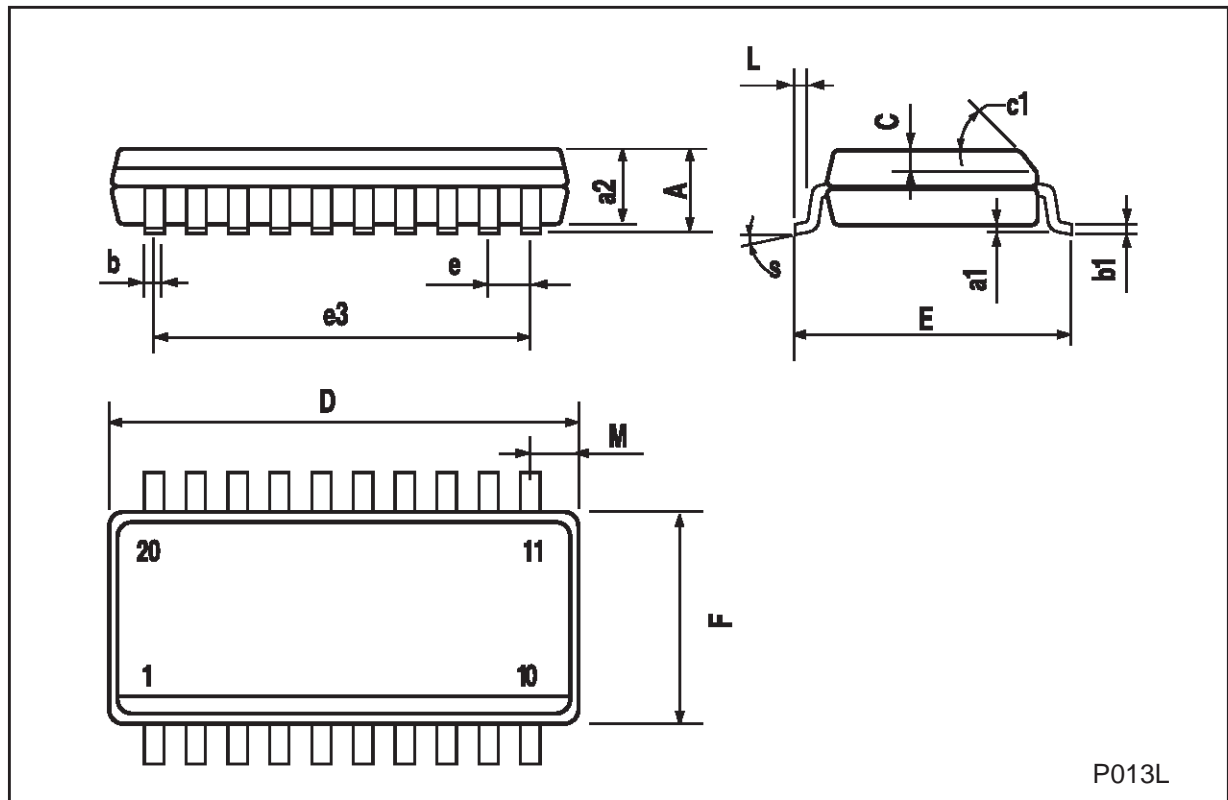
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)**WAVEFORM 3: RECOVERY TIME** (f=1MHz; 50% duty cycle)

SO-20 MECHANICAL DATA

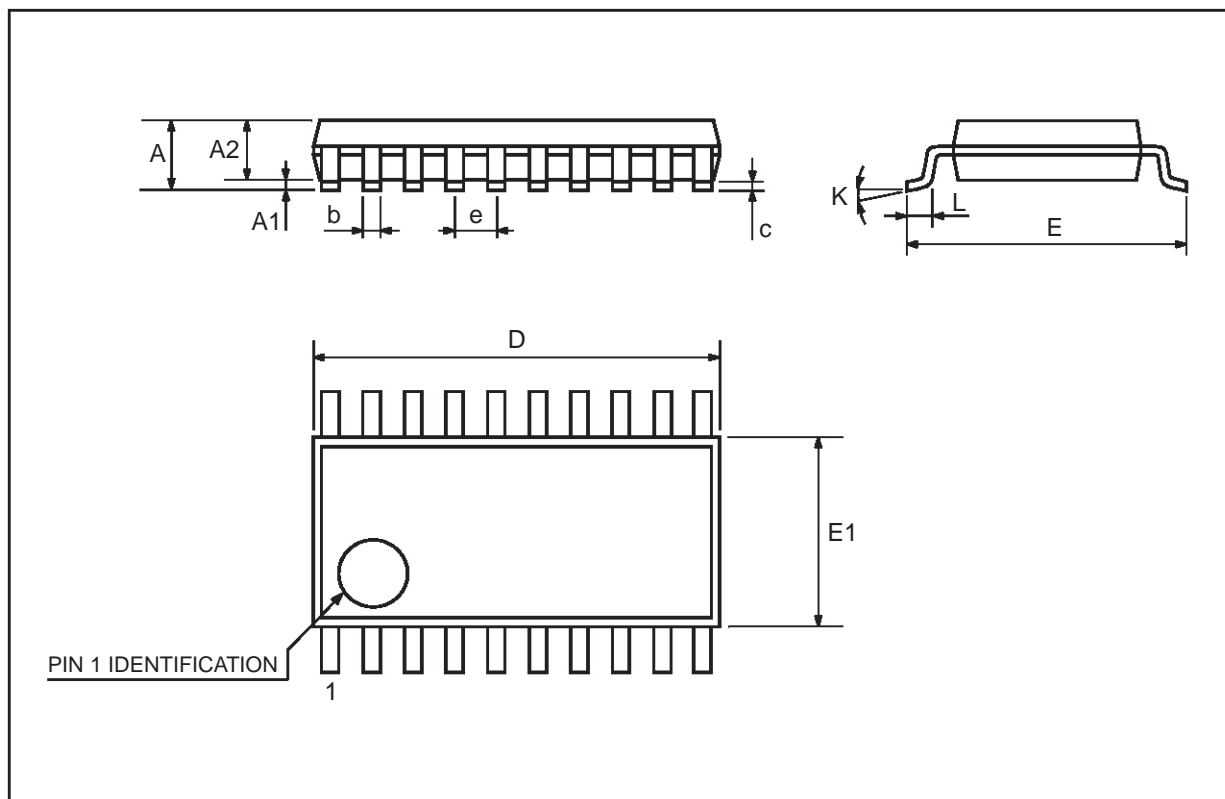
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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