FAIRCHILD SEMICONDUCTOR®

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74VHC74
Dual D-Type Flip-Flop with Preset and Clear

Features

- High Speed: f_{MAX} = 170MHz (typ.) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Power down protection is provided on all inputs
- Low power dissipation: I_{CC} = 2µA (max.) at T_A = 25°C
- Pin and function compatible with 74HC74

General Description

The VHC74 is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D input is transferred to the Q output during the positive going transition of the CK pulse. $\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input LOW.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

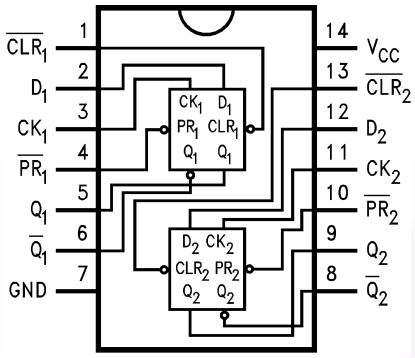
Ordering Information

Order Number	Package Number	Package Description
74VHC74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

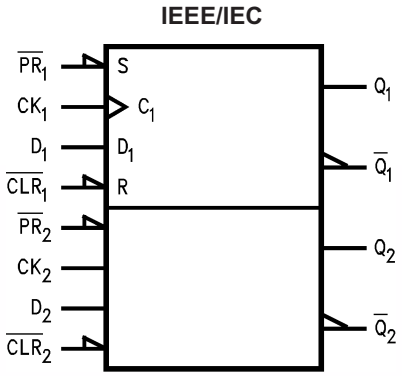
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Output

Truth Table

Inputs				Outputs		
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	Function
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H(1)	H(1)	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

Note:

1. This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) state.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions[2]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time, V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	 0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

Note:

2. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50µA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I_{OH} = –4mA	2.58			2.48		
		4.5		I_{OH} = –8mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50µA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I_{OL} = 4mA			0.36		0.44	
		4.5		I_{OL} = 8mA			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				2.0		20.0	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	C_L = 15pF	80	125		70		MHz
			C_L = 50pF	50	75		45		
		5.0 ± 0.5	C_L = 15pF	130	170		110		
			C_L = 50pF	90	115		75		
t_{PLH}, t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	3.3 ± 0.3	C_L = 15pF		6.7	11.9	1.0	14.0	ns
			C_L = 50pF		9.2	15.4	1.0	17.5	
		5.0 ± 0.5	C_L = 15pF		4.6	7.3	1.0	8.5	
			C_L = 50pF		6.1	9.3	1.0	10.5	
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ -Q, $\overline{Q}$)	3.3 ± 0.3	C_L = 15pF		7.6	12.3	1.0	14.5	ns
			C_L = 50pF		10.1	15.8	1.0	18.0	
		5.0 ± 0.5	C_L = 15pF		4.8	7.7	1.0	9.0	
			C_L = 50pF		6.3	9.7	1.0	11.0	
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		(3)		25				pF

Note:

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC} / 2 (per F/F).

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)(4)	T_A = 25°C		T_A = –40°C to +85°C	Units
			Typ.	Guaranteed Minimum		
t_W(L), t_W(H)	Minimum Pulse Width (CK)	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_H	Minimum Hold Time	3.3		0.5	0.5	ns
		5.0		0.5	0.5	
t_{REC}	Minimum Recovery Time ($\overline{CLR}$, $\overline{PR}$)	3.3		5.0	5.0	ns
		5.0		3.0	3.0	

Note:

4. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

Physical Dimensions

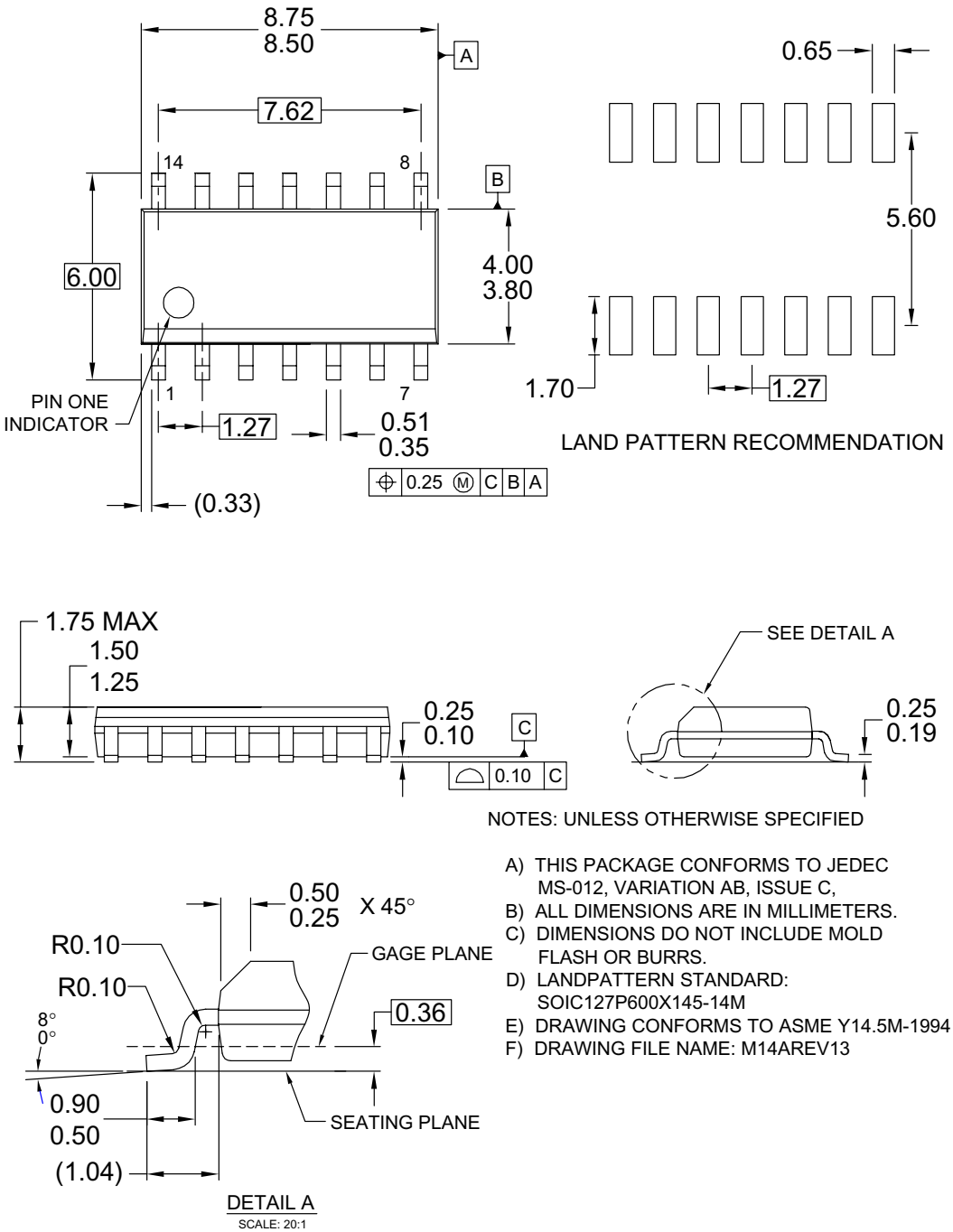


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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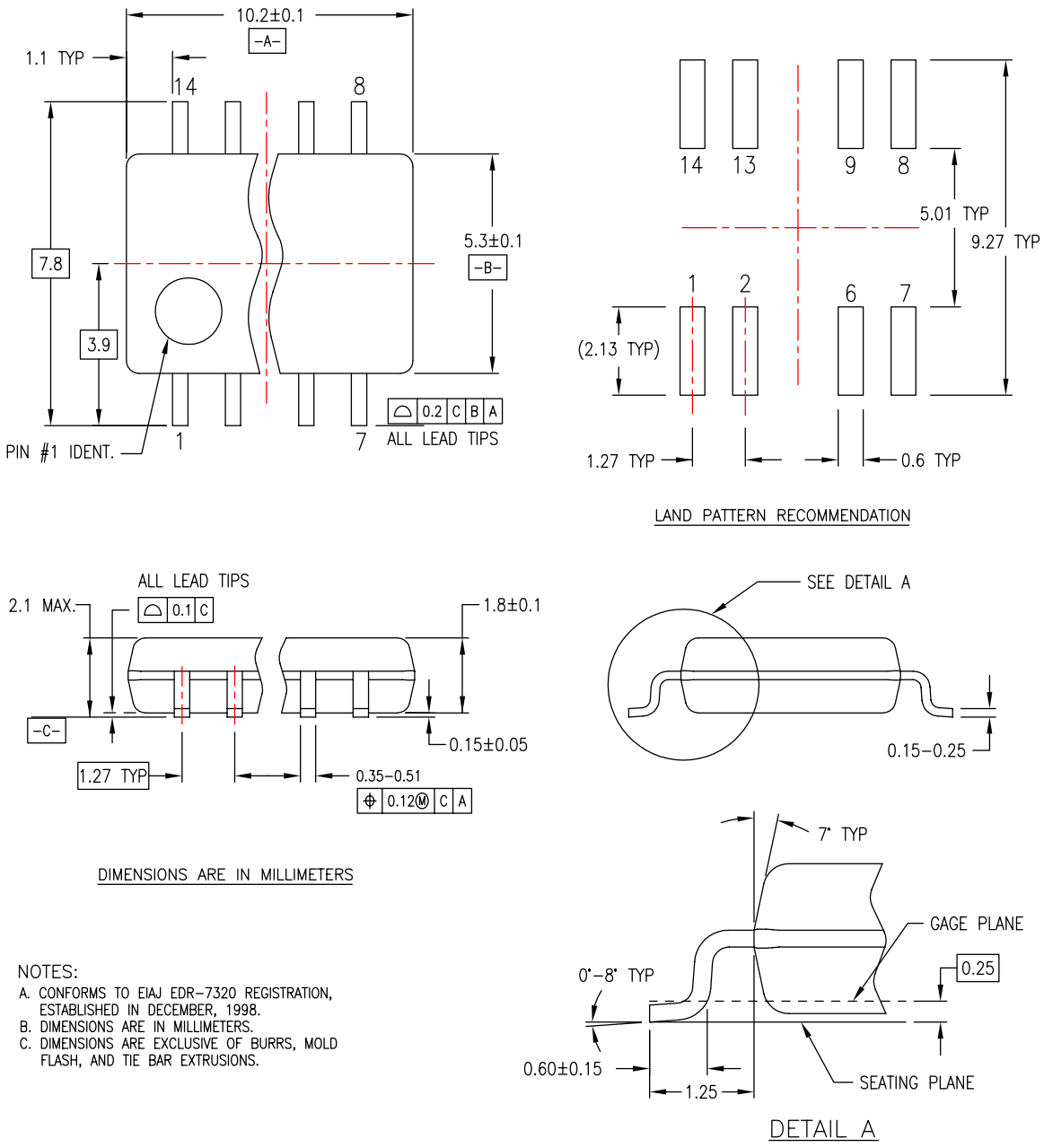
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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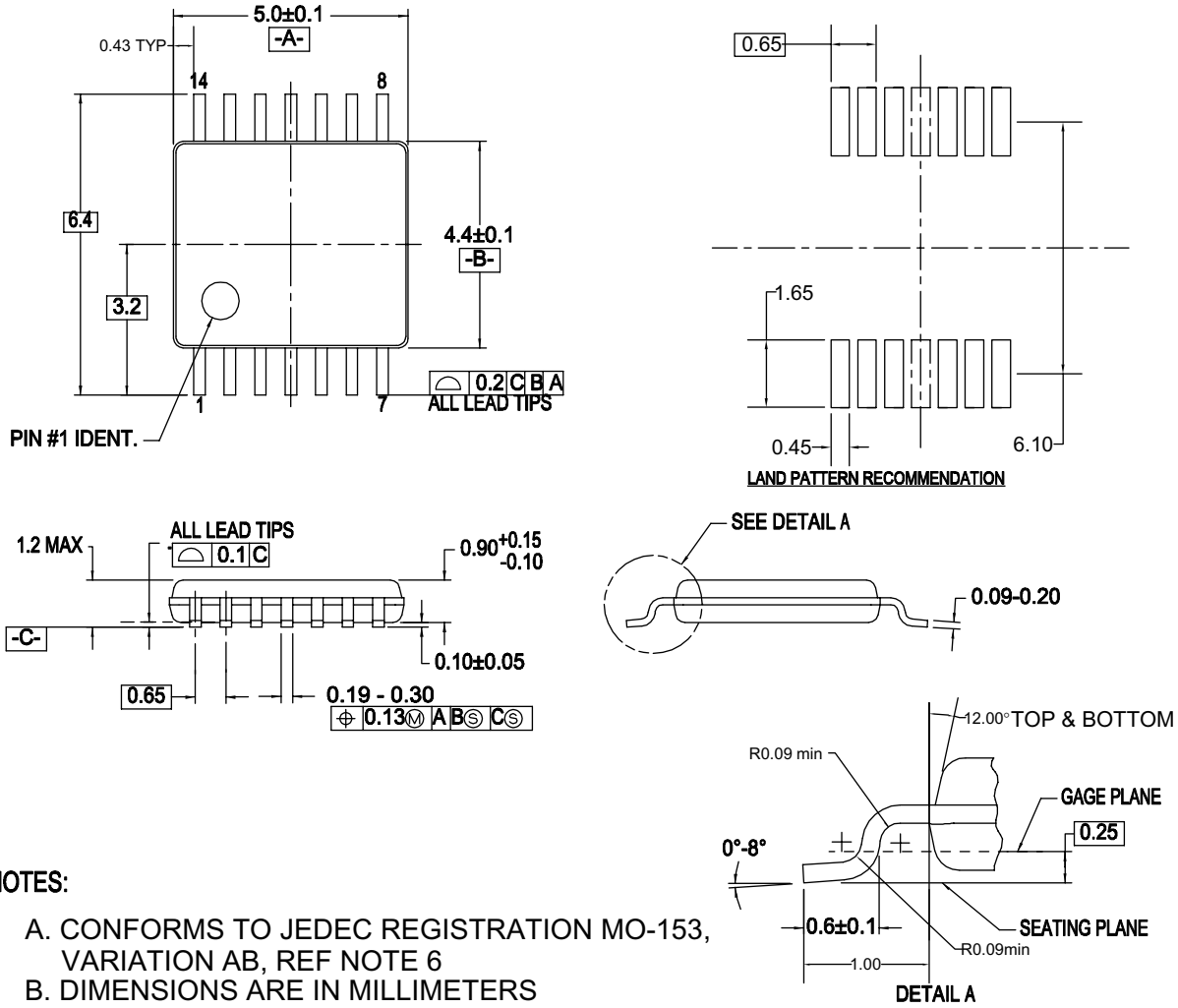
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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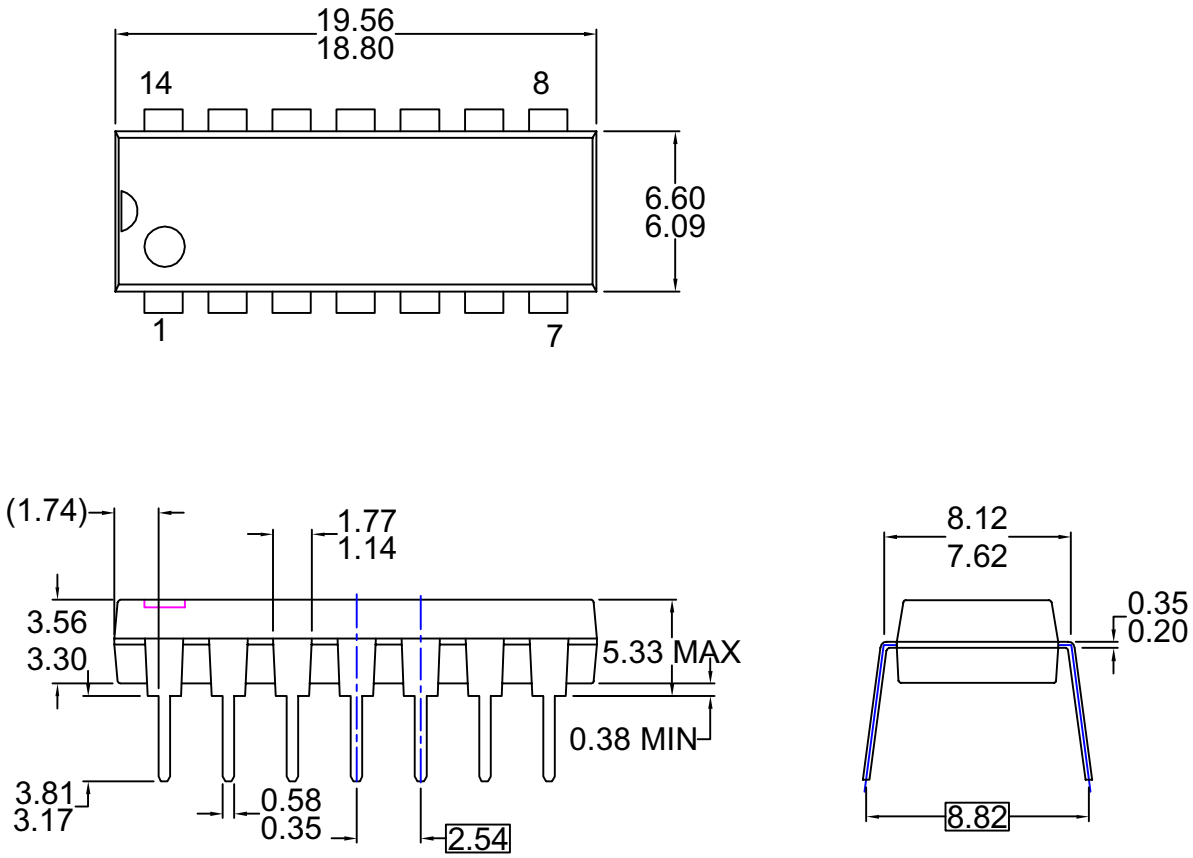
Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.
DIMENSIONS ARE EXCLUSIVE OF BURRS,

C) MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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