

N-Channel Power MOSFET (75A, 100Volts)

DESCRIPTION

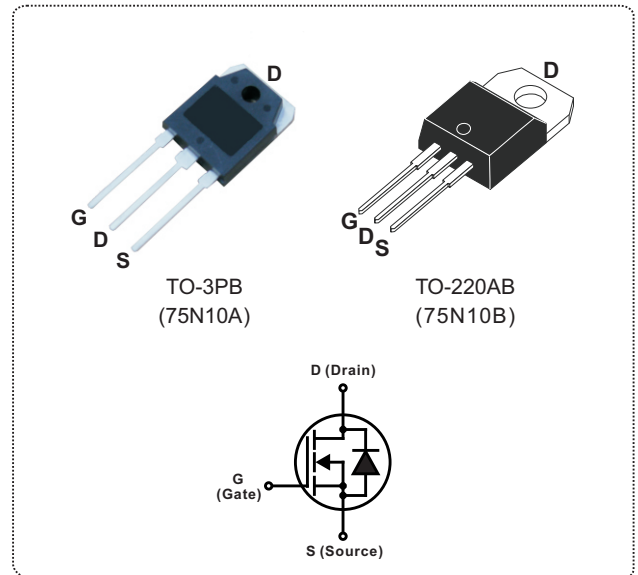
The Nell **75N10** is a three-terminal silicon device with current conduction capability of 75A, fast switching speed, low on-state resistance, breakdown voltage rating of 100V, and max. threshold voltage of 5 volts.

They are designed as an extremely efficient and reliable device for use in a wide variety of applications.

These transistors can be operated directly from integrated circuits.

FEATURES

- $R_{DS(ON)} = 0.025\Omega @ V_{GS} = 10V$
- Ultra low gate charge(74nC typical)
- Low reverse transfer capacitance ($C_{RSS} = 275pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



PRODUCT SUMMARY

I_D (A)	75
I_D (A), Package Limited	75
V_{DSS} (V)	100
$R_{DS(ON)}$ (Ω)	0.025 @ $V_{GS} = 10V$
Q_G (nC) typical	74

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage	$T_J = 25^\circ C$ to $150^\circ C$	100	V
V_{DGR}	Drain to Gate voltage	$R_{GS} = 1M\Omega$	100	
V_{GS}	Gate to Source voltage		± 20	
I_D	Continuous Drain Current	$T_C = 25^\circ C$	75	A
		$T_C = 100^\circ C$	50	
I_{DM}	Pulsed Drain current(Note 1)		200	
I_{AR}	Avalanche current(Note 1)		50	
E_{AR}	Repetitive avalanche energy(Note 1)		30	mJ
E_{AS}	Single pulse avalanche energy(Note 3)	$I_{AS} = 50A, L = 0.8mH$	1000	
dv/dt	Peak diode recovery dv/dt(Note 4)		10	V/ns
P_D	Total power dissipation	$T_C = 25^\circ C$	300	W
	Linear derating factor above $T_C = 25^\circ C$		1.90	
T_J	Operation junction temperature		-55 to 150	$^\circ C/W$ $^\circ C$
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N-m)

Note: 1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

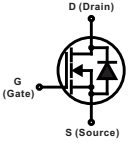
2. Repetitive rating: pulse width limited by junction temperature.

3. $L = 0.8mH, I_{AS} \leq 50A, R_G = 25\Omega, T_J \leq 150^\circ C$.

4. $I_{SD} \leq 50A, di/dt \leq 100A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J = 150^\circ C$.

THERMAL RESISTANCE						
SYMBOL	PARAMETER		Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case				0.42	°C/W
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-220AB			62	
		TO-3PB			40	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
OFF CHARACTERISTICS						
$V_{(BR)DSS}$	Drain to source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	100			V
$V_{(BR)DSS}/T_J$	Breakdown voltage temperature coefficient	$I_D = 1mA$, referenced to 25°C		0.105		V/°C
I_{DSS}	Drain to source leakage current	$V_{DS}=100V, V_{GS}=0V$ $T_C = 25^\circ\text{C}$			25	μA
		$V_{DS}=80V, V_{GS}=0V$ $T_C = 125^\circ\text{C}$			250	
I_{GSS}	Gate to source forward leakage current	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -20V, V_{DS} = 0V$			-100	
ON CHARACTERISTICS						
$R_{DS(ON)}$	Static drain to source on-state resistance	$V_{GS} = 10V, I_D = 37.5A$ (Note 1)		21	25	mΩ
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2.5		5.0	V
g_{fS}	Forward transconductance	$V_{DS}=10V, I_D=37.5A$	20	28		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		2250		μF
C_{OSS}	Output capacitance			890		
C_{RSS}	Reverse transfer capacitance			275		
SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 50V, I_D = 75A, R_G = 10\Omega, V_{GS} = 10V$ (Note 1)		27		ns
t_r	Rise time			53		
$t_{d(OFF)}$	Turn-off delay time			66		
t_f	Fall time			45		
Q_G	Total gate charge	$V_{DS} = 50V, V_{GS} = 10V, I_D = 37.5A$		74		nC
Q_{GS}	Gate to source charge			18		
Q_{GD}	Gate to drain charge (Miller charge)			40		
L_D	Internal drain inductance	Between lead, 6mm from package and center of die		4.5		μH
L_S	Internal source inductance			7.5		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	$I_{SD} = 75\text{A}, V_{GS} = 0\text{V}$			1.5	V
$I_S(I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			75	A
I_{SM}	Pulsed source current				200	
t_{rr}	Reverse recovery time	$I_{SD} = 75\text{A}, V_{GS} = 0\text{V},$ $dI_F/dt = 100\text{A}/\mu\text{s}$		120		ns
Q_{rr}	Reverse recovery charge			1.4		μC
t_{ON}	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by $LS+LD$)				

Note: 1. Pulse test: Pulse width $\leq 400\mu\text{s}$, duty cycle $\leq 2\%$.

ORDERING INFORMATION SCHEME	
	75 N 10 A
Current rating, I_D 75 = 75A	
MOSFET series N = N-Channel	
Voltage rating, V_{DS} 10 = 100V	
Package type A = TO-220AB B = TO-3PB	

Fig.1 Output characteristics

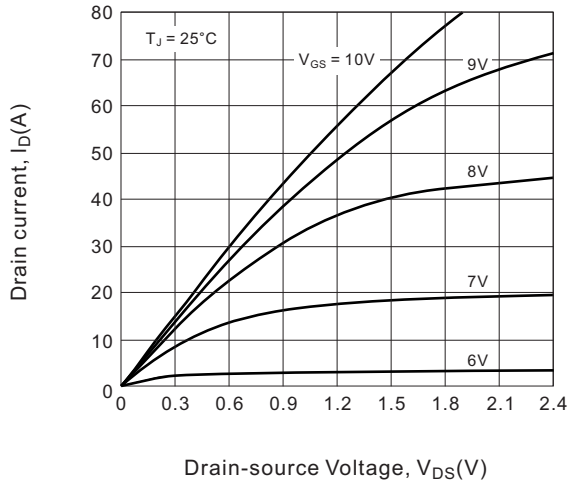


Fig.2 Extended output characteristics

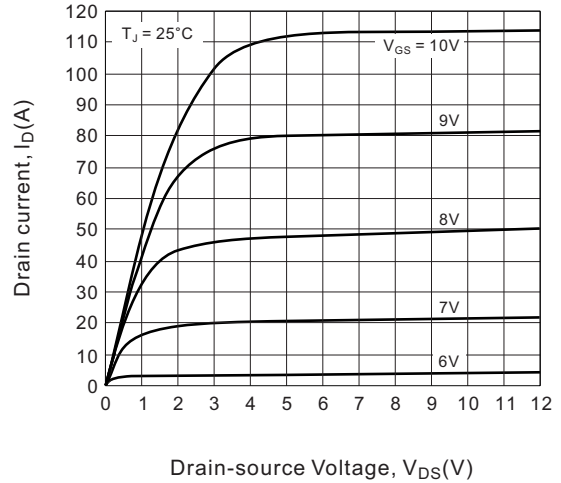


Fig.3 Output characteristics

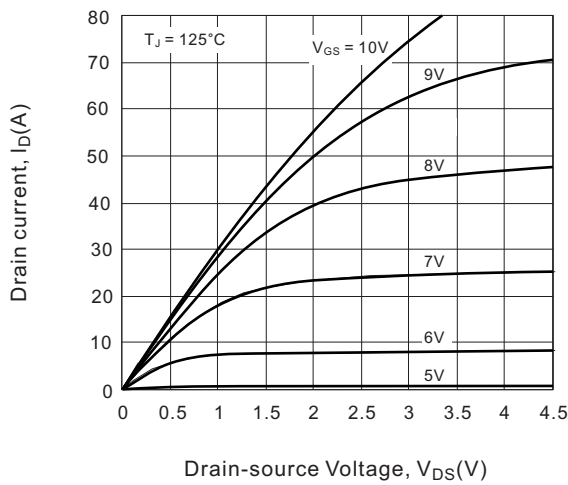


Fig.4 $R_{DS(on)}$ Normalized to 0.5 I_D value vs. Junction temperature

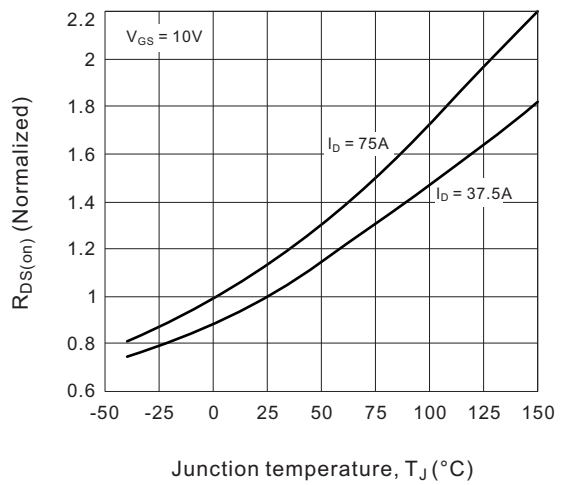


Fig.5 $R_{DS(on)}$ Normalized to 0.5 I_D value vs. Drain current

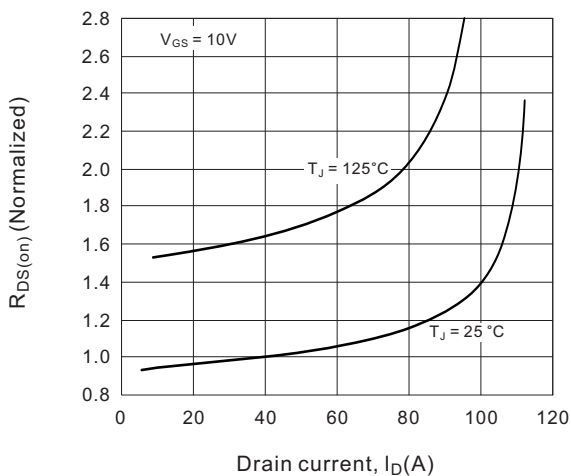


Fig.6 Maximum drain current vs. Case temperature

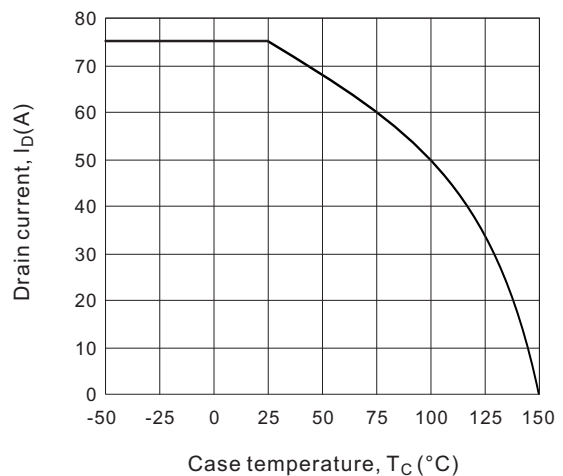


Fig.7 Typical transfer characteristics

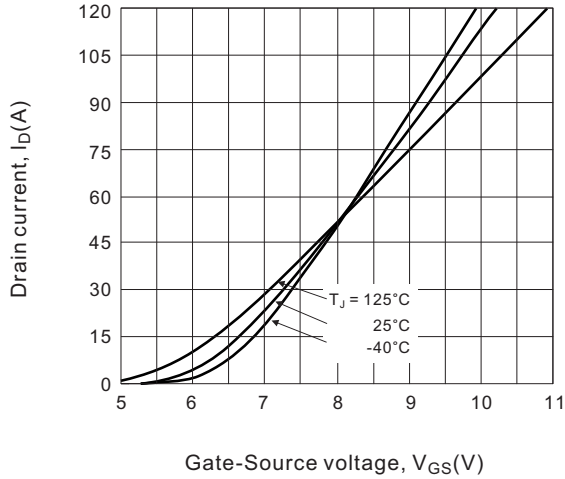


Fig.8 Forward transconductance

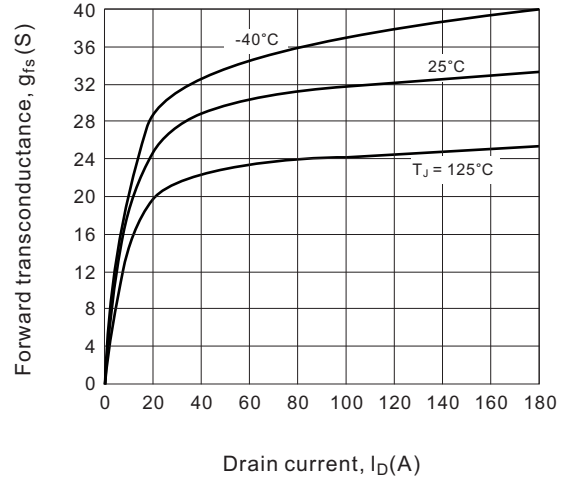


Fig.9 Typical source to drain diode forward voltage

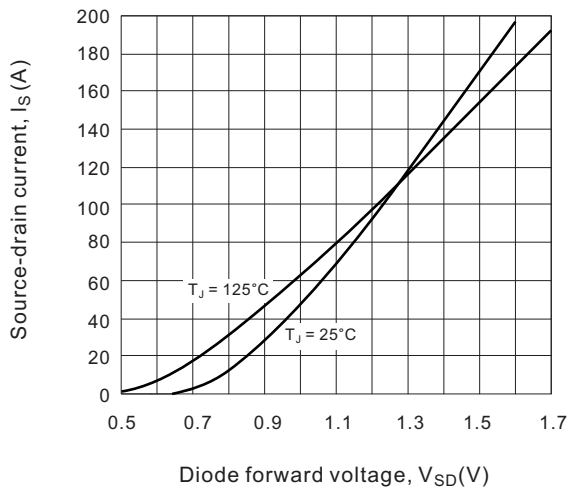


Fig.10 Gate charge characteristics

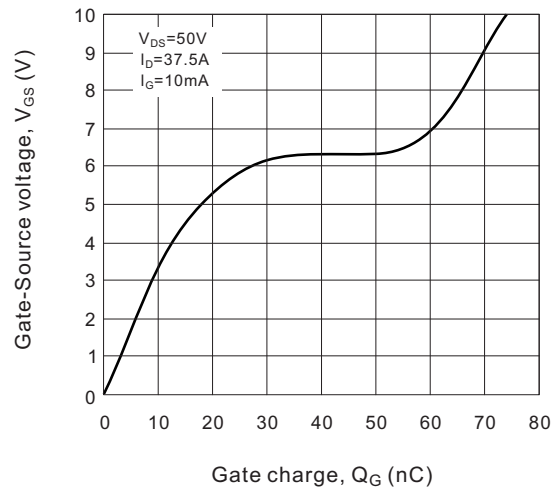


Fig.11 Typical capacitance vs. drain-Source voltage

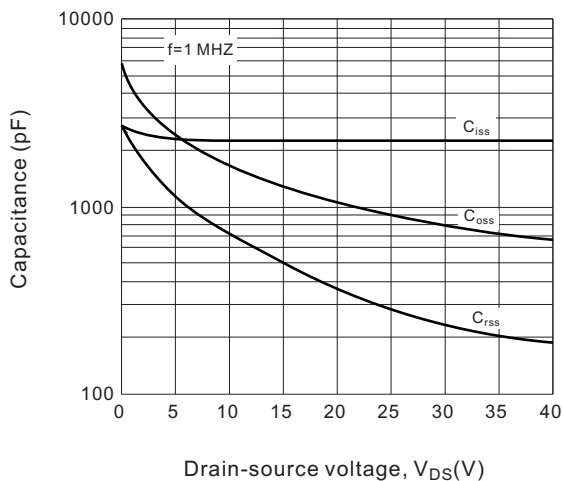


Fig.12 Maximum safe operating area

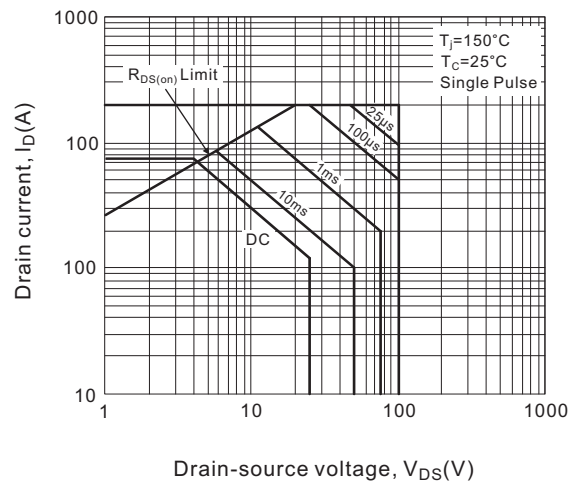


Fig.13 Maximum transient thermal Resistance

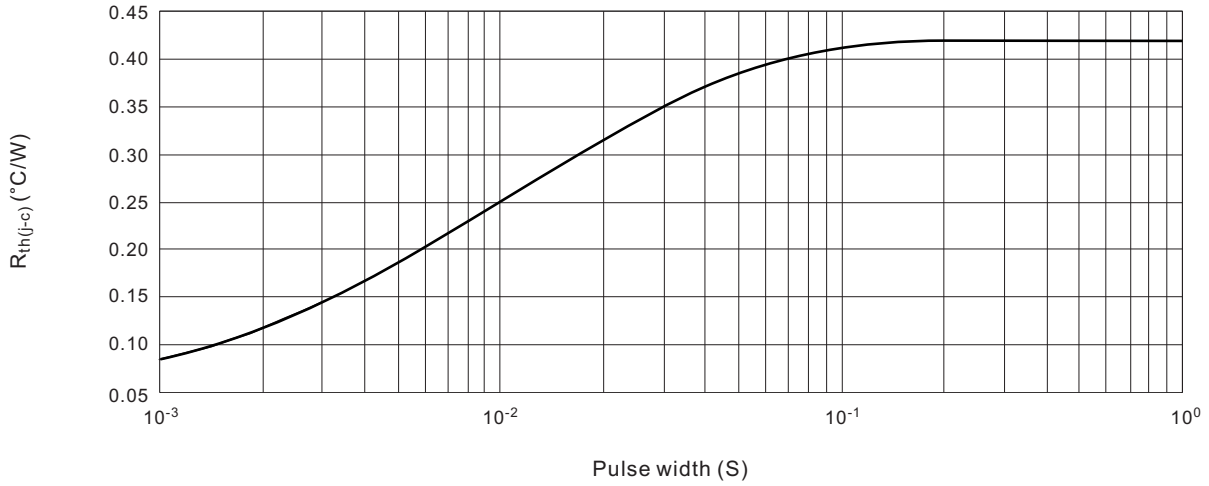


Fig.14a. Switching time test circuit

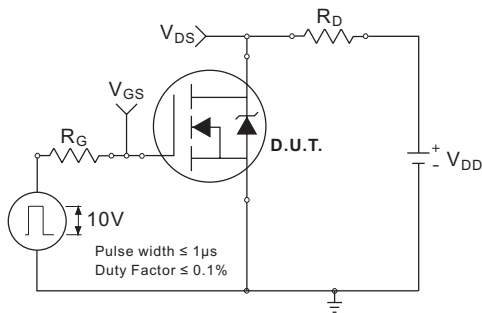


Fig.14b. Switching time waveforms

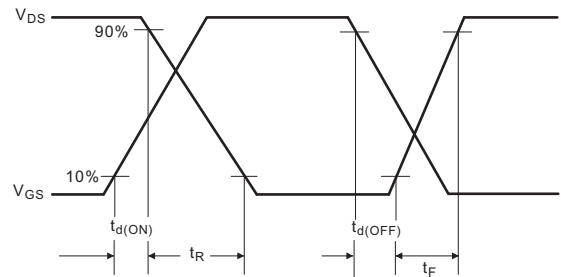


Fig.15a. Unclamped Inductive test circuit

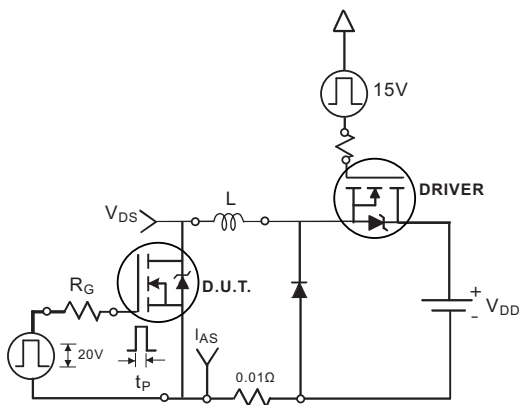


Fig.15b. Unclamped Inductive waveforms

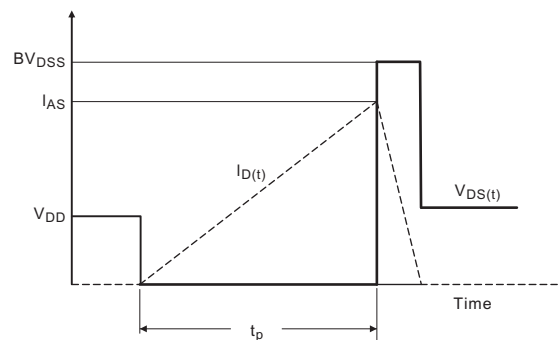


Fig.16a. Basic gate charge waveform

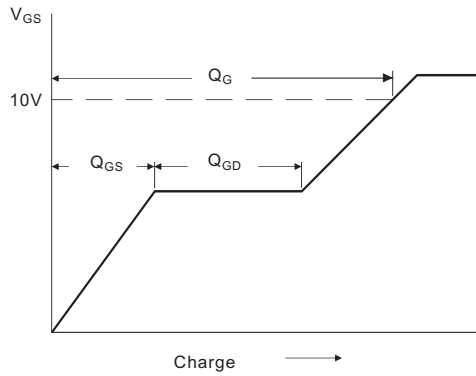


Fig.16b. Gate charge test circuit

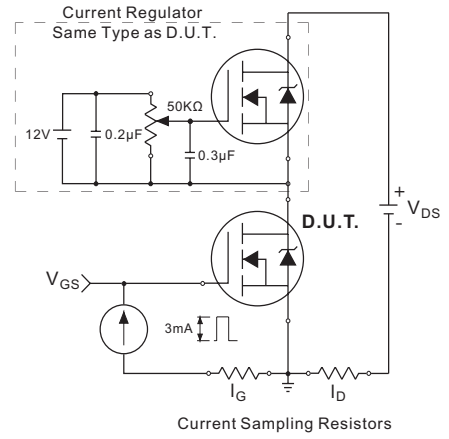
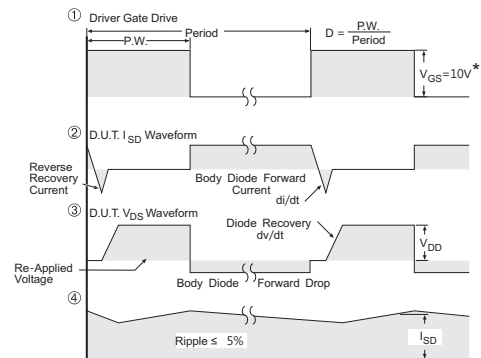
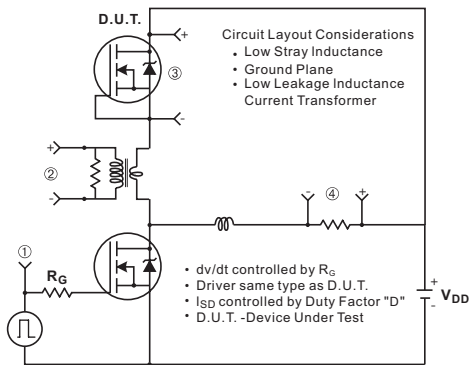
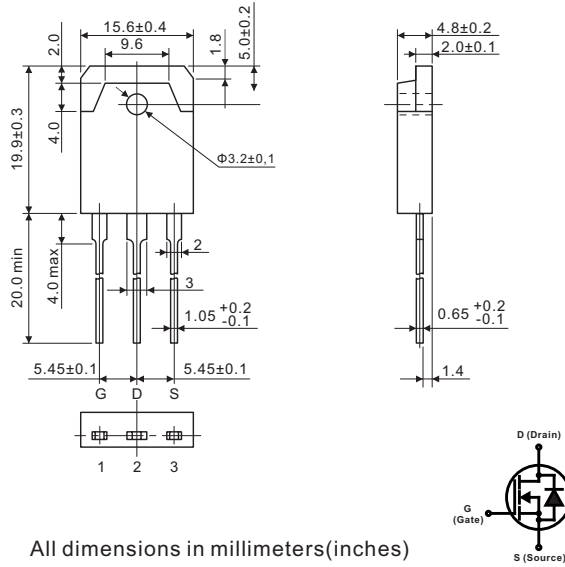


Fig.17 Peak diode recovery dv/dt test circuit for N-Channel MOSFET



* $V_{GS} = 5V$ for Logic Level Devices

TO-3PB



TO-220AB

