Bowmar/White Technology

128K x 8 BIT PROGRAMMABLE EEPROM 8090

PIN DIAGRAM

```
A14  [ 1        56 ] Vcc
A12  [ 2        55 ] WE
A7   [ 3        54 ] A13
A6   [ 4        53 ] A8
A5   [ 5        52 ] A9
A4   [ 6        51 ] A11
A3   [ 7        50 ] OE
A2   [ 8        49 ] A10
A1   [ 9        48 ] CE
A0   [ 10       47 ] I/O7
I/O0 [ 11       46 ] I/O6
I/O1 [ 12       45 ] I/O5
I/O2 [ 13       44 ] I/O4
Vss  [ 14       43 ] I/O3
A15  [ 15       42 ] A16
NC   [ 16       41 ] NC
NC   [ 17       40 ] NC
NC   [ 18       39 ] NC
NC   [ 19       38 ] NC
NC   [ 20       37 ] NC
NC   [ 21       36 ] NC
NC   [ 22       35 ] NC
NC   [ 23       34 ] NC
NC   [ 24       33 ] NC
NC   [ 25       32 ] NC
NC   [ 26       31 ] NC
NC   [ 27       30 ] NC
NC   [ 28       29 ] NC
```
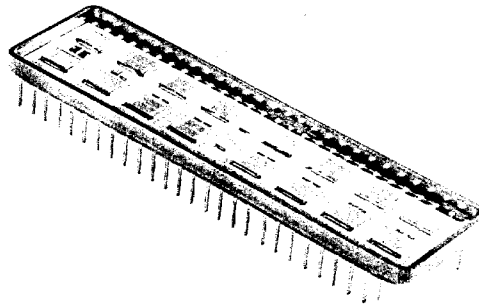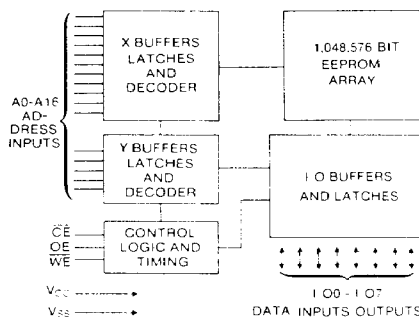
FEATURES

- **Voltage: +5.0V and Gnd**
- **Operating Temperature: -55° to +200°C**
- **Operating Current: 10mA (Typ)**
- **Standby Current: 1.0mA (Typ)**
- **Programming Temp: -55° to +180°C**
- **Access Time: 250nS**

BLOCK DIAGRAM

A0-A16 ADDRESS INPUTS → X BUFFERS LATCHES AND DECODER → 1,048,576 BIT EEPROM ARRAY; Y BUFFERS LATCHES AND DECODER; I/O BUFFERS AND LATCHES; CE OE WE → CONTROL LOGIC AND TIMING; Vcc; Vss; I/O0 - I/O7 DATA INPUTS OUTPUTS

DESCRIPTION

The Bowmar/White Technology 8090 is a low-power, high-performance 128K x 8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features, with data retention and readability to +200°C; and programmability to +180°C.

The 8090 is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write," the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes a method for detecting the end of a write cycle, DATA polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 250nS at low power dissipation. When the chip is deselected, the standby current is less than 1.0mA.

EEPROM Characteristics

Sym	Parameter (At 125°C)	Min	Typ	Max	Units
I_{li}	Input Load Current			50	μA
I_{lo}	Output Leakage Current			50	μA
I_{sb}	V_{cc} Standby Current $\overline{CE} = V_{cc}$			175	μA
I_{cc}	V_{cc} Active Current f = 5MHz			10.2	mA
V_{il}	Input Low Voltage	-0.1		0.8	V
V_{ih}	Input High Voltage	2.0		$V_{cc}+1$	V
V_{ol}	Output Low Voltage			.45	V
V_{oh}	Output High Voltage	2.4			V
C_{in}	Capacitance		110	150	pF
C_{out}	Capacitance		180	250	pF
	Access Time at 125°C			150	nS
	Access Time at 200°C			250	nS
	Endurance	10000 Write Cycles			
	Data Retention	10 Years			

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
L	L	H	Read	D_OUT	Active
L	H	L	Write	D_IN	Active
H	X	X	Standby/Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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DEVICE OPERATION

READ The 8090 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE Writing data into the 8090 is similar to writing into a static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Write cycle is 1mS max.

DATA POLLING The 8090 also utilizes $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the compliment of that data for I/O7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION Inadvertent writes to the device are protected against in the following ways: (a) Vcc sense—if Vcc is below 3.8V, the write function is inhibited; (b) Vcc power on delay—once Vcc has reached 3.8V, the device will automatically time out 5mS before allowing a byte write; (c) Write Inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

TIMING DIAGRAMS

All times are maximums unless otherwise specified.

READ CYCLE

WRITE CYCLE
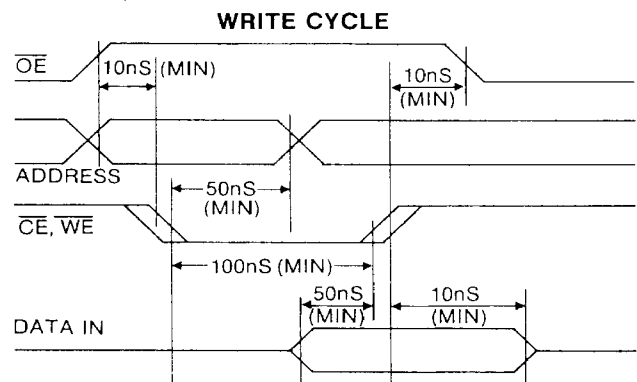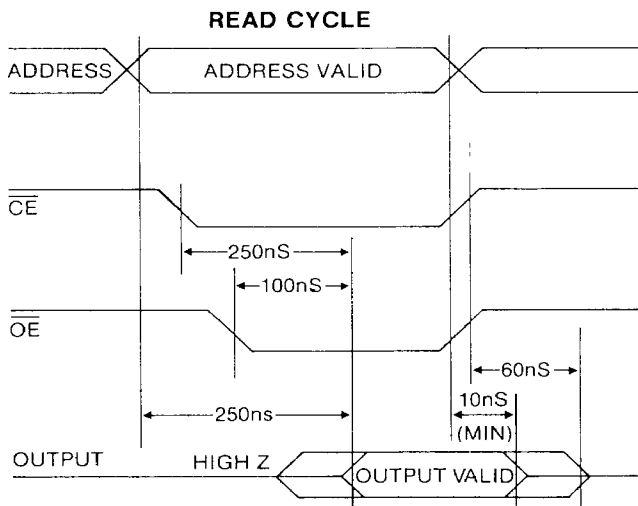
CASE OUTLINE
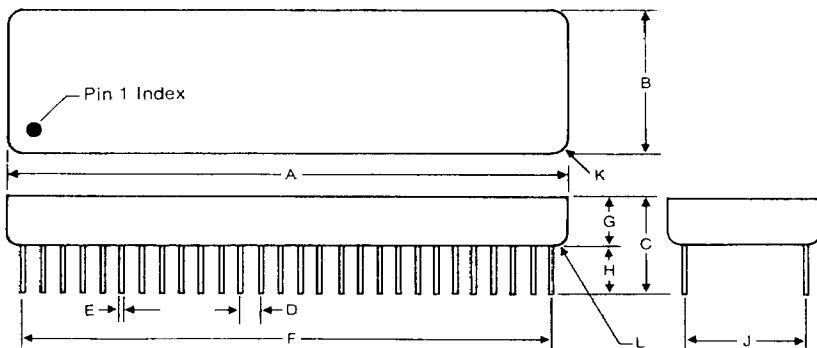
DIM	INCHES		MILLIMETERS	
	MIN	**MAX**	**MIN**	**MAX**
A	2.870	2.880	72.90	73.15
B	0.770	0.780	19.56	19.81
C	0.495	0.535	12.57	13.59
D	0.100 TYP		2.54 TYP	
E	0.018 DIA ±0.002		0.46 DIA ±0.05	
F	2.695	2.705	68.45	68.71
G	0.255	0.275	6.48	6.99
H	0.240	0.260	6.10	6.60
J	0.595	0.605	15.11	15.38
K	0.086 R ±0.003		2.18 R ±0.08	
L	0.060 R MAX TYP		1.52 R MAX TYP	

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