

8x931AA/8x931HA UNIVERSAL SERIAL BUS PERIPHERAL CONTROLLERS

- **8x931AA Hubless USB Peripheral Controller**
- **On-chip USB Transceivers**
- **On-chip Phase-locked loop**
- **FIFO Data Buffers**
 - **Two Pairs of 8-byte Transmit and Receive FIFOs**
 - **One Pair of 16-byte Transmit and Receive FIFOs**
 - **Supports Isochronous and Non-isochronous Data**
- **Automatic FIFO Management**
- **Three USB Interrupt Vectors**
 - **Endpoint Transmit/Receive Done**
 - **Start of Frame**
 - **Global Suspend/Resume/USB Reset**
- **Regulated 3V Output for Root Port Pullup Resistor**
- **On-chip ROM Options**
 - **0 or 8 Kbytes**
- **256 bytes On-chip Data RAM**
- **Four Input/Output Ports**
- **MCS[®] 51 UART**
- **Three 16-bit Timer/Counters**
- **Keyboard Control Interface**
- **Four Dedicated LED Driver Outputs**
- **6- or 12-MHz Crystal Operation**
 - **Low Clock Mode (3MHz)**
- **8x931HA Includes all 8x931AA Features**
- **8x931HA USB Hub has One Internal Downstream, and Four External Downstream Ports**
 - **Universal Serial Bus Specification 1.0 Compliant**
 - **Serves as both USB Hub and USB Embedded Function (Internal Port)**
- **USB Hub**
 - **Connectivity Management**
 - **Downstream Device Connect/Disconnect Detection**
 - **Power Management, Including Suspend and Resume**
 - **Bus Fault Detection and Recovery**
 - **Full and Low Speed Downstream Device Support**
- **Hub Endpoint Done Interrupt**
- **Output Pin for Port Power Switching**
- **Input Pin for Overcurrent Detection**
- **Hub FIFO Data Buffers**
 - **One Pair of 8-byte Transmit and Receive FIFOs**
 - **One 1-byte Transmit Register**
- **Embedded Function FIFO Data Buffers**
 - **Same as the 8x931AA**
- **12-MHz Crystal Operation**
 - **Low Clock Mode (3MHz)**

The 8x931AA and 8x931HA USB peripheral controllers are based on the MCS[®]51 microcontroller. They consist of standard 8XC51Fx peripherals plus a USB module. The 8x931HA USB module provides both USB hub and USB embedded function capabilities. The 8x931HA supports USB hub functionality, embedded function, suspend/resume modes, isochronous/non-isochronous transfers, and is USB rev 1.0 specification compliant. The USB module contains one internal and 4 external downstream ports and integrates the USB transceivers, serial bus interface engine (SIE), hub interface unit (HIU), function interface unit (FIU), and transmit/receive FIFOs. The 8x931AA is a hubless USB peripheral controller which contains the same feature set as the 8x931HA hub controller except for the hub module. The 8x931AA/HA uses the standard instruction set of the MCS 51 architecture.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel retains the right to make changes to specifications and product descriptions at any time, without notice.

*Third-party brands and names are the property of their respective owners.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
Literature Sales
PO Box 5937
Denver, CO 80217-9808
or call 1-800-548-4725

CONTENTS

| | | |
|-------|--|----|
| 1.0 | About This Document..... | 1 |
| 1.1 | Additional Information Sources | 1 |
| 1.2 | Electronic Information..... | 1 |
| 1.3 | Product Summary..... | 2 |
| 2.0 | Nomenclature Overview..... | 4 |
| 3.0 | Pinout..... | 6 |
| 3.0.1 | 8x931HA 68-pin PLCC Package | 6 |
| 3.0.2 | 8x931AA 68-pin PLCC Package | 7 |
| 4.0 | Signals | 10 |
| 5.0 | Electrical Characteristics..... | 13 |
| 5.1 | Operating Frequencies..... | 14 |
| 5.2 | DC Characteristics..... | 15 |
| 5.3 | Explanation of Timing Symbols..... | 17 |
| 5.4 | System Bus AC Characteristics..... | 18 |
| 5.4.1 | System Bus Timing Diagrams | 19 |
| 5.5 | AC Characteristics — Synchronous Mode 0..... | 21 |
| 5.6 | External Clock Drive..... | 22 |
| 5.7 | Testing Waveforms | 23 |
| 6.0 | Thermal Characteristics | 24 |
| 7.0 | Design Considerations..... | 24 |
| 7.1 | Low Clock Mode Frequency..... | 24 |
| 7.2 | Setting RXFFRC Bit Clears Only the Oldest Packet in the FIFO | 24 |
| 7.3 | Series Resistor Requirement for Impedance Matching..... | 24 |
| 7.4 | Pullup Resistor Requirement for 8x931AA/HA devices..... | 24 |
| 7.5 | Powerdown Mode Cannot Be Invoked Before USB Suspend..... | 24 |
| 7.6 | Unused Downstream Ports..... | 24 |
| 7.7 | ECAP Usage to Supply 3.0 to 3.6 Volts for 1.5K Ohm Pullup..... | 24 |
| 8.0 | 8x931AA/HA Errata..... | 25 |
| 9.0 | Datasheet Revision History..... | 25 |

Figures

| | | |
|-----|--|----|
| 1. | 8x931 Functional Block Diagram..... | 2 |
| 2. | 8x931HA USB Module Block Diagram..... | 3 |
| 3. | Product Nomenclature | 4 |
| 4. | 8x931HA 68-pin PLCC Package..... | 6 |
| 5. | 8x931AA 68-pin PLCC Package | 7 |
| 6. | 8x931AA/HA External Program Memory Read | 19 |
| 7. | 8x931AA/HA External Data Memory Read | 20 |
| 8. | 8x931AA/HA External Data Memory Write..... | 20 |
| 9. | Serial Port Waveform — Synchronous Mode 0..... | 21 |
| 10. | External Clock Drive Waveforms..... | 22 |
| 11. | AC Testing Input, Output Waveforms..... | 23 |
| 12. | Float Waveforms | 23 |

Tables

| | | |
|-----|--|----|
| 1. | Related Documentation..... | 1 |
| 2. | Electronic Information | 1 |
| 3. | Description of Product Nomenclature..... | 4 |
| 5. | 8x931AA Proliferation Options | 5 |
| 4. | 8x931HA Proliferation Options..... | 5 |
| 6. | 68-pin PLCC Pin Assignment..... | 8 |
| 7. | 68-pin PLCC Signal Assignments Arranged by Functional Category | 9 |
| 8. | Signal Description | 10 |
| 9. | 8x931AA/8x931HA Supply Voltages | 13 |
| 10. | 8x931HA Operating Frequency..... | 14 |
| 11. | 8x931AA Operating Frequencies | 14 |
| 12. | DC Characteristics at Operating Conditions..... | 15 |
| 13. | AC Timing Symbol Definitions..... | 17 |
| 14. | External Bus Characteristics | 18 |
| 15. | Serial Port Timing — Synchronous Mode 0 | 21 |
| 16. | External Clock Drive..... | 22 |
| 17. | Thermal Characteristics | 24 |
| 18. | Vcc and Typical ECAP Voltages | 25 |

1.0 ABOUT THIS DOCUMENT

This data sheet contains advance information about Intel's 8x931AA and 8x931HA Universal Serial Bus peripheral controllers, based on the MCS@51 peripheral controller, which includes a functional overview, mechanical data, targeted electrical specifications (simulated), and bus functional waveforms. A detailed functional description, other than parametric performance, is published in the 8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual (273102-001).

1.1 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
PO Box 5937
Denver, CO 80217-9808

or call 1-800-548-4725

1.2 Electronic Information

We offer a variety of technical and product information through the World Wide Web (see Table 2 for URL) and through FaxBack service which is an on-demand publishing system that sends documents to your fax machine. You can get product announcements, change notifications, product literature, device characteristics, design recommendations, and quality and reliability information 24 hours a day, 7 days a week. Just dial the telephone number and respond to the system prompts.

Table 1. Related Documentation

| Document Title | Order/Contact |
|--|-------------------------|
| <i>8x931AA, 8x931HA Universal Serial Bus Peripheral Controller User's Manual</i> | Intel Order #273102-001 |
| <i>Universal Serial Bus Specification, Rev. 1.0</i> | Intel Order #272904 |

Table 2. Electronic Information

| Document Title | Order/Contact |
|---|---|
| Intel's World-Wide Web (WWW) Location: | http://www.intel.com/design/usb/ |
| Customer Support (US and Canada): | 800-628-8686 |
| FaxBack Service: | |
| <i>US and Canada</i> | 800-628-2283 |
| <i>Europe</i> | +44(0)793-496646 |
| <i>worldwide</i> | 916-356-3105 |
| Application Bulletin Board Service: | |
| <i>up to 14.4-Kbaud line, worldwide</i> | 916-356-3600 |
| <i>dedicated 2400-baud line, worldwide</i> | 916-356-7209 |
| <i>Europe</i> | +44(0)793-496340 |

1.3 Product Summary

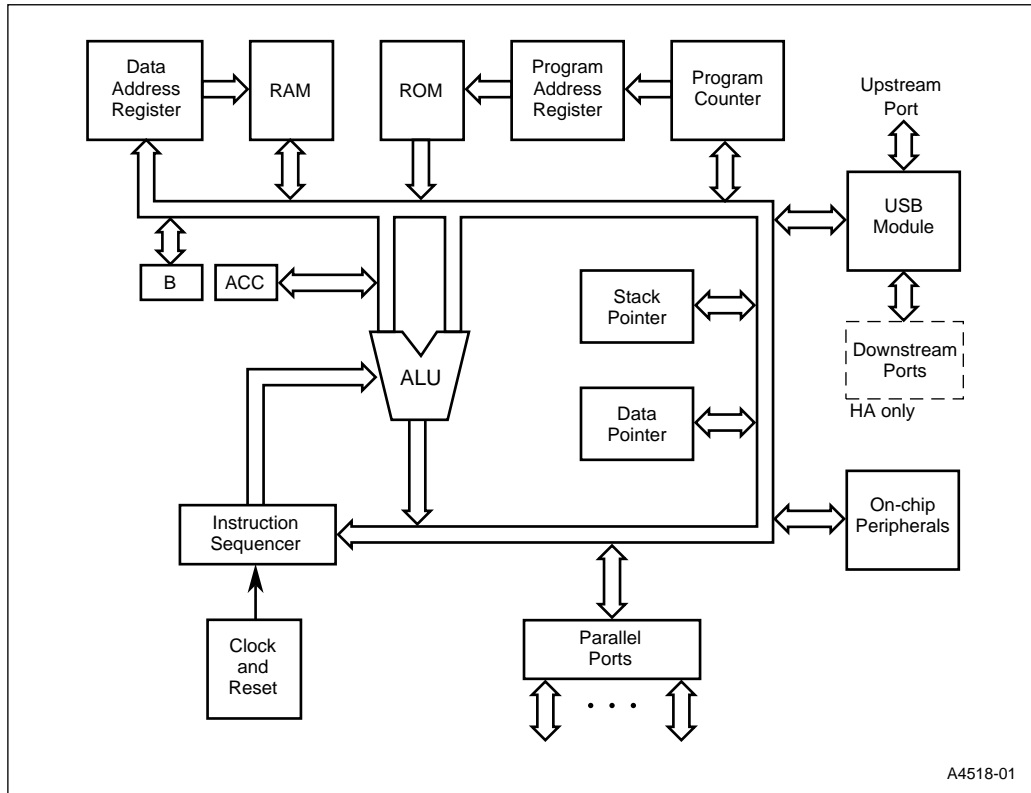
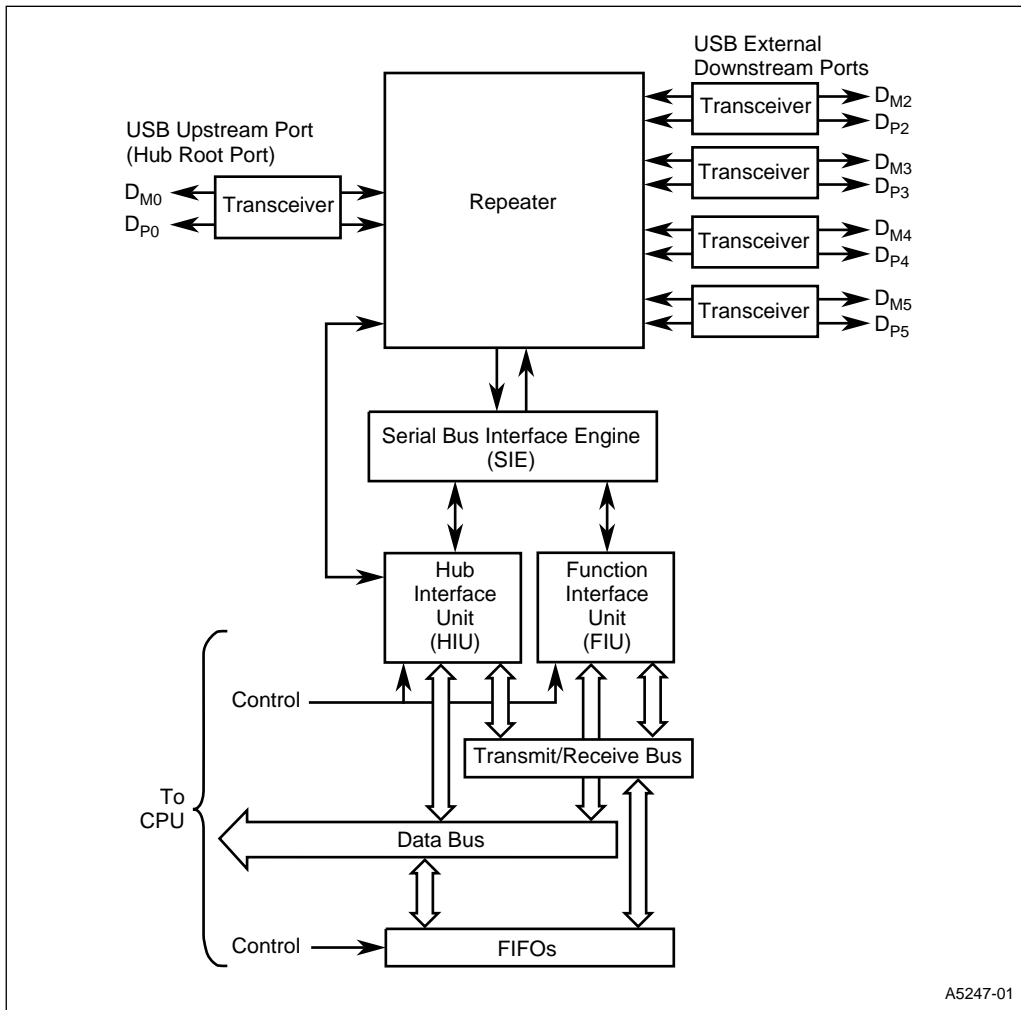


Figure 1. 8x931 Functional Block Diagram



A5247-01

Figure 2. 8x931HA USB Module Block Diagram

2.0 NOMENCLATURE OVERVIEW

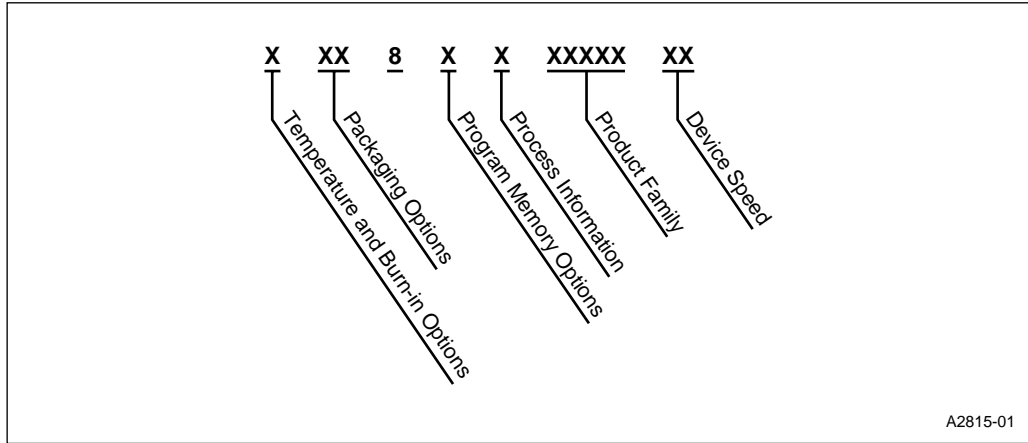


Figure 3. Product Nomenclature

Table 3. Description of Product Nomenclature

| Parameter | Options | Description |
|---------------------------------|---------|---|
| Temperature and Burn-in | no mark | Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in |
| Packaging Options | N | Plastic Leaded Chip Carrier (PLCC) |
| Program Memory Options | 0 | Without ROM |
| | 3 | With ROM |
| Process and Voltage Information | no mark | CHMOS |
| Product Family | 931Hx | Advanced 8-bit microcontroller architecture with on-chip Universal Serial Bus Hub and Function capability. Indicates ROM size, RAM size, and quantity of external downstream ports (see Table 4). |
| | 931Ax | Advanced 8-bit microcontroller architecture with on-chip Universal Serial Bus Function capability. Indicates ROM size, RAM size, and quantity of external downstream ports (see Table 5). |
| Device Speed | no mark | 6 or 12 MHz crystal (8x931AA), 12MHz crystal (8x931HA) |

Table 4. 8x931HA Proliferation Options

| Part Name | ROM Size | RAM Size | Package |
|------------------|-----------------|-----------------|----------------|
| N80931HA | 0 | 256 bytes | 68-pin PLCC |
| N83931HA | 8 Kbytes | 256 bytes | 68-pin PLCC |

Table 5. 8x931AA Proliferation Options

| Part Name | ROM Size | RAM Size | Package |
|------------------|-----------------|-----------------|----------------|
| N80931AA | 0 | 256 bytes | 68-pin PLCC |
| N83931AA | 8 Kbytes | 256 bytes | 68-pin PLCC |

8x931AA, 8x931HA USB PERIPHERAL CONTROLLER

3.0 PINOUT

3.0.1 8x931HA 68-pin PLCC Package

Figure 4 illustrates a diagram of the 8x931HA PLCC package. Table 6 and Table 7 contain indexes of the pin arrangement. Table 8 contains the signal descriptions for all pins.

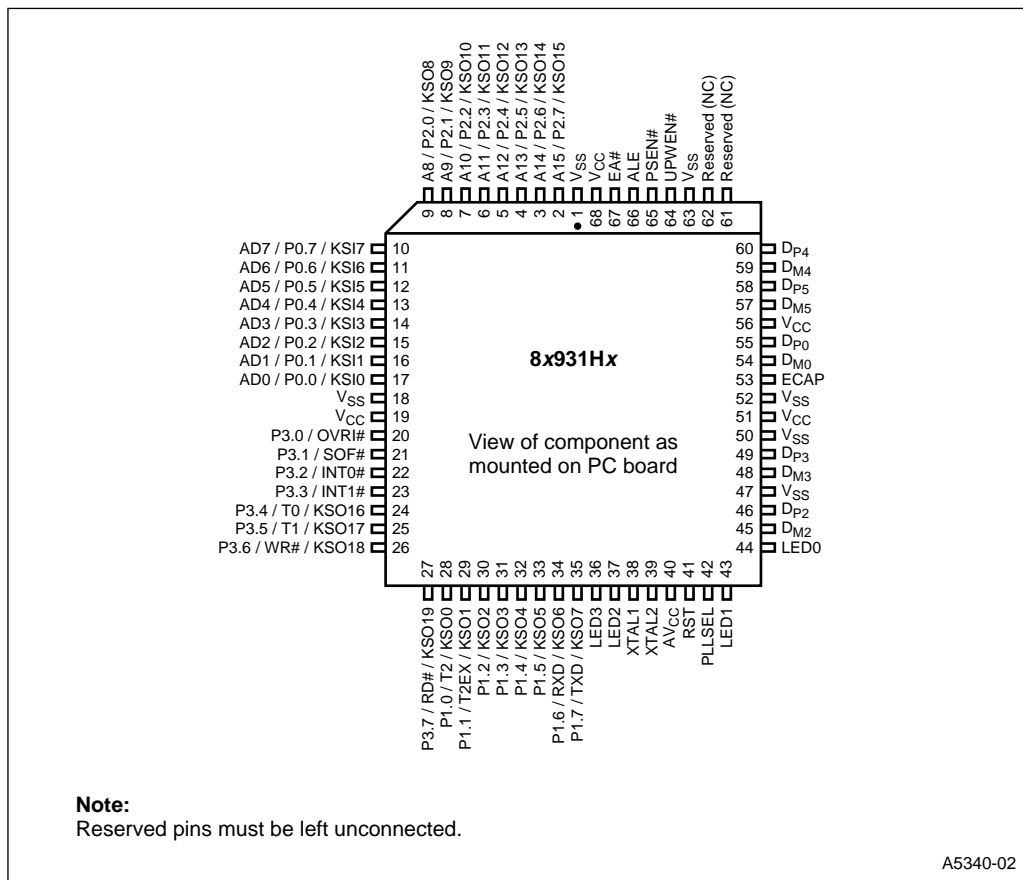


Figure 4. 8x931HA 68-pin PLCC Package

3.0.2 8x931AA 68-pin PLCC Package

Figure 5 illustrates a diagram of the 8x931AA PLCC package. Table 6 and Table 7 contain indexes of the pin arrangement. Table 8 contains the signal descriptions for all pins.

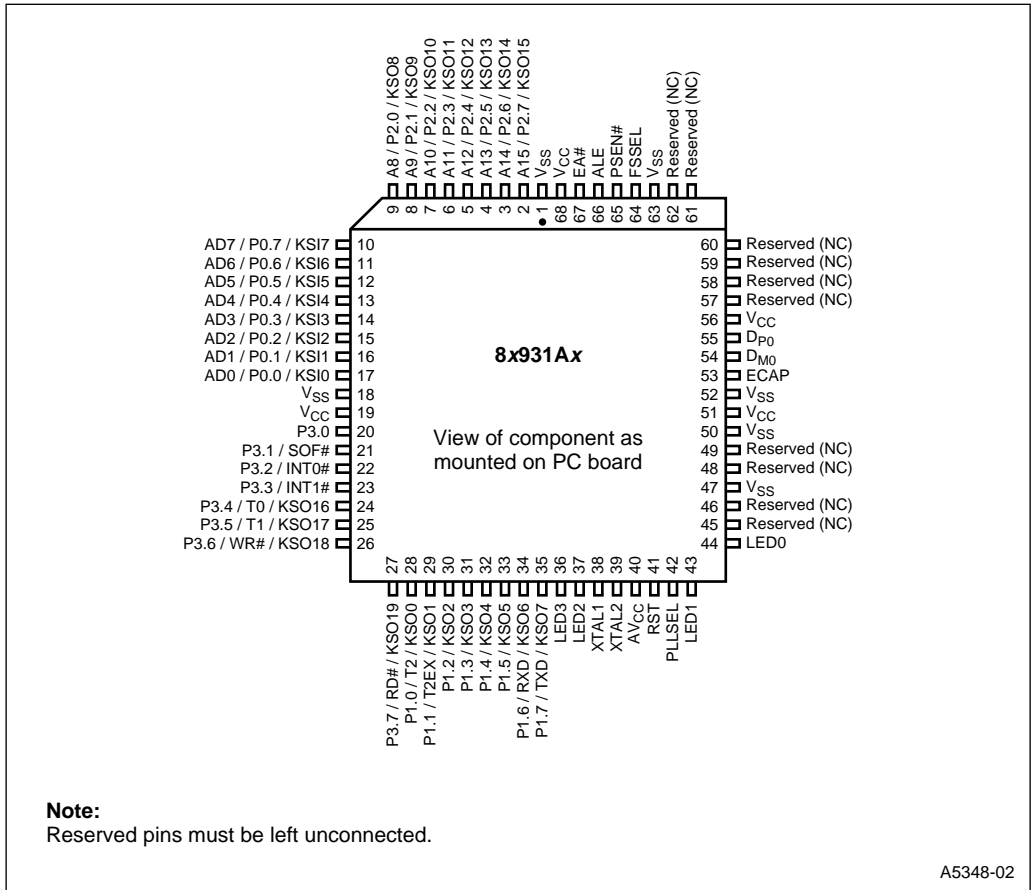

Figure 5. 8x931AA 68-pin PLCC Package

Table 6. 68-pin PLCC Pin Assignment

| Pin | Name | Pin | Name | Pin | Name |
|-----|---------------------------|-----|---|-----|---|
| 1 | V _{SS} | 24 | P3.4/T0/KSO16 | 47 | V _{SS} |
| 2 | A15/P2.7/KSO15 | 25 | P3.5/T1/KSO17 | 48 | Reserved [†] / D _{M3} ^{††} |
| 3 | A14/P2.6/KSO14 | 26 | P3.6/WR#/KSO18 | 49 | Reserved [†] / D _{P3} ^{††} |
| 4 | A13/P2.5/KSO13 | 27 | P3.7/RD#/KSO19 | 50 | V _{SS} |
| 5 | A12/P2.4/KSO12 | 28 | P1.0/T2/KSO0 | 51 | V _{CC} |
| 6 | A11/P2.3/KSO11 | 29 | P1.1/T2EX/KSO1 | 52 | V _{SS} |
| 7 | A10/P2.2/KSO10 | 30 | P1.2/KSO2 | 53 | ECAP |
| 8 | A9/P2.1/KSO9 | 31 | P1.3/KSO3 | 54 | D _{M0} |
| 9 | A8/P2.0/KSO8 | 32 | P1.4/KSO4 | 55 | D _{P0} |
| 10 | AD7/P0.7/KSI7 | 33 | P1.5/KSO5 | 56 | V _{CC} |
| 11 | AD6/P0.6/KSI6 | 34 | P1.6/KSO6/RXD | 57 | Reserved [†] / D _{M5} ^{††} |
| 12 | AD5/P0.5/KSI5 | 35 | P1.7/KSO7/TXD | 58 | Reserved [†] / D _{P5} ^{††} |
| 13 | AD4/P0.4/KSI4 | 36 | LED3 | 59 | Reserved [†] / D _{M4} ^{††} |
| 14 | AD3/P0.3/KSI3 | 37 | LED2 | 60 | Reserved [†] / D _{P4} ^{††} |
| 15 | AD2/P0.2/KSI2 | 38 | XTAL1 | 61 | Reserved (NC) |
| 16 | AD1/P0.1/KSI1 | 39 | XTAL2 | 62 | Reserved (NC) |
| 17 | AD0/P0.0/KSI0 | 40 | AV _{CC} | 63 | V _{SS} |
| 18 | V _{SS} | 41 | RST | 64 | FSSEL [†] / UPWEN# ^{††} |
| 19 | V _{CC} | 42 | PLLSEL | 65 | PSEN# |
| 20 | P3.0/ OVRI# ^{††} | 43 | LED1 | 66 | ALE |
| 21 | P3.1/SOF# | 44 | LED0 | 67 | EA# |
| 22 | P3.2/INT0# | 45 | Reserved [†] / D _{M2} ^{††} | 68 | V _{CC} |
| 23 | P3.3/INT1# | 46 | Reserved [†] / D _{P2} ^{††} | | |

[†] Specific to the 8x931AA

^{††} Specific to the 8x931HA

Table 7. 68-pin PLCC Signal Assignments Arranged by Functional Category

| Address & Data | | Input/Output | | USB | |
|----------------|-----|---------------------------|-----|---|-----|
| Name | Pin | Name | Pin | Name | Pin |
| A15/P2.7/KSO15 | 2 | P1.0/T2/KSO0 | 28 | PLLSEL | 42 |
| A14/P2.6/KSO14 | 3 | P1.1/T2EX/KSO1 | 29 | D _{M0} | 54 |
| A13/P2.5/KSO13 | 4 | P1.2/KSO2 | 30 | D _{P0} | 55 |
| A12/P2.4/KSO12 | 5 | P1.3/KSO3 | 31 | Reserved [†] / D _{M5} ^{††} | 57 |
| A11/P2.3/KSO11 | 6 | P1.4/KSO4 | 32 | Reserved [†] / D _{P5} ^{††} | 58 |
| A10/P2.2/KSO10 | 7 | P1.5/KSO5 | 33 | Reserved [†] / D _{M2} ^{††} | 45 |
| A9/P2.1/KSO9 | 8 | P1.6/KSO6 | 34 | Reserved [†] / D _{P2} ^{††} | 46 |
| A8/P2.0/KSO8 | 9 | P1.7/KSO7 | 35 | Reserved [†] / D _{M3} ^{††} | 48 |
| AD7/P0.7/KSI7 | 10 | P3.0/ OVRI# ^{††} | 20 | Reserved [†] / D _{P3} ^{††} | 49 |
| AD6/P0.6/KSI6 | 11 | P3.1/SOF# | 21 | ECAP | 53 |
| AD5/P0.5/KSI5 | 12 | P3.2/INT0# | 22 | Reserved [†] / D _{M4} ^{††} | 59 |
| AD4/P0.4/KSI4 | 13 | P3.3/INT1# | 23 | Reserved [†] / D _{P4} ^{††} | 60 |
| AD3/P0.3/KSI3 | 14 | P3.4/T0/KSO16 | 24 | FSSEL [†] /UPWEN# ^{††} | 64 |
| AD2/P0.2/KSI2 | 15 | P3.5/T1/KSO17 | 25 | OVRI# ^{††} | 20 |
| AD1/P0.1/KSI1 | 16 | P3.6/WR#/KSO18 | 26 | | |
| AD0/P0.0/KSI0 | 17 | P3.7/RD#/KSO19 | 27 | | |

| Processor Control | | Power & Ground | | Bus Control & Status | |
|-------------------|-----|------------------|------------------|----------------------|-----|
| Name | Pin | Name | Pin | Name | Pin |
| P3.2/INT0# | 22 | V _{CC} | 19,51,56,68 | P3.6/WR#/KSO18 | 26 |
| P3.3/INT1# | 23 | AV _{CC} | 40 | P3.7/RD#/KSO19 | 27 |
| RST | 41 | V _{SS} | 1,18,47,50,52,63 | PSEN# | 65 |
| XTAL1 | 38 | | | ALE | 66 |
| XTAL2 | 39 | | | EA# | 67 |

[†] Specific to the 8x931AA

^{††} Specific to the 8x931HA

4.0 SIGNALS
Table 8. Signal Description (Sheet 1 of 3)

| Signal Name | Type | Description | Alternate Function |
|--|------|---|--------------------|
| A15:8 | O | Address Lines. Upper byte of external memory address. | P2.7:0/KS08:15 |
| AD7:0 | I/O | Address/Data Lines. Lower byte of external memory address multiplexed with data | P0.7:0/KS10:7 |
| ALE | O | Address Latch Enable. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus. | — |
| AV _{CC} | PWR | Analog V_{CC}. A separate V _{CC} input for the phase-locked loop circuitry. | — |
| D _{M0} , D _{P0} | I/O | USB Port 0. Root port. Upstream port to the host PC. D _{P0} and D _{M0} are the differential data plus and data minus signals of USB port 0. These lines do not have internal pullup resistors. Provide an external 1.5 K Ω pullup resistor at D _{P0} so the device indicates to the host that it is a full-speed device; or provide an external 1.5 K Ω pullup resistor at D _{M0} so the device indicates to the host that it is a low-speed device. NOTE: D _{P0} low AND D _{M0} low signals an SE0 (USB reset), causing the 8x931 to stay in reset. | — |
| D _{M2} , D _{P2} D _{M3} , D _{P3} D _{M4} , D _{P4} D _{M5} , D _{P5} | I/O | USB External Downstream Ports 2, 3, 4, 5. These pins are the differential data plus and data minus lines for the four USB external downstream ports. These lines do not have internal pulldown resistors. Provide an external 15 K Ω pulldown resistor at each of these pins. See “Design Considerations” on page 24. | — |
| EA# | I | External Access. Directs program memory accesses to on-chip or off-chip code memory. For EA# strapped to ground, all program memory accesses are off-chip. For EA# strapped to V _{CC} , program accesses on-chip ROM if the address is within the range of the on-chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM, EA# must be strapped to ground. | — |
| ECAP | I | External Capacitor. Connect a 1 μ F or larger capacitor between this pin and V _{SS} to ensure proper operation of the differential line drivers. May be used to supply 3.0v to 3.6v for 1.5K pullup resistor connected to USB Port 0. See “Design Considerations” on page 24. | — |
| FSSEL | | Full Speed Select. Applies to the 8x931AA only. If this pin is high, full speed USB data rate is selected (12Mbps). If pin is low, low speed USB data rate is selected (1.5 Mbps). Refer to Table 11. | — |

Table 8. Signal Description (Sheet 2 of 3)

| Signal Name | Type | Description | Alternate Function |
|--|------|--|---|
| INT1:0# | I | External Interrupts 0 and 1. These inputs set the IE1:0 interrupt flags in the TCON register. Bits IT1:0 in TCON select the triggering method: edge-triggered (high-to-low) or level triggered (active low). INT1:0 also serves as external run control for timer1:0 when selected by GATE1:0# in TCON. | P3.3:2 |
| KS17:0 | I | Keyboard Scan Input. Schmitt-trigger inputs with firmware-enabled internal pullup resistors used for the input side of the keyboard scan matrix. | AD7:0/P0.7:0 |
| KSO19 KSO18 KSO17:16 KSO15:8 KSO7:0 | O | Keyboard Scan Output. Quasi-bidirectional ports with weak internal pullup resistors used for the output side of the keyboard scan matrix. | P3.7/RD# P3.6/WR# P3.5:4/T1:0 A15:8/P2.7:0 P1.7:0 |
| LED3:0 | O | LED Drivers. Designed to drive LEDs connected directly to V_{CC} . The current each driver is capable of sinking is given as V_{OL2} in the datasheet. | — |
| OVR1# | I | Overcurrent Sense. Sense input to indicate an overcurrent condition on an external down-stream port. Active low with an internal pullup. | P3.0 |
| P0.7:0 | I/O | Port 0. Eight-bit, open-drain, bidirectional I/O port. Port 0 pins have Schmitt trigger inputs. | AD7:0/KS17:0 |
| P1.7:0 | I/O | Port 1. Eight-bit quasi-bidirectional I/O port with internal pullups. | KSO7:0 |
| P2.7:0 | I/O | Port 2. Eight-bit quasi-bidirectional I/O port with internal pullups. | A15:8/KSO15:8 |
| P3.0 P3.1 P3.2 P3.3 P3.4 P3.5 P3.6 P3.7 | I/O | Port 3. Eight-bit quasi-bidirectional I/O port with internal pullups. | OVR1# SOF# INT0# INT1# T0/KSO16 T1/KSO17 WR#/KSO18 RD#/KSO19 |
| PLLSEL | I | Phase-locked Loop Select. For normal operation using the 8x931HA, connect PLLSEL to logic high. PLLSEL = 0 is used for factory test only. (See Table 10). For 8x931AA operation, see Table 11. | — |
| PSEN# | O | Program Store Enable. Read signal output. Asserted for read accesses to external program memory. | — |
| RD# | O | Read. Read signal output. Asserted for read accesses to external data memory. | P3.7/KSO19 |
| RXD | I/O | Receive Serial Data. RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3. | P1.6 |

Table 8. Signal Description (Sheet 3 of 3)

| Signal Name | Type | Description | Alternate Function |
|-------------|------|---|--------------------|
| RST | I | Reset. Reset input to the chip. Holding this pin high for two machine cycles while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor which allows the device to be reset by connecting a capacitor between this pin and V_{CC} . Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation. | — |
| SOF# | O | Start of Frame. Start of frame pulse. Active low. Asserted for 8 states when frame timer is locked to USB frame timing and SOF token or artificial SOF is detected. | P3.1 |
| T1:0 | I | Timer 1:0 External Clock Input. When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count. | P3.5:4/KSO17:16 |
| T2 | I/O | Timer 2 Clock Input/Output. For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output. | P1.0 |
| T2EX | I | Timer 2 External Input. In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down. | P1.1 |
| TXD | O | Transmit Serial Data. TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3. | P1.7 |
| UPWEN# | O | USB Power Enable. A low signal on this pin applies power to the external downstream ports. | — |
| V_{CC} | PWR | Supply Voltage. Connect this pin to the +5v supply voltage. Use a 0.1 μ f decoupling capacitor for each V_{CC} pin. | — |
| V_{SS} | GND | Circuit Ground. Connect this pin to ground. | — |
| WR# | O | Write. Write signal output to external memory. | P3.6/KSO19 |
| XTAL1 | I | Oscillator Amplifier Input. When implementing the on-chip oscillator, connect the external crystal or ceramic resonator across XTAL1 and XTAL2. If an external clock source is used, connect it to this pin. | — |
| XTAL2 | O | Oscillator Amplifier Output. When implementing the on-chip oscillator, connect the external crystal or ceramic resonator across XTAL1 and XTAL2. If an external oscillator is used, leave XTAL2 unconnected. | — |

5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[†]

| | |
|--|------------------|
| Ambient Temperature Under Bias..... | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pins to V _{SS} | -0.5 V to +6.5 V |
| I _{OL} per I/O Pin..... | 15 mA |
| Power Dissipation (1) | 1.5 W |

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

OPERATING CONDITIONS[†]

| | |
|--|------------------|
| T _A (Ambient Temperature Under Bias): | |
| Commercial..... | -0°C to +70°C |
| V _{CC} (Digital Supply Voltage) | 4.40 V to 5.25 V |
| V _{SS} | 0 V |
| AV _{CC} (Analog Supply Voltage) | 4.40 V to 5.25 V |
| F _{OSC} | 12 MHz |

[†] **WARNING:** *Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.*

NOTE:

- Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

Table 9. 8x931AA/8x931HA Supply Voltages

| Parameter | Condition | Symbol | Min | Max |
|----------------|-----------|---|--------------------|-------|
| Supply Voltage | | 8x931HA V _{CC} /V _{bus} | 4.40V | 5.25V |
| | | 8x931AA V _{CC} /V _{bus} | 4.15V [†] | 5.25V |

[†]For bus-powered device, voltage droop during hot plug may cause the supply voltage to drop to 4V worst case. The functionality of the device is supported at this voltage.

5.1 Operating Frequencies
Table 10. 8x931HA Operating Frequency

| PLLSEL | XTAL1 Frequency (F_{osc}) | USB Rate (1) | Internal Frequency (F_{CLK}) (2) | XTAL1 Clocks per State ($T_{osc}/state$) (3) | Comments |
|--------|-------------------------------|----------------------|--------------------------------------|--|----------|
| 0 (4) | – | – | – | – | – |
| 1 | 12 MHz | 12 Mbps (Full Speed) | 6 MHz (3) | 2 | PLL On |

NOTES:

1. The sampling rate is 4 times the USB rate.
2. The internal frequency, $F_{CLK} = 1/T_{CLK}$, is the clock signal distributed to the CPU and the on-chip peripherals.
3. Following device reset, the CPU and on-chip peripherals operate in low-clock mode ($F_{CLK} = 3$ MHz) until the LC bit in the PCON register is cleared. In low clock mode, there are four T_{OSC} periods per state. Low-clock mode does not affect the USB rate.
4. PLLSEL = 0 is used during factory test only.

Table 11. 8x931AA Operating Frequencies

| PLLSEL Pin | FSSEL Pin | LC Bit (1) | XTAL1 Frequency (MHz) | USB Rate (FS/LS) (2) | Core Frequency F_{CLK} (Mhz) | Comment |
|------------|-----------|------------|-----------------------|----------------------|--------------------------------|---------|
| 0 | 0 | 0 | 6 | LS | 3 | PLL Off |
| 0 | 0 | 1 | 6 | LS | 3 | PLL Off |
| 1 | 0 | 0 | 12 | LS | 6 | PLL Off |
| 1 | 0 | 1 | 12 | LS | 3 | PLL Off |
| 1 | 1 | 0 | 12 | FS | 6 | PLL On |
| 1 | 1 | 1 | 12 | FS | 3 | PLL On |

NOTES:

1. Reset and power up routines set the LC bit in PCON to put the 8x931AA in low-clock mode (core frequency = 3 MHz) for lower I_{CC} prior to device enumeration. Following completion of device enumeration, firmware should clear the LC bit to exit the low-clock mode. The user may switch the core frequency back and forth at any time, as needed.
2. USB rates: Low speed = 1.5 Mbps; Full speed = 12 Mbps. The USB sample rate is 4X the USB rate.

5.2 DC Characteristics

Table 12. DC Characteristics at Operating Conditions

| Symbol | Parameter | Min | Typical (1) | Max | Units | Test Conditions |
|-----------|--|--|-------------|--------------------|---------|---|
| V_{IL} | Input Low Voltage (except EA#) | -0.5 | | $0.2 V_{CC} - 0.1$ | V | |
| V_{IL1} | Input Low Voltage (EA#) | 0 | | $0.2 V_{CC} - 0.3$ | V | |
| V_{IH} | Input High Voltage (except XTAL1, RST) | $0.2 V_{CC} + 0.9$ | | $V_{CC} + 0.5$ | V | |
| V_{IH1} | Input High Voltage (XTAL1, RST) | $0.7 V_{CC}$ | | $V_{CC} + 0.5$ | V | |
| V_{OL} | Output Low Voltage (port 1, 2, 3) (2) | | | 0.3 0.45 1.0 | V | $I_{OL} = 100 \mu A$ $I_{OL} = 1.6 \text{ mA}$ $I_{OL} = 3.5 \text{ mA}$ |
| V_{OL1} | Output Low Voltage (port 0, ALE, PSEN#, SOF#) (2) | | | 0.3 0.45 1.0 | V | $I_{OL} = 200 \mu A$ $I_{OL} = 3.2 \text{ mA}$ $I_{OL} = 7.0 \text{ mA}$ |
| V_{OL2} | Output Low Voltage (LED 0, 1, 2, 3) | | | 2.0 3.0 | V | $I_{OL} = 6 \text{ mA}$ $I_{OL} = 22 \text{ mA}$ |
| V_{OH} | Output High Voltage (port 1, 2, 3, ALE, PSEN#, SOF#) (3) | $V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$ | | | V | $I_{OH} = -10 \mu A$ $I_{OH} = -30 \mu A$ $I_{OH} = -60 \mu A$ |
| V_{OH1} | Output High Voltage (port 0 in external address space) (3) | $V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$ | | | V | $I_{OH} = -200 \mu A$ $I_{OH} = -3.2 \text{ mA}$ $I_{OH} = -7.0 \text{ mA}$ |
| I_{IL} | Logical 0 Input Current (port 1,2,3) | | | -50 | μA | $V_{IN} = 0.45 \text{ V}$ |
| I_{LI} | Input Leakage Current (port 0) | | | ± 10 | μA | $V_{IN} = V_{IL}$ or V_{IH} |

NOTE:

- Typical values are obtained using $V_{CC} = 5.0V$, $T_A = 25^\circ C$ and are not guaranteed.
- Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
- Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN to drop below the V_{CC} specification when the address lines are stabilizing.

Table 12. DC Characteristics at Operating Conditions (Continued)

| Symbol | Parameter | Min | Typical (1) | Max | Units | Test Conditions |
|------------|---|-----|-------------|------|-----------|--|
| I_{TL} | Logical 1-to-0 Transition Current (Port 1, 2,3) | | | -650 | μA | $V_{IN} = 2.0 V$ |
| R_{RST} | RST Pulldown Resistor | 40 | | 100 | $K\Omega$ | |
| C_{IO} | Pin Capacitance | | 10 | | μF | $F_{OSC} = 12 MHz$ $T_A = 25^\circ C$ |
| I_{PD} | Powerdown Current USB suspend | | 145 | 175 | μA | |
| I_{DL} | Idle Mode I_{CC} | | | 40 | mA | $F_{CLK} = 6 MHz$ |
| | | | | 30 | | $F_{CLK} = 3 MHz$ |
| I_{CC} | Active I_{CC} | | | 70 | mA | $F_{CLK} = 6 MHz$ |
| | | | | 50 | | $F_{CLK} = 3 MHz$ |
| U_{ZDRV} | USB Drivers Output | 10 | | 25 | $K\Omega$ | |

NOTE:

1. Typical values are obtained using $V_{CC} = 5.0V$, $T_A = 25^\circ C$ and are not guaranteed.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN to drop below the V_{CC} specification when the address lines are stabilizing.

5.3 Explanation of Timing Symbols

Table 13 defines the timing symbols used in Tables 14 through 16 and the associated timing diagrams. They have the form T_{XYY} , where the character pairs represent a signal and its condition. Timing symbols represent the time between two signal / condition points.

Table 13. AC Timing Symbol Definitions

| Symbol | Definition |
|--------|------------------------------|
| A | Address: A15:8, A7:0 |
| C | External Clock (XTAL1) |
| D | Data In: D7:0 |
| L | ALE: Address Latch Enable |
| P | Program Store Enable (PSEN#) |
| Q | Data Out: D7:0 |
| R | Read: RD# |
| W | Write: WR# |

| Character | Condition |
|-----------|--------------------------|
| H | High |
| L | Low |
| V | Valid, Setup |
| X | No Longer Valid, Hold |
| Z | Floating (low impedance) |

5.4 System Bus AC Characteristics

Test Conditions: $F_{OSC} = 12$ MHz. Rise and fall times = 10 ns. Capacitive loading on ALE, PSEN#, and port P0 = 100 pF. Capacitive loading on all other outputs = 80 pF.

Table 14. External Bus Characteristics

| Symbol | Parameter | $F_{OSC} = 12$ MHz, $F_{CLK} = 6$ MHz | | Variable F_{CLK} | | Units |
|----------------------|------------------------------------|--|-----|--------------------|--------------------|-------|
| | | Min | Max | Min | Max | |
| F_{OSC} | XTAL1 Frequency | 12 ± 0.25% | | | | MHz |
| T_{CLK} | 1/ $F_{CLK} = 1$ /CPU Frequency | 166.67 (Typical) | | | | ns |
| T_{LHLL} | ALE Pulse Width | 127 | | $T_{CLK} - 40$ | | ns |
| T_{AVLL} | Address Valid to ALE Low | 43 | | $0.5T_{CLK} - 40$ | | ns |
| T_{LLAX} | Address Hold after ALE Low | 53 | | $0.5T_{CLK} - 30$ | | ns |
| T_{PLAZ} | PSEN# Low to Address Float | | 10 | | 10 | ns |
| T_{LLV} | ALE Low to Instruction In Valid | | 259 | | $2T_{CLK} - 75$ | ns |
| T_{LLPL} | ALE Low to PSEN# Low | 53 | | $0.5T_{CLK} - 30$ | | ns |
| T_{PLPH} | PSEN# Pulse Width | 205 | | $1.5T_{CLK} - 45$ | | ns |
| T_{PLIV} | PSEN# Low to Instruction In Valid | | 77 | | $T_{CLK} - 90$ | ns |
| T_{PHIX} | Instruction Hold after PSEN# High | 0 | | 0 | | ns |
| T_{PHIZ} | Instruction Float after PSEN# High | | 63 | | $0.5T_{CLK} - 20$ | ns |
| T_{AVIV} | Address Valid to Instruction Valid | | 312 | | $2.5T_{CLK} - 105$ | ns |
| T_{LLRL}, T_{LLWL} | ALE Low to RD# or WR# Low | 200 | 300 | $1.5T_{CLK} - 50$ | $1.5T_{CLK} + 50$ | ns |
| T_{RLRH}, T_{WLWH} | RD# and WR# Pulse Width | 400 | | $3T_{CLK} - 100$ | | ns |
| T_{LLDV} | ALE Low to Data In Valid | | 578 | | $4T_{CLK} - 90$ | ns |
| T_{RLDV} | RD# Low to Data In Valid | | 322 | | $2.5T_{CLK} - 95$ | ns |
| T_{RLAZ} | RD# Low to Address Float | | 0 | | 0 | ns |
| T_{RHDX} | Data Hold After RD# High | 0 | | 0 | | ns |
| T_{RHDZ} | Data Float After RD# High | | 23 | | $0.5T_{CLK} - 60$ | ns |
| T_{AVRL}, T_{AVWL} | Address Valid to RD# or WR# Low | 244 | | $2T_{CLK} - 90$ | | ns |

Table 14. External Bus Characteristics (Continued)

| Symbol | Parameter | $F_{OSC} = 12\text{ MHz},$ $F_{CLK} = 6\text{ MHz}$ | | Variable F_{CLK} | | Units |
|----------------------|--------------------------------|--|-----|--------------------|-------------------|-------|
| | | Min | Max | Min | Max | |
| T_{AVDV} | Address Valid to Data In Valid | | 661 | | $4.5T_{CLK} - 90$ | ns |
| T_{RHLH}, T_{WHLH} | RD# or WR# High to ALE High | 43 | 123 | $0.5T_{CLK} - 40$ | $0.5T_{CLK} + 40$ | ns |
| T_{QVWX} | Data Valid to WR# Transition | 48 | | $0.5T_{CLK} - 35$ | | ns |
| T_{QVWH} | Data Valid to WR# High | 514 | | $3.5T_{CLK} - 70$ | | ns |
| T_{WHQX} | Data Hold After WR# High | 43 | | $0.5T_{CLK} - 40$ | | ns |

5.4.1 System Bus Timing Diagrams

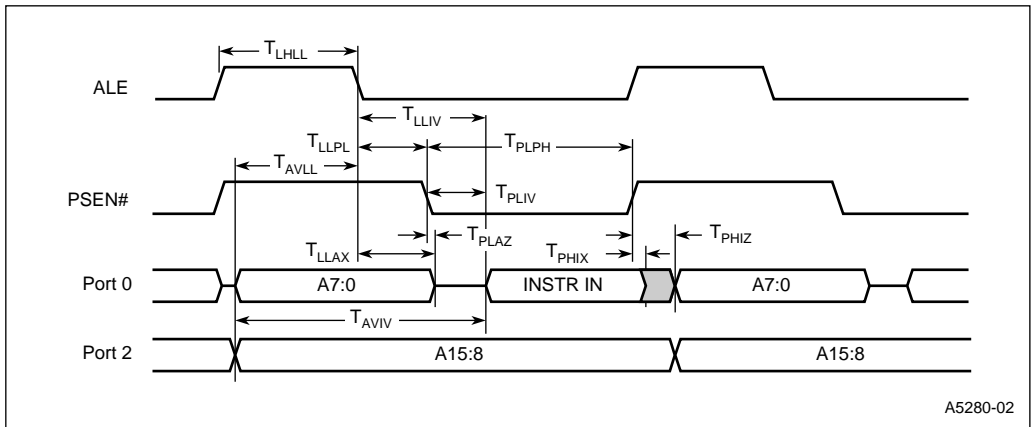


Figure 6. 8x931AA/HA External Program Memory Read

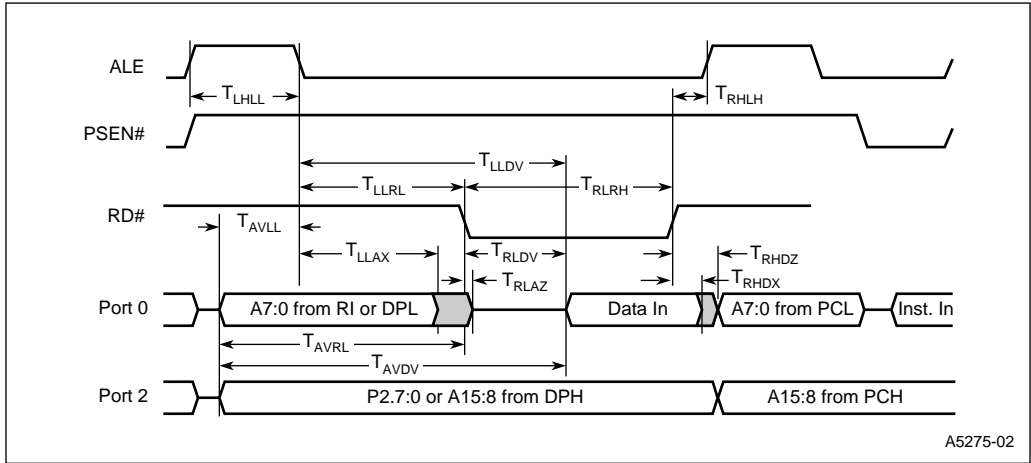


Figure 7. 8x931AA/HA External Data Memory Read

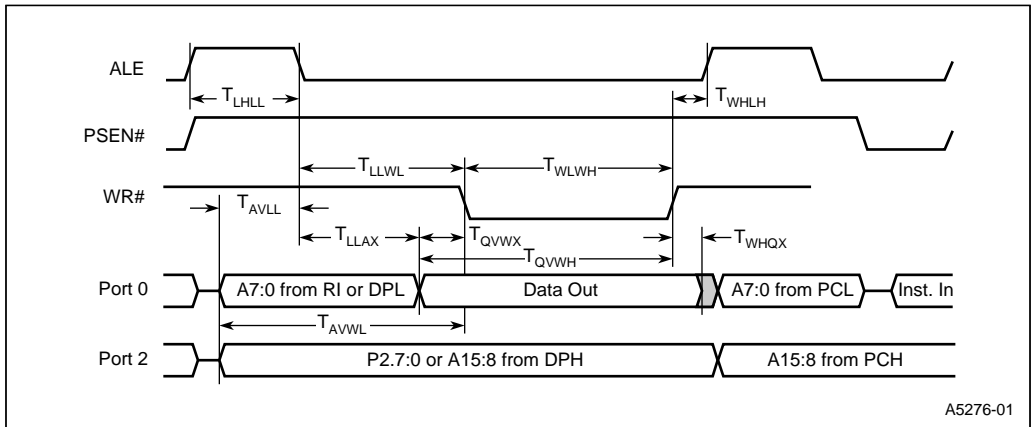


Figure 8. 8x931AA/HA External Data Memory Write

5.5 AC Characteristics — Synchronous Mode 0

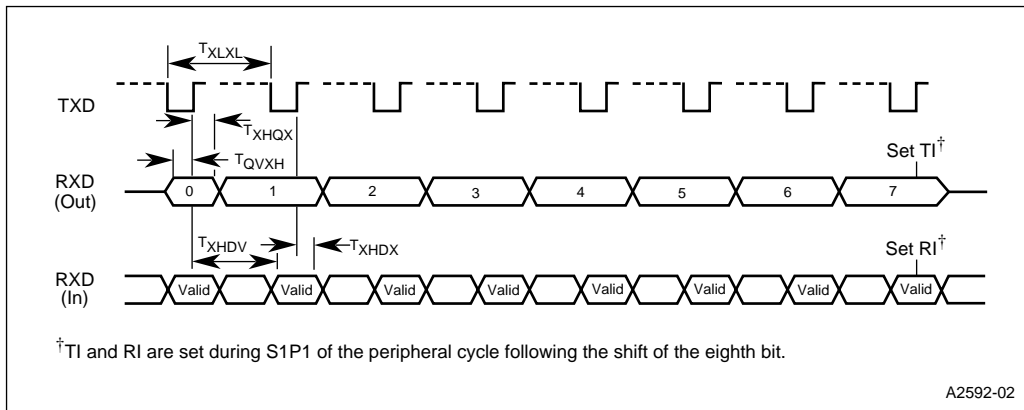


Figure 9. Serial Port Waveform — Synchronous Mode 0

Table 15. Serial Port Timing — Synchronous Mode 0

| Symbol | Parameter | Min | Max | Units |
|------------|--|--------------------|--------------------|-------|
| T_{XLXL} | Serial Port Clock Cycle Time | $12 T_{OSC}$ | | ns |
| T_{QVXH} | Output Data Setup to Clock Rising Edge | $10 T_{OSC} - 133$ | | ns |
| T_{XHQX} | Output Data Hold after Clock Rising Edge | $2 T_{OSC} - 50$ | | ns |
| T_{XHDX} | Input Data Hold after Clock Rising Edge | 0 | | ns |
| T_{XHDV} | Clock Rising Edge to Input Data Valid | | $10 T_{OSC} - 133$ | ns |

5.6 External Clock Drive

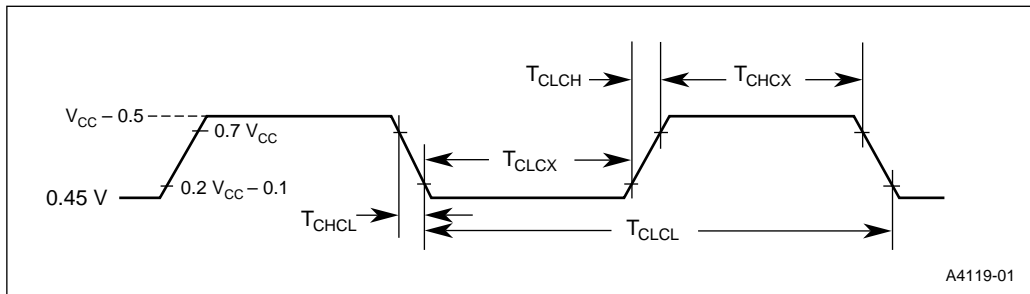


Figure 10. External Clock Drive Waveforms

Table 16. External Clock Drive

| Symbol | Parameter | Min | Max | Units |
|-------------|------------------------------------|-----|-----|-------|
| $1/T_{OSC}$ | Oscillator Frequency (F_{OSC}) | 6 | 12 | MHz |
| T_{CHCX} | High Time | 20 | | ns |
| T_{CLCX} | Low Time | 20 | | ns |
| T_{CLCH} | Rise Time | | 20 | ns |
| T_{CHCL} | Fall Time | | 20 | ns |

5.7 Testing Waveforms

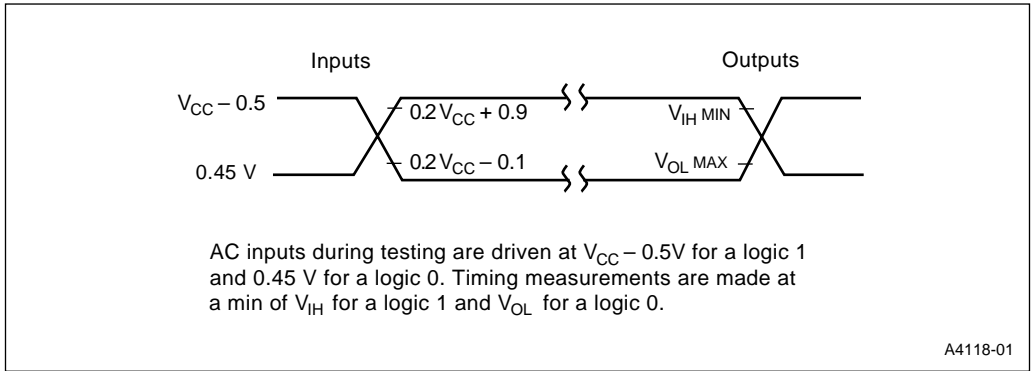


Figure 11. AC Testing Input, Output Waveforms

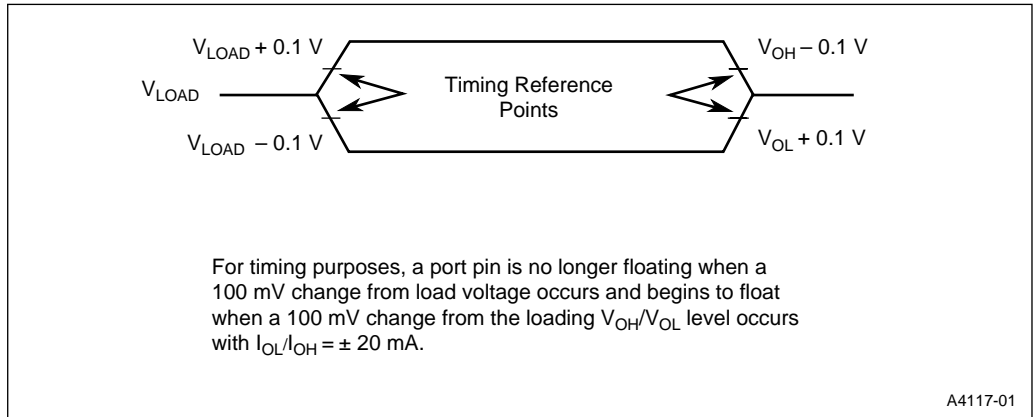


Figure 12. Float Waveforms

6.0 THERMAL CHARACTERISTICS

The microcontroller operates over the commercial temperature range from 0°C to 70°C. All thermal impedance data (see Table 17) is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel **Packaging Handbook** (order number 240800) describes Intel's thermal impedance test methodology. The **Components Quality and Reliability Handbook** (order number 210997) provides quality and reliability information.

Table 17. Thermal Characteristics

| Package Type | θ_{JA} † | θ_{JC} † |
|--------------|-----------------|-----------------|
| 68-pin PLCC | N/A | N/A |

† Data unavailable at time of publication.

7.0 DESIGN CONSIDERATIONS

7.1 Low Clock Mode Frequency

During low clock mode, the internal clock F_{CLK} distributed to the CPU and peripherals is 3 MHz. Peripheral timing and external bus accesses (including instruction fetch and data read/write) are affected. Refer to Table 10 and Table 11 for clock rates.

7.2 Setting RXFFRC Bit Clears Only the Oldest Packet in the FIFO

If the receive FIFO is set as a dual packet mode, then it can receive two packets. Setting RXFFRC (in RXCON registers) to indicate FIFO Read Complete will **not** flush the entire FIFO; it will flush only the oldest packet. The read marker will be advanced to the location of the read pointer.

7.3 Series Resistor Requirement for Impedance Matching

Per USB rev. 1.0 specification (page 111, section 7.1.1.1), the impedance of the differential driver must be between 29Ω and 44Ω. To match the cable impedance, a series resistor of 27Ω to 33Ω should be connected to each USB line; i.e., on D_{P0} and on D_{M0} . If the USB line is improperly terminated or not matched, then signal fidelity will suffer. This

condition can be seen on the oscilloscopes as excessive overshoot and undershoot. This condition can potentially introduce bit errors.

7.4 Pullup Resistor Requirement for 8x931AA/HA devices

The USB specification requires a pullup resistor to allow the host to identify which devices are low speed and which are full speed in order to communicate at the appropriate data rate. For 8x931HA hub devices (12 Mbps), use a 1.5KΩ pullup resistor (to 3.0 V – 3.6 V; may use the ECAP pin.) on the D_{P0} line. 8x931AA devices can be either full speed or low speed; add a 1.5KΩ pullup to the appropriate USB line.

7.5 Powerdown Mode Cannot Be Invoked Before USB Suspend

If the 8x931AA/HA is put into powerdown mode before receiving a USB suspend signal from the host, then a USB resume will not properly wake up the 8x931AA/HA from powerdown mode.

7.6 Unused Downstream Ports

If the USB downstream ports are not used, it is still required that the two data lines be pulled low externally (similar to a disconnect) so that the inputs are not floating. This will eliminate the possibility of induced system noise. All USB data lines require 15KΩ external pulldown resistors. Do **not** leave unused port(s) disconnected.

7.7 ECAP Usage to Supply 3.0 to 3.6 Volts for 1.5K Ohm Pullup

For a self-powered or bus-powered device, when the voltage at the V_{CC} pins are at 5.25v, the voltage at ECAP pin will be at approximately 3.6v. If the V_{CC} pin is at 4.65v [Min, Vbus Powered (host or hub) Port specification], the voltage at the ECAP pin will be at approximately 3.2v (refer to Table 18 below). The capability for this pin to supply the 3.0v to 3.6v voltage to the 1.5KΩ USB pullup terminator depends upon the V_{CC} voltage level.

For a bus-powered device that is connected to a bus-powered hub, when the voltage at the Vcc pins (in the bus-powered devices) are at 4.28v, the voltage at ECAP pin will be at approximately 3.0v. If the Vcc voltage drops below 4.28v, the ECAP pin can not supply voltage above 3.0 v for the 1.5KΩ USB pullup terminator.

NOTE: *The typical ECAP values, listed in the table below, reflect a 1 μF capacitor connection between the ECAP pin and ground.*

Table 18. Vcc and Typical ECAP Voltages

| Vcc | ECAP Pin |
|-------|----------|
| 5.25v | 3.6v |
| 5.00v | 3.5v |
| 4.65v | 3.2v |
| 4.40v | 3.1v |
| 4.28v | 3.0v |

8.0 8x931AA/HA ERRATA

The 8x931AA/HA may contain design defects or errors known as errata. Characterized errata that may cause the 8x931AA/HA's operational behavior to deviate from published specifications are documented in a specification update. Specification updates can be obtained from your local Intel sales office or from the World Wide Web (www.intel.com).

9.0 DATASHEET REVISION HISTORY

Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This is the original version of the datasheet.

