ADVANCE INFORMATION

8XC196NT
CHMOS MICROCONTROLLER WITH 1 MBYTE LINEAR ADDRESS SPACE

- **20 MHz Operation**
- **High Performance CHMOS 16-Bit CPU**
- **Up to 32 Kbytes of On-Chip OTPROM**
- **Up to 1 Kbyte of On-Chip Register RAM**
- **Up to 512 Bytes of Internal RAM**
- **Register-Register Architecture**
- **4 Channel/10-Bit A/D with Sample/Hold**
- **37 Prioritized Interrupt Sources**
- **Up to Seven 8-Bit (56) I/O Ports**
- **Full Duplex Serial I/O Port**
- **Dedicated Baud Rate Generator**
- **Interprocessor Communication Slave Port**
- **Selectable Bus Timing Modes for Flexible External Memory Interfacing**
- **Oscillator Fail Detection Circuitry**
- **High Speed Peripheral Transaction Server (PTS)**
- **Two Dedicated 16-Bit High-Speed Compare Registers**
- **10 High Speed Capture/Compare (EPA)**
- **Full Duplex Synchronous Serial I/O Port (SSIO)**
- **Two Flexible 16-Bit Timer/Counters**
- **Quadrature Counting Inputs**
- **Flexible 8-/16-Bit External Bus (Programmable)**
- **Programmable Bus (HOLD/HLDA)**
- **1.4 μs 16 x 16 Multiply**
- **2.4 μs 32/16 Divide**
- **68-Pin Package**

Device	Pins/Package	OTPROM	Reg RAM	Code RAM	Address Space	I/O	EPA	A/D
8XC196NT	68P PLCC	32K	1K	512	1 Mbyte	56	10	4

X = 7 OTPROM Device
X = 0 ROMLESS

The 8XC196NT 16-bit microcontroller is a high performance member of the MCS® 96 microcontroller family. The 8XC196NT is an enhanced 8XC196KR device with 1 Mbyte of linear address space, 1000 bytes of register RAM, 512 bytes of internal RAM, 20 MHz operation and an optional 32 Kbytes of OTPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

Ten high-speed capture/compare modules are provided. As capture modules event times with 200 ns resolution can be recorded and generate interrupts. As compare modules events such as toggling of a port pin, starting an A/D conversion, pulse width modulation, and software timers can be generated. Events can be based on the timer or up/down counter.

December 1996

Order Number: 272267-005

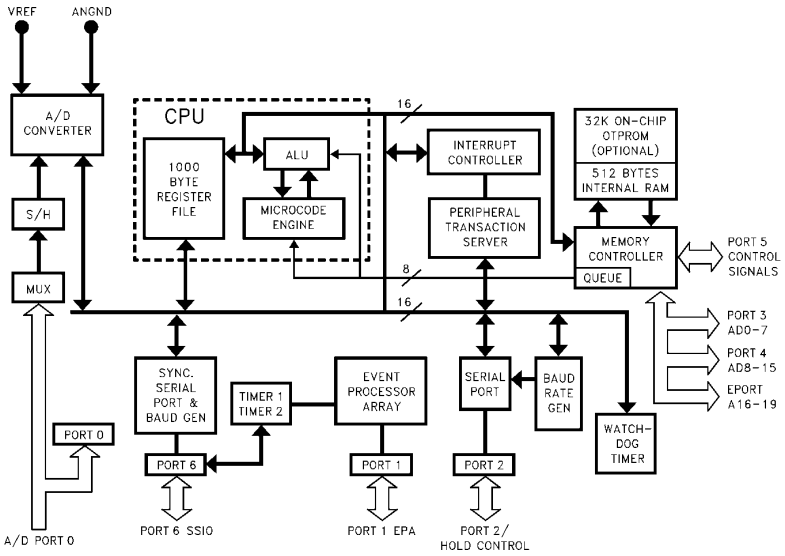


Figure 1. 8XC196NT Block Diagram

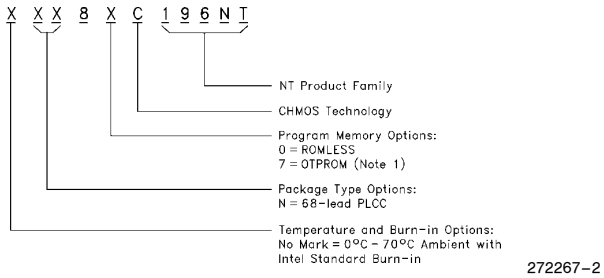
PROCESS INFORMATION

This device is manufactured on P629.5, a CHMOS III-E process. Additional process and reliability information is available in the *Intel® Quality System Handbook*.

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
PLCC	36.5°C/W	13°C/W



EXAMPLE: N87C196NT is 68-Lead PLCC OTPROM.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

Figure 2. The 8XC186NT Familiy Nomenclature

8XC196NT Memory Map

Address (Note 7)	Description
FFFFFFH FFA000H	External Memory
FF9FFFH FF2080H	Internal OTPROM or External Memory (Determined by $\overline{EA}$ Pin) RESET at FF2080H
FF207FH FF2000H	Reserved Memory (Internal OTPROM or External Memory) (Determined by $\overline{EA}$ Pin)
FF1FFFH FF0600H	External Memory
FF05FFH FF0400H	Internal RAM (Identically Mapped into 00400H–005FFH)
FF03FFH FF0100H	External Memory
FF00FFH FF0000H	Reserved for ICE
FEFFFFH 100000H	External Memory for future devices
FFFFFH 00A000H	984 Kbytes External Memory
009FFFH 002080H	Internal OTPROM or External Memory (Note 1)
00207FH 002000H	Reserved Memory (Internal OTPROM or External Memory) (Notes 1, 3, and 6)
001FFFH 001FE0H	Memory Mapped Special Function Registers (SFR's)
001FDFH 001F00H	Internal Special Function Registers (SFR's) (Note 5)
001EFFH 000600H	External Memory
0005FFH 000400H	Internal RAM (Address with Indirect or Indexed Modes)
0003FFH 000100H	Register RAM — Upper Register File (Address with Indirect or Indexed Modes or through Windows.) (Note 2)
0000FFH 000018H	Register RAM — Lower Register File (Address with Direct, Indirect, or Indexed Modes.) (Notes 2, 4)
000017H 000000H	CPU SFR's — Lower Register File (Address with Direct, Indirect, or Indexed Modes.) (Notes 2, 4)

NOTES:
1. These areas are mapped internal OTPROM if the REMAP bit (CCB2.2) is set and $\overline{EA}$ = 5V. Otherwise they are external memory.
2. Code executed in locations 00000H to 003FFH will be forced external.
3. Reserved memory locations must contain 0FFH unless noted.
4. Reserved SFR bit locations must be written with 0.
5. Refer to 8XC196NT User's Guide and Quick Reference for SFR descriptions.
6. **WARNING:** The contents or functions of reserved memory locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.
7. The 8XC196NT internally uses 24 bit address, but only 20 address lines are bonded out allowing 1 Mbyte external address space.

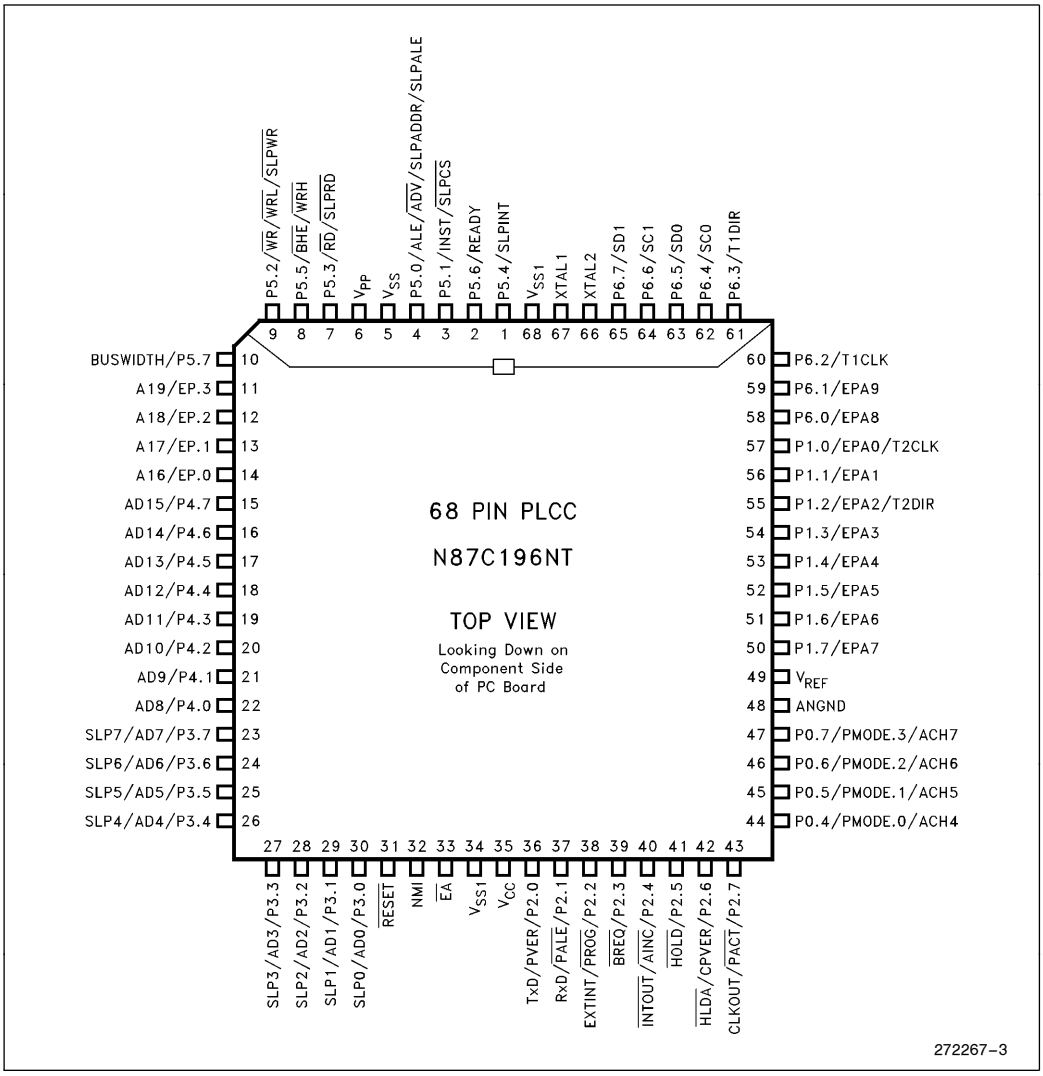


Figure 3. 68-Pin PLCC Package Diagram

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}, V_{SS1}, V_{SS1}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the OTPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. Connect to V_{CC} if powerdown not being used.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. $\overline{\text{RESET}}$ has an internal pullup.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dyamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is ''0'' and CCR1 bit 2 is ''1'', all bus cycles are 8-bit, if CCR bit 1 is ''1'' and CCR1 bit 2 is ''0'', all bus cycles are 16-bit. CCR bit 1 = ''0'' and CCR1 bit 2 = ''0'' is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non maskable interrupt vector through memory location 203EH.
P5.1/INST/$\overline{\text{SLPCS}}$	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal OTPROM fetches INST is held low. Also LSIO when not INST. $\overline{\text{SLPCS}}$ is the Slave Port Chip Select.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a high causes memory accesses to locations 0FF2000H through 0FF9FFFH to be directed to on-chip OTPROM. $\overline{\text{EA}}$ equal to a low causes accesses to these locations to be directed to off-chip memory. $\overline{\text{EA}}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{\text{EA}}$ is latched at reset.
$\overline{\text{HOLD}}$	Bus Hold Input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
P5.0/ALE/$\overline{\text{ADV}}$/ SLPADDR/ SLPALE	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is active only during external memory accesses. Also LSIO when not used as ALE. SLPADDR is the Slave Port Address Control Input and SLPALE is the Slave Port Address Latch Enable Input.
P5.3/$\overline{\text{RD}}$/$\overline{\text{SLPRD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is active only during external memory reads or LSIO when not used as $\overline{\text{RD}}$. $\overline{\text{SLPRD}}$ is the Slave Port Read Control Input.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
P5.2/$\overline{WR}$/$\overline{WRL}$/$\overline{SLPWR}$	Write and Write Low output to external memory, as selected by the CCR, $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active during external memory writes. Also an LSIO pin when not used as $\overline{WR}$/$\overline{WRL}$. $\overline{SLPWR}$ is the Slave Port Write Control Input
P5.5/$\overline{BHE}$/$\overline{WRH}$	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0) or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory read/write cycles. Also an LSIO pin when not BHE/$\overline{WRH}$.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.3/T1DIR	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–7 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH4–7	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to OTPROM parts to select the Programming Mode.
P6.3–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
EPORT	8-bit bidirectional standard and I/O port. These bits are shared with the extended address bus, A16–A19. Pin function is selected on a per pin basis.
$\overline{INTOUT}$	Interrupt Output. This active-low output indicates that a pending interrupt requires use of the external bus.
SLP0–SLP7	Slave Port Address/Data Bus

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND . . . . . −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND . . . . . −0.5 to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation 0.5W

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	20	MHz (Note 4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current			90	mA	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While device in Reset)
I_{REF}	A/D Reference Supply Current			5	mA	
I_{IDLE}	Idle Mode Current			40	mA	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current(6)		50	75	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$(11)
V_{IL}	Input Low Voltage (all pins)	−0.5V		0.3 V_{CC}	V	For PORT0(10)
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	For PORT0(10)
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	XTAL1 Input Pin Only(1)
V_{IH2}	Input High Voltage on RESET	0.7 V_{CC}		V_{CC} + 0.5	V	RESET input pin only
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA(3,5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Complementary)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200µA(3,5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
I_{LI1}	Input Leakage Current (Port 0)			±3	µA	$V_{CC} < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current			−70	µA	V_{IN} = 0.45V(1)

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OL1}	Output Low Voltage in RESET			0.8	V	(Note 7)
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output High Voltage in RESET	2.0			V	$I_{OH} = 0.8$ mA(7)
V_{OH2}	Output High Voltage in RESET	$V_{CC}-1V$			V	$I_{OH} = -6\ \mu A$(1)
C_S	Pin Capacitance (Any pin to V_{SS})			10	pF	$f_{test} = 1.0$ MHz
R_{WPU}	Weak Pullup Resistance		150K		Ω	(Note 6)
R_{RST}	Reset Pullup	65K		180K	Ω	

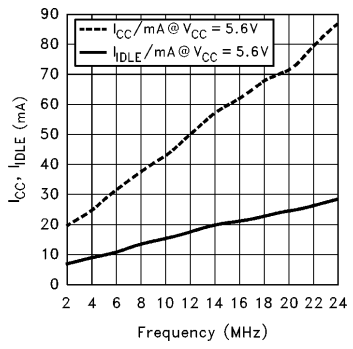
NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5, Port6 and EPORT except SPLINT (P5.4) and HLDA (P2.6).
2. Standard input pins include XTAL1, $\overline{EA}$, RESET, and Port 1/2/5/6 and EPORT when setup as inputs.
3. All bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{DL}/I_{DH} currents per pin are as follows:

   a.) Test Condition: $V_{OH} = V_{CC} - 0.7V$ $V_{OL} = 0.45V$

   Part 1: $I_{OL} = 0.65$ mA $I_{OH} = 7.5$ mA
   Part 2: $I_{OL} = 8.0$ mA $I_{OH} = 12.0$ mA
   Part 3: $I_{OL} = 7.5$ mA $I_{OH} = 7.5$ mA
   Part 4: $I_{OL} = 7.5$ mA $I_{OH} = 7.5$ mA
   Part 5: $I_{OL} = 9.0$ mA $I_{OH} = 9.0$ mA
   Part 6: $I_{OL} = 8.0$ mA $I_{OH} = 9.0$ mA

   b.) Test Condition: $V_{OH} = V_{CC} - 1.5V$ $V_{OL} = 1.5V$

   Part 1: $I_{OL} = 21.0$ mA $I_{OH} = 26.0$ mA
   Part 2: $I_{OL} = 26.0$ mA $I_{OH} = 29.0$ mA
   Part 3: $I_{OL} = 17.0$ mA $I_{OH} = 25.0$ mA
   Part 4: $I_{OL} = 16.0$ mA $I_{OH} = 25.0$ mA
   Part 5: $I_{OL} = 21.0$ mA $I_{OH} = 28.0$ mA
   Part 6: $I_{OL} = 19.0$ mA $I_{OH} = 26.0$ mA
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.5V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. TBD = To Be Determined.
9. Pullup present during return from powerdown condition.
10. When P0 is used as analog inputs, refer to A/D specifications.
11. For temperatures <100°C typical is 10 μA.



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8XC196NT ADDITIONAL BUS TIMING MODES

The 8XC196NT device has 3 additional bus timing modes for external memory interfacing.

MODE 3:

Mode 3 is the standard timing mode. Use this mode for systems that emulate the 8XC196KR bus timings.

MODE 0:

Mode 0 is the standard timing mode, but 1 (minimum) wait state is always inserted in external bus cycles.

MODE 1:

Mode 1 is the long R/W mode. This mode advances $\overline{RD}$ and $\overline{WR}$ signals by 1 T_{OSC} creating a 2 T_{OSC} $\overline{RD}$/$\overline{WR}$ low time. ALE is also advanced by 0.5 T_{OSC} but ALE high time remains 1 T_{OSC}.

MODE 2:

Mode 2 is the long R/W mode with Early Address. Mode 2 is similar to Mode 1 with respect to $\overline{RD}$, $\overline{WR}$, and ALE signals. Additionally, the address is output on the bus 0.5 T_{OSC} earlier in the bus cycle.

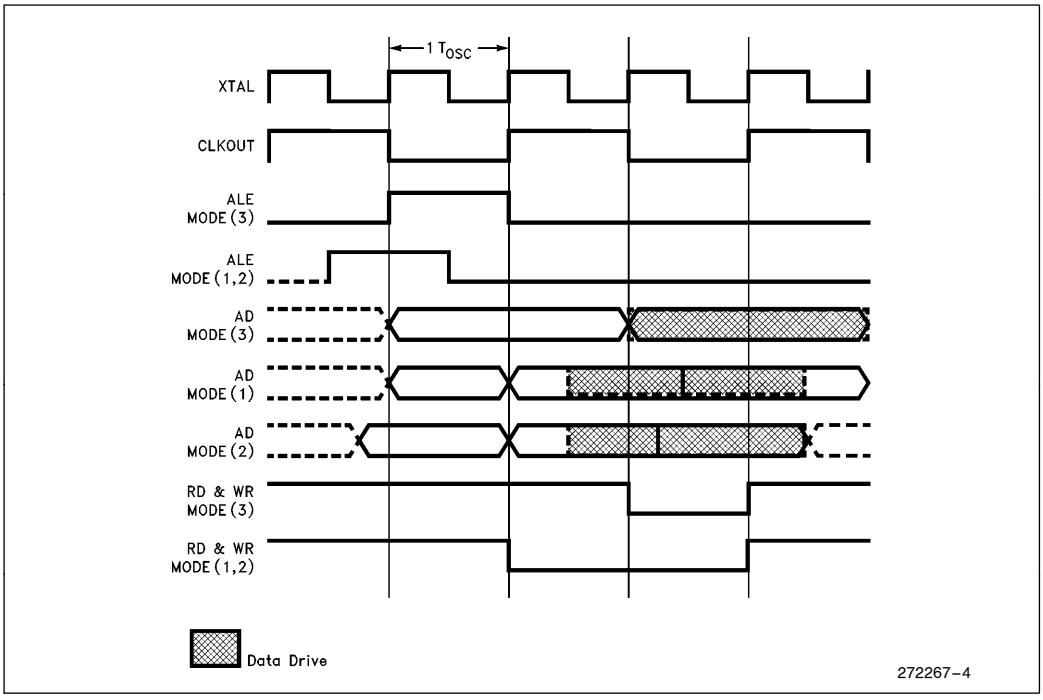


Figure 4. Detailed MODE 1, 2, 3, Comparison

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:	Signals:	
H—High	A—Address	HA—$\overline{\text{HLDA}}$
L—Low	B—$\overline{\text{BHE}}$	L—ALE/$\overline{\text{ADV}}$
V—Valid	BR—$\overline{\text{BREQ}}$	Q—Data Out
X—No Longer Valid	C—CLKOUT	RD—$\overline{\text{RD}}$
Z—Floating	D—DATA	W—$\overline{\text{WR}}$/$\overline{\text{WRH}}$/$\overline{\text{WRI}}$
	G—Buswidth	X—XTAL1
	H—$\overline{\text{HOLD}}$	Y—READY

BUS MODE 0 and 3—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\,T_{OSC} - 75$	ns(3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\,T_{OSC} - 75$	ns(2, 3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns(2, 3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 55$	ns(2)
T_{RLDV}	$\overline{\text{RD}}$ active to input Data Valid		$T_{OSC} - 30$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of $\overline{\text{RD}}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{\text{RD}}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2\,T_{OSC} \times n$, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add $2\,T_{OSC}$ to the specification.

BUS MODE 0 and 3—AC CHARACTERISTICS (Over Specified Operating Conditions)

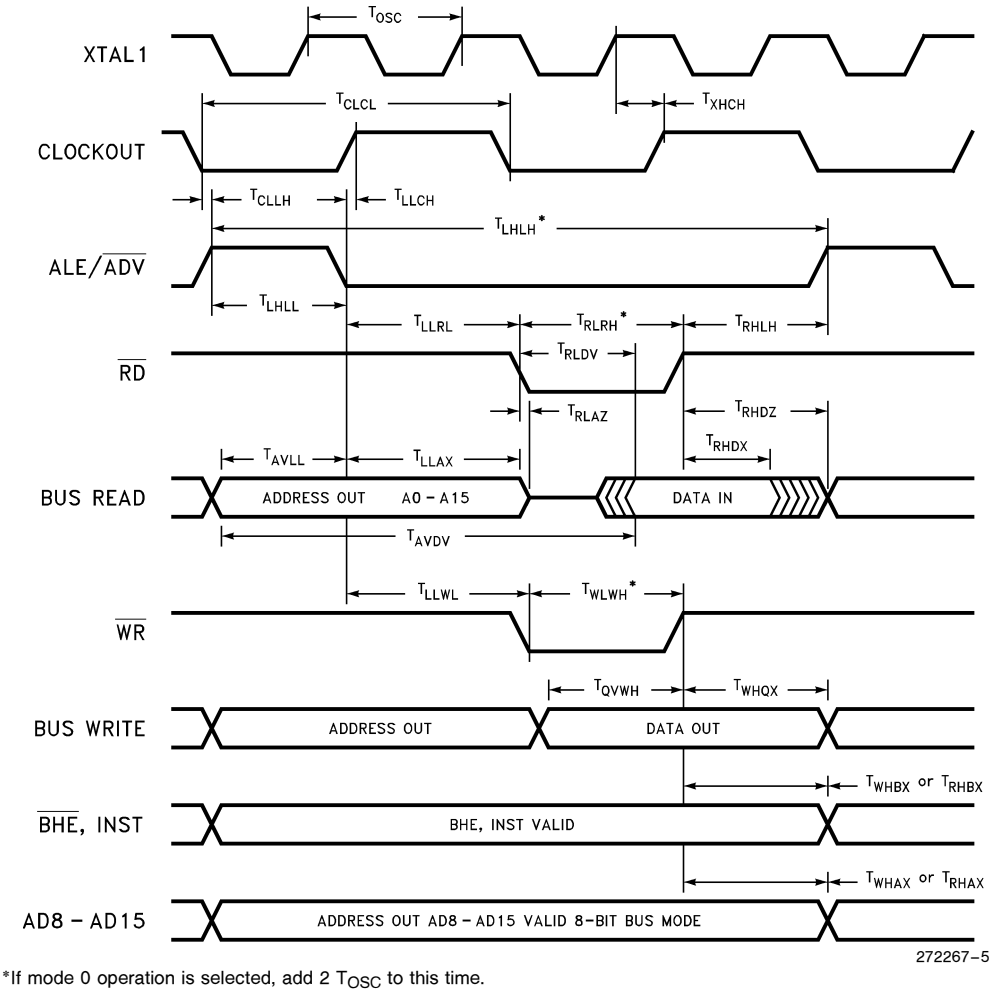
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{OFD}	Clock Failure to Reset Pulled Low(6)	4	40	μs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 30	ns
T_{CLLH}	CLKOUT Low to ALE/$\overline{ADV}$ High	−10	+15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Low to CLKOUT High	−25	+15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	T_{OSC} − 40		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	−5	+35	ns
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	T_{OSC}	T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	−10	+25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{OSC} − 35		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	T_{OSC} − 10	T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ High	T_{OSC} − 10		ns
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ High	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	T_{OSC} − 30		ns(4)

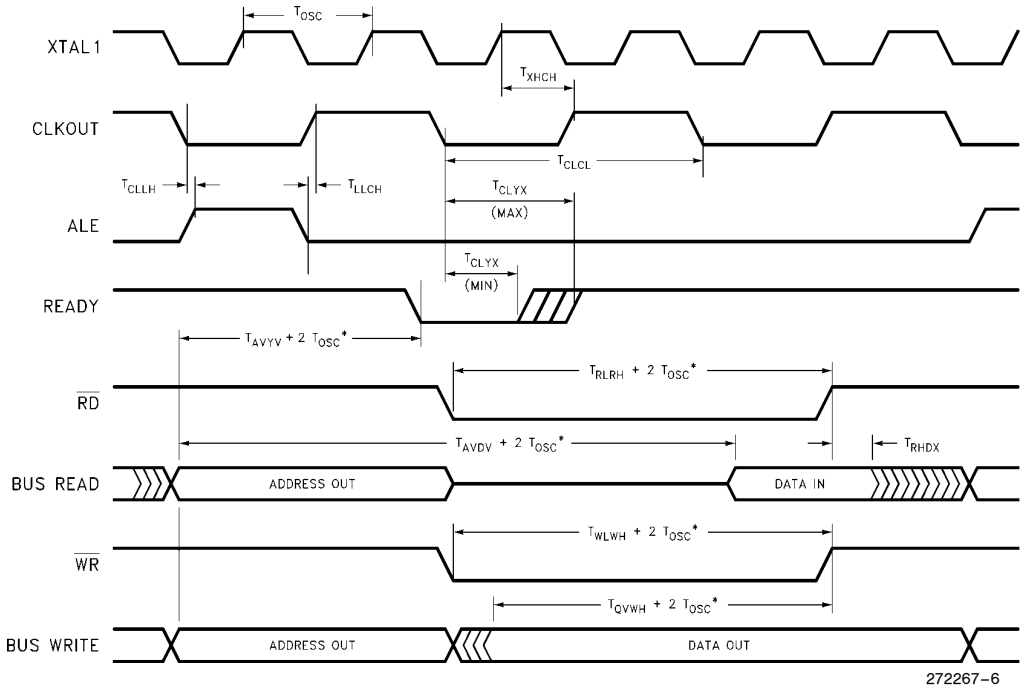
NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. NT/NQ customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

BUS MODE 0 and 3—8XC196NT SYSTEM BUS TIMING



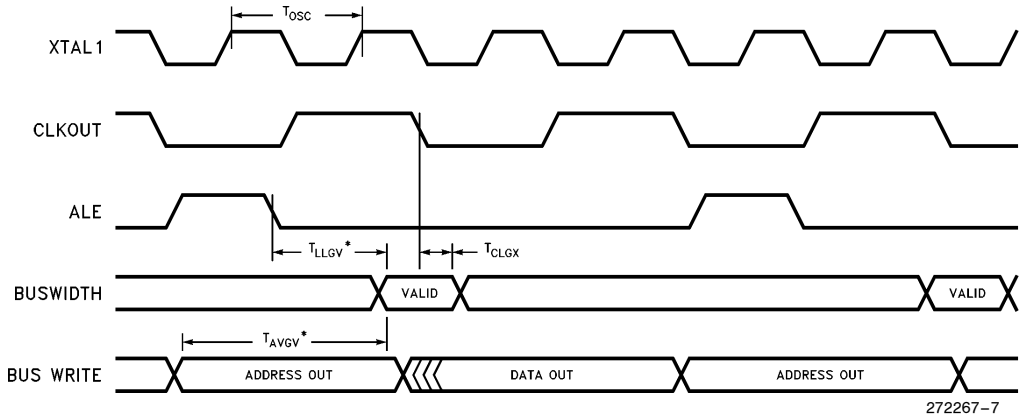
*If mode 0 operation is selected, add 2 T_{OSC} to this time.

8XC196NT MODE 0 and 3—READY TIMINGS (ONE WAIT STATE)



*If mode 0 selected, one wait state is always added. If additional wait states are required, add 2 T_{OSC} to these specifications.

MODE 0 and 3—8XC196NT BUSWIDTH TIMINGS



*If mode 0 selected, add 2 T_{OSC} to these specifications.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\ T_{OSC} - 75$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\ T_{OSC} - 75$	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		$1.5\ T_{OSC} - 60$	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\ T_{OSC} - 60$	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		$2\ T_{OSC} - 44$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2\ T_{OSC} \times n$, where n = number of wait states.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

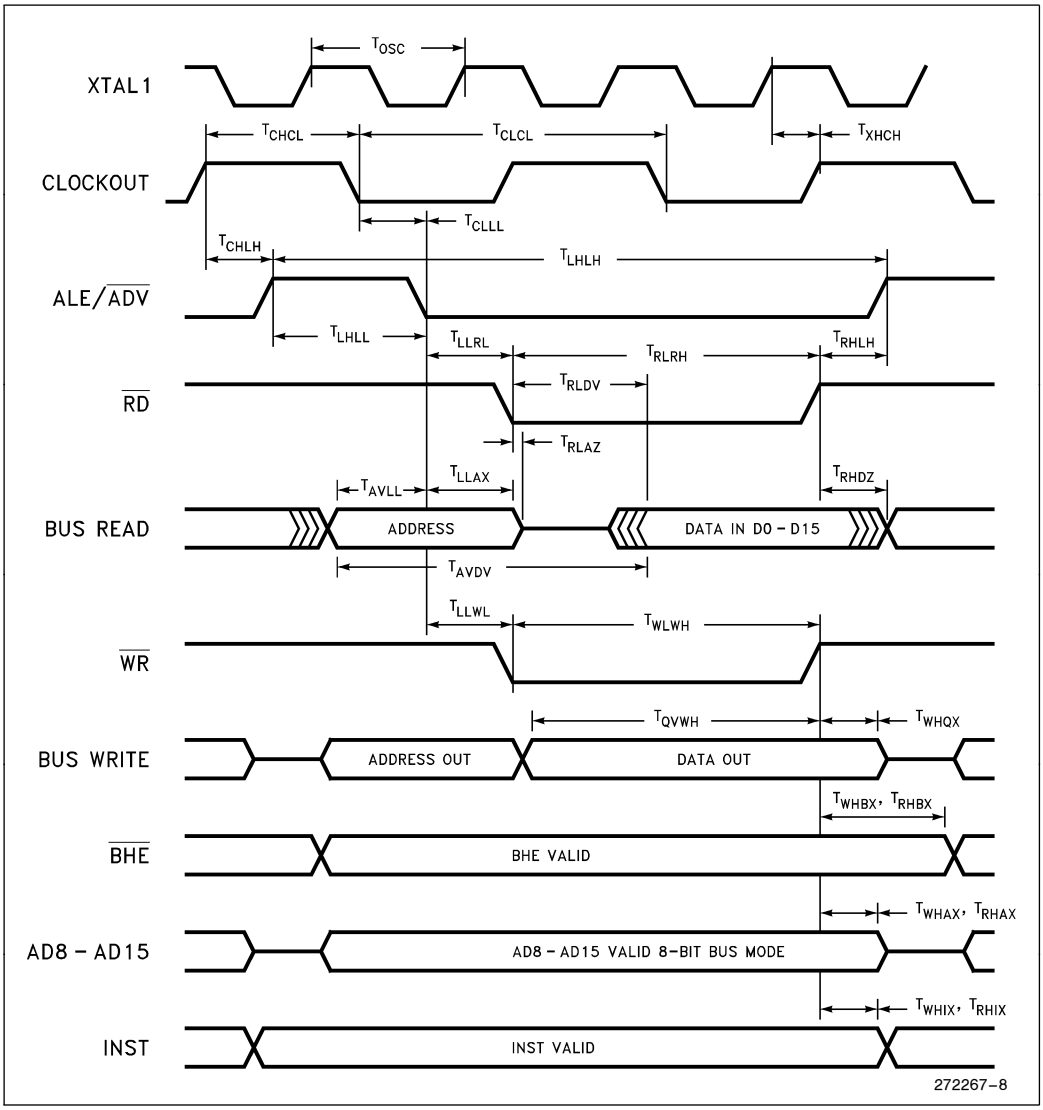
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

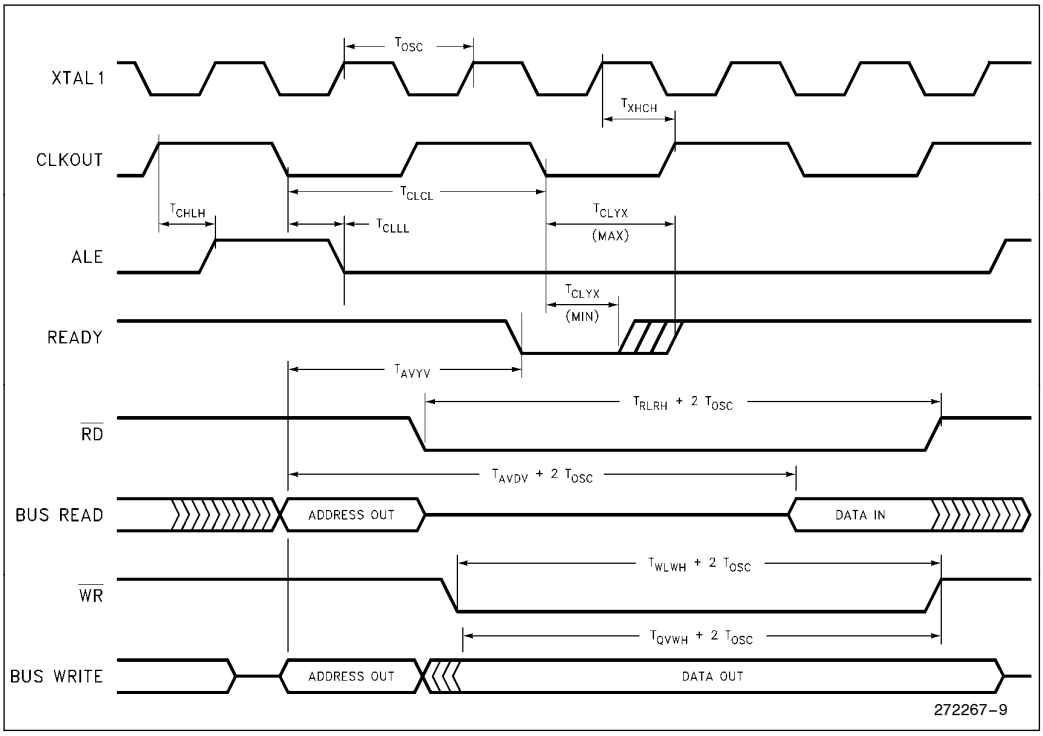
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 15	0.5 T_{OSC} + 15	ns
T_{CLLL}	CLKOUT LOW to ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 20	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	0.5 T_{OSC} − 20		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	0.5 T_{OSC} − 15		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	$\overline{RD}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC}	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	T_{OSC} − 15	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	2 T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	2 T_{OSC} − 15		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	0.5 T_{OSC} − 12		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$ Hold after $\overline{WR}$ High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after $\overline{WR}$ High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$ Hold after $\overline{RD}$ High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after $\overline{RD}$ High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

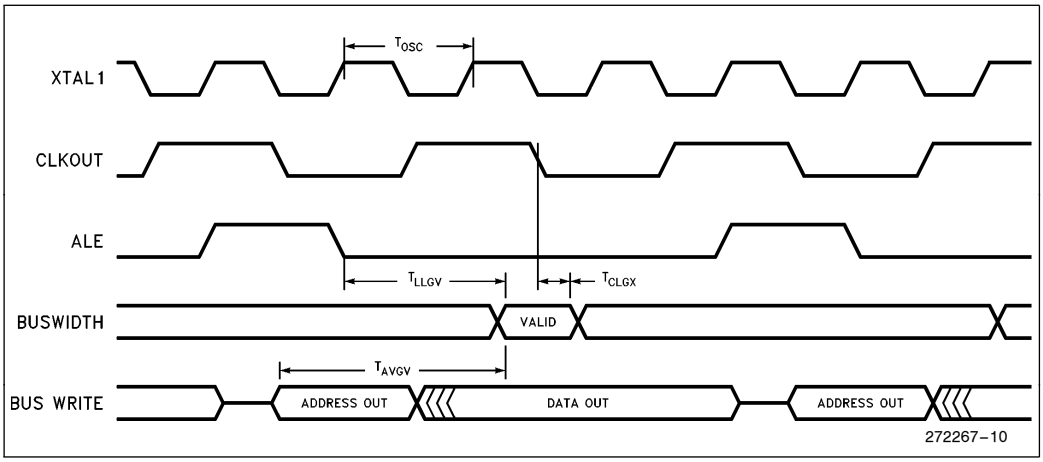
MODE 1—8XC196NT SYSTEM BUS TIMING



MODE 1—8XC196NT READY TIMINGS (ONE WAIT STATE)



MODE 1—8XC196NT BUSWIDTH TIMINGS



BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2.5 T_{OSC} − 75	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2.5 T_{OSC} − 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		1.5 T_{OSC} − 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3.5 T_{OSC} − 55	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		2 T_{OSC} − 44	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 60	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		0.5 T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

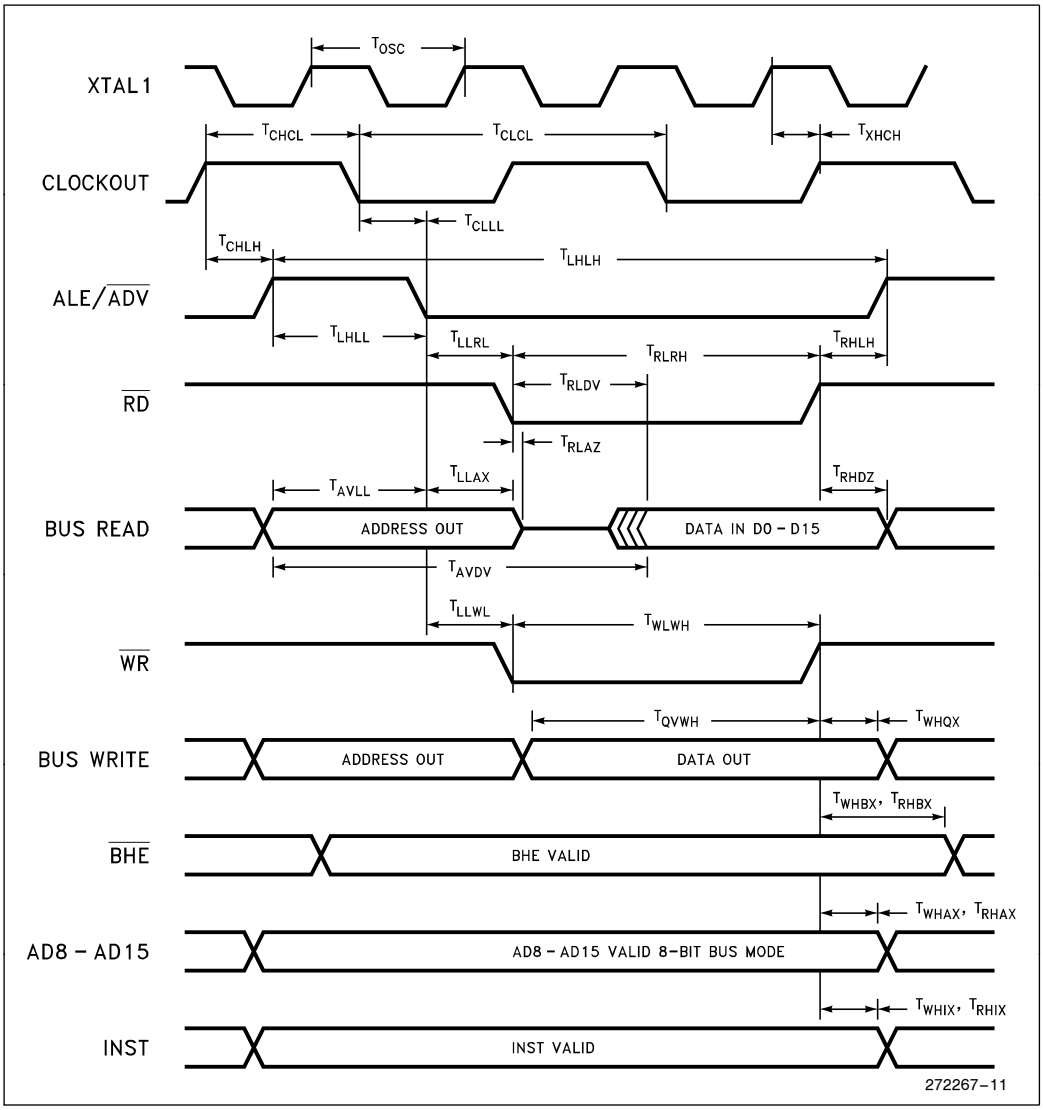
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

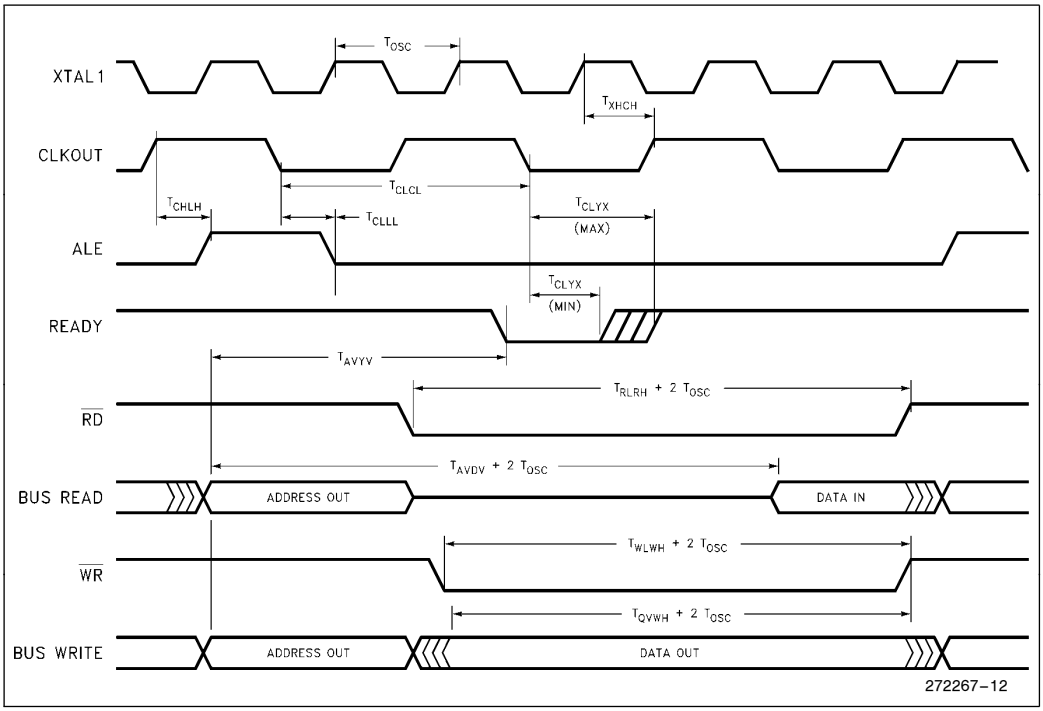
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+85	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 15	0.5 T_{OSC} + 15	ns
T_{CLLL}	CLKOUT LOW to ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 20	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 20		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	0.5 T_{OSC} − 15		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	$\overline{RD}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 5	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	T_{OSC} − 22	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	2 T_{OSC} − 25		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	0.5 T_{OSC} − 12		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	$\overline{BHE}$ Hold after $\overline{WR}$ High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after $\overline{WR}$ High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$ Hold after $\overline{RD}$ High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after $\overline{RD}$ High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

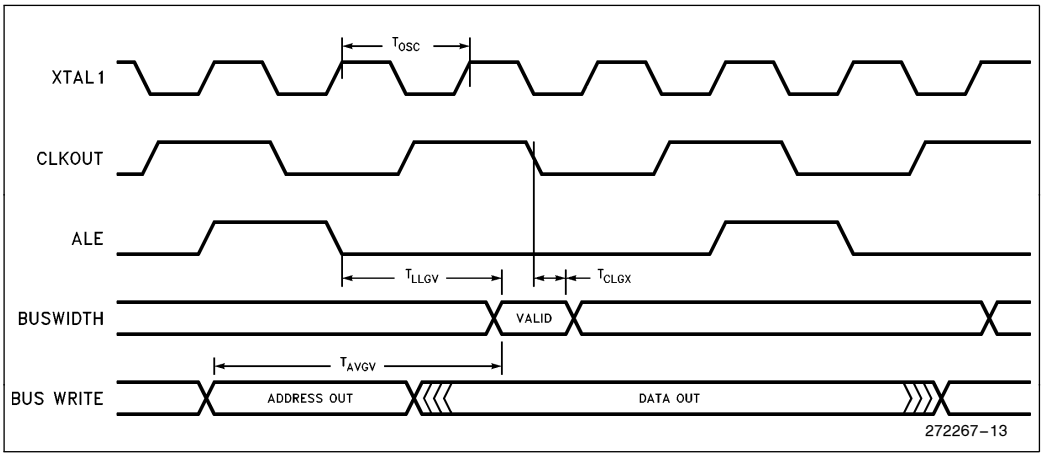
MODE 2—8XC196NT SYSTEM BUS TIMING



MODE 2—8XC196NT READY TIMINGS (ONE WAIT STATE)



MODE 2—8XC196NT BUSWIDTH TIMINGS



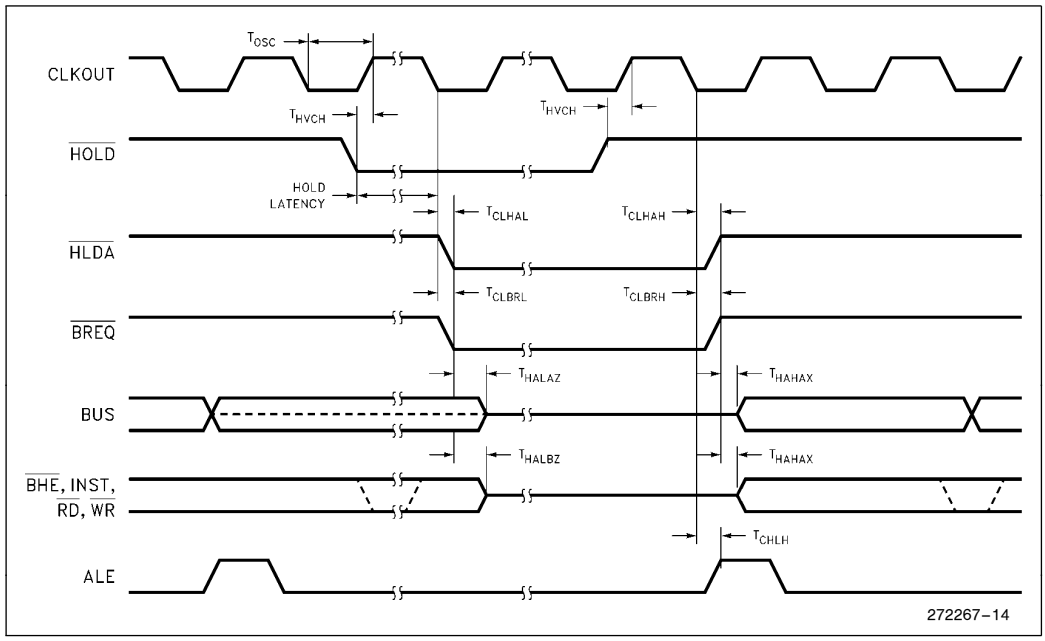
BUS MODE 0, 1, 2, and 3—$\overline{HOLD}$/$\overline{HLDA}$ TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	$\overline{HOLD}$ Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to $\overline{HLDA}$ Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to $\overline{BREQ}$ Low	−15	+15	ns
T_{HALAZ}	$\overline{HLDA}$ Low to Address Float		+25	ns
T_{HALBZ}	$\overline{HLDA}$ Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to $\overline{HLDA}$ High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to $\overline{BREQ}$ High	−25	+25	ns
T_{HAHAX}	$\overline{HLDA}$ High to Address No Longer Float	−15		ns
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10		ns

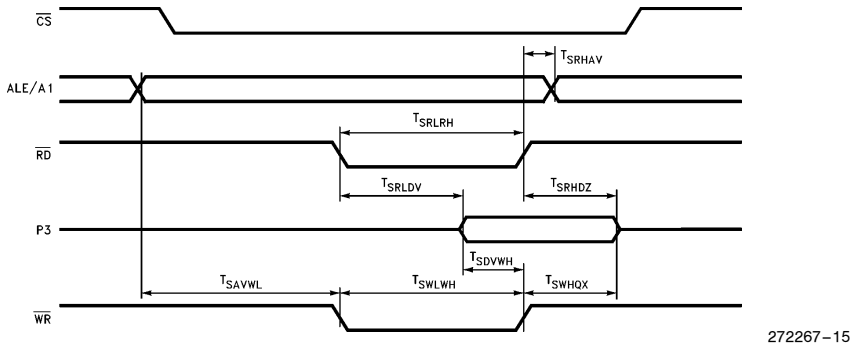
NOTE:
1. To guarantee recognition at next clock.

8XC196NT $\overline{HOLD}$/$\overline{HLDA}$ TIMINGS



AC CHARACTERISTICS—SLAVE PORT

SLAVE PORT WAVEFORM—(SLPL = 0)



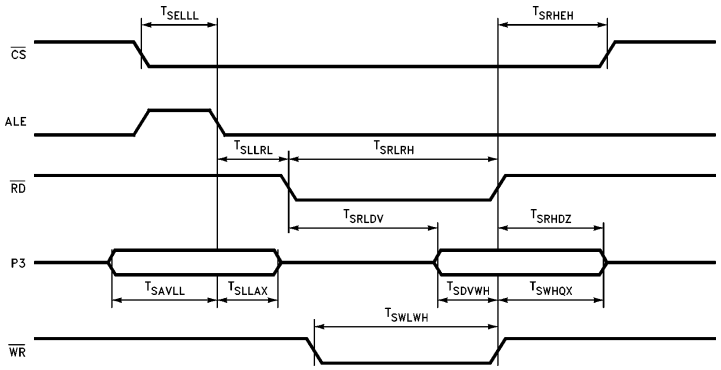
SLAVE PORT TIMING—(SLPL = 0)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to $\overline{WR}$ Low	50		ns
T_{SRHAV}	$\overline{RD}$ High to Address Valid	60		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 50 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

AC CHARACTERISTICS—SLAVE PORT (Continued)

SLAVE PORT WAVEFORM—(SLPL = 1)



SLAVE PORT TIMING—(SLPL = 1)

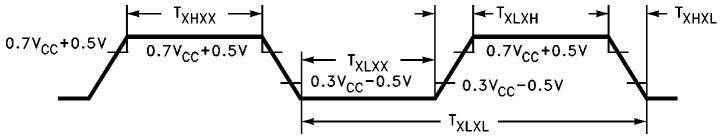
Symbol	Parameter	Min	Max	Units
T_{SELLL}	$\overline{CS}$ Low to ALE Low	20		ns
T_{SRHEH}	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	60		ns
T_{SLLRL}	ALE Low to $\overline{RD}$ Low	T_{OSC}		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 50 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

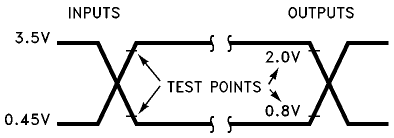
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	20	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	50	250	ns
T_{XHXX}	High Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS

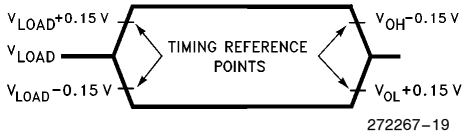


AC TESTING INPUT, OUTPUT WAVEFORMS



AC Testing inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

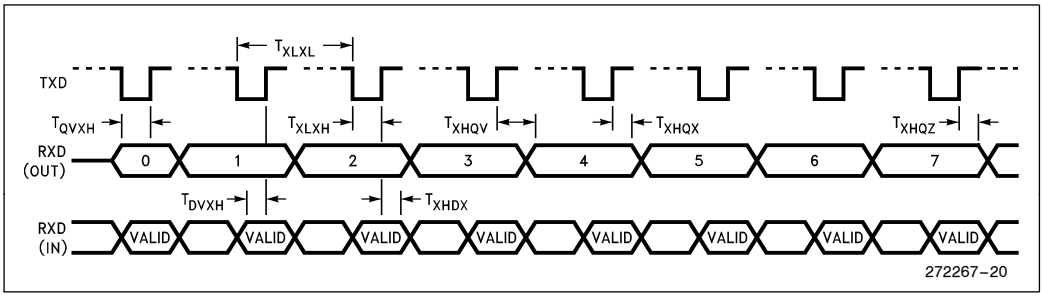
FLOAT WAVEFORMS



For timing purposes a Port Pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



AC CHARACTERISTICS—SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}(2)	Serial Port Clock Period (BRR ≥ 8002H) Receive Only	6 T_{OSC}		ns
T_{XLXH}(2)	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}(2)	Serial Port Clock Period (BRR = 8001H) Transmit Only	4 T_{OSC}		ns
T_{XLXH}(2)	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(1)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(1)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTES:
1. Parameters not tested.
2. The minimum baud rate register value for Receive is 8002H. The minimum baud rate register value for Transmit is 8001H.

A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10	15	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD__TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3.0	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3.0	LSBs
Differential Non-Linearity		−0.75	+0.75	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An ''LSB'' as used here has a value of approximately 5 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	7	20	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD__TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1.0	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1.0	LSBs
Differential Non-Linearity		−0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An ''LSB'' as used here has a value of approximately 5 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

OTPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	°C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	20.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC OTPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(2)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with F_{OSC} = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
2. This specification is for the word dump mode. For programming pulses use Modified Quick Pulse Algorithm.

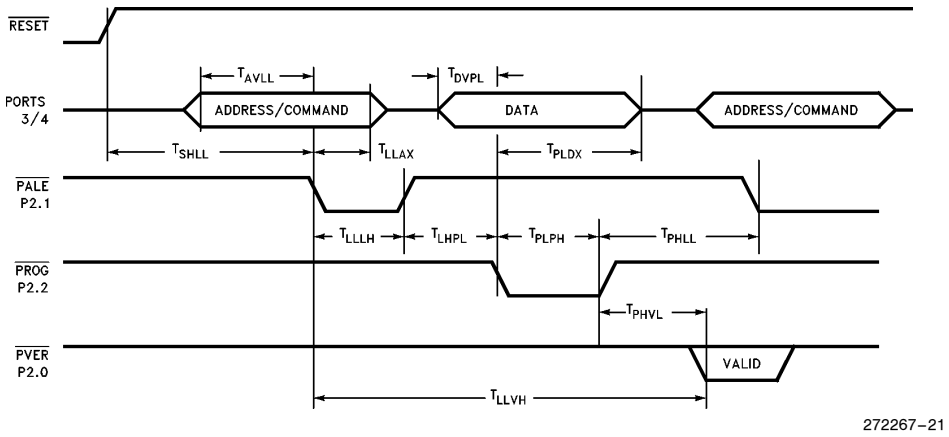
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

NOTE:
Do not apply V_{PP} unti V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

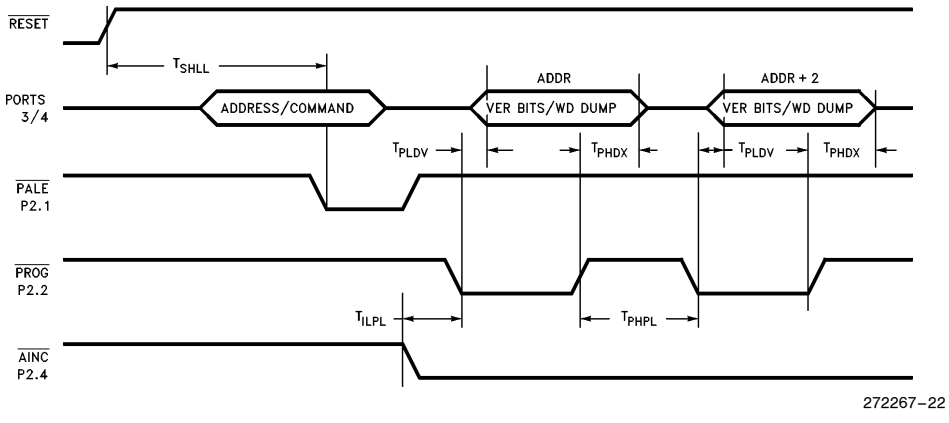
OTPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



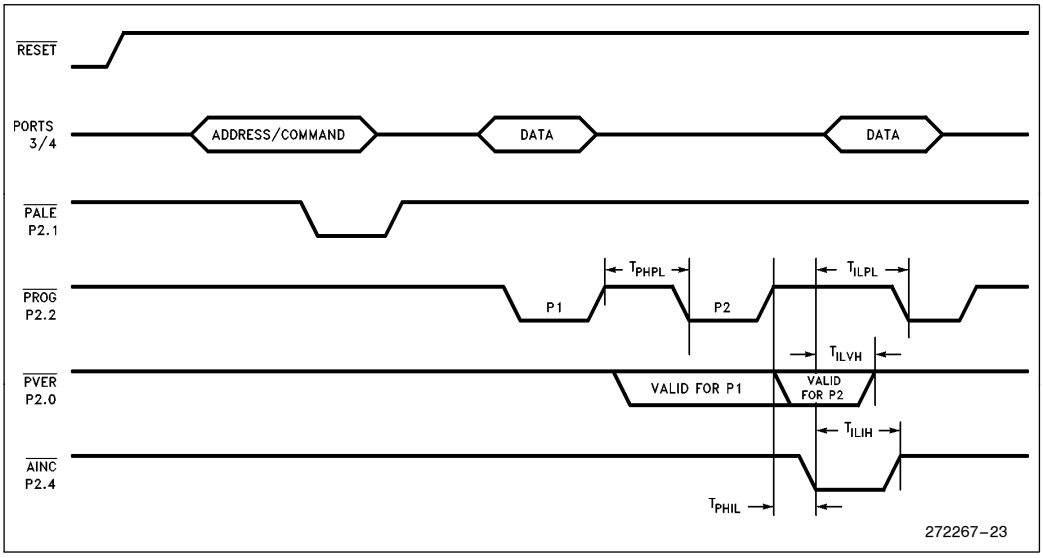
NOTE:
P3.0 must be high (''1'')

SLAVE PROGRAMMING MODE IN WORD DUMP MODE WITH AUTO INCREMENT



NOTE:
P3.0 must be low (''0'')

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



This data sheet (272267-004) applies to devices marked with a ''D'' at the end of the top side tracking number.

8XC196NT Design Considerations

1. When operating in bus timing modes 1 or 2, the upper and lower address/data lines must be latched. Even in 8-bit bus mode, the upper address lines must be latched. In modes 0 and 3, the upper address lines DO NOT NEED to be latched in 8-bit bus width mode. But in 16-bit buswidth mode the upper address lines need to be latched.

8XC196NT ERRATA see Faxback #2344

1. ILLEGAL Opcode interrupt vector.
2. Aborted Interrupt vectors to lowest priority.
3. PTS Request during Interrupt latency.

DATA SHEET REVISION HISTORY

This datasheet applies to devices marked with a ''D'' at the end of the topside tracking number. The topside tracking number consists of nine characters and is the second line on the top side of the device. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are differences between the 272267-003 and 272267-004 datasheets:

1. Changed all references of ''EPROM'' to ''OTPROM''.
2. Added all the Slave Port pins to the package diagram and pin descriptions.
3. Added $\overline{\text{INTOUT}}$ pin to pin descriptions.
4. Changed ILI1 (input leakage current for Port 0) from ± 1 μA to ± 3 μA.
5. Removed T_{LLYV} from AC characterisics and waveform diagrams.
6. T_{RLCL} in Mode 0 and 3, changed from $+4$ ns min. to -5 ns min.
7. T_{WHQX} in Mode 0 and 3, changed from $T_{OSC} - 30$ min. to $T_{OSC} - 35$ min.
8. Clarified the Ready waveform timings for Mode 0 and 3, by adding ''$+2\ T_{OSC}$*''.
9. T_{LHLL} in Mode 1, changed from $T_{OSC} - 10$ min. to $T_{OSC} - 20$ min.
10. T_{AVLL} in Mode 1, changed from $0.5\ T_{OSC} - 15$ min. to $0.5\ T_{OSC} - 20$ min.
11. T_{LLAX} in Mode 1, changed from $0.5\ T_{OSC} - 20$ min. to $0.5\ T_{OSC} - 25$ min.
12. T_{LHLL} in Mode 2, changed from $T_{OSC} - 10$ min. to $T_{OSC} - 20$ min.
13. T_{XLXL} and T_{XLXH} for the Serial Port timings were changed to reflect the minimum baudrate for receive and transmit modes.
14. Added the 8XC196NT ERRATA section.