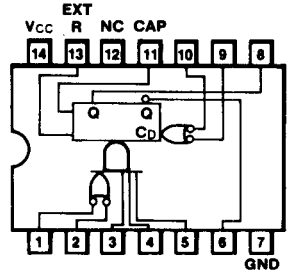
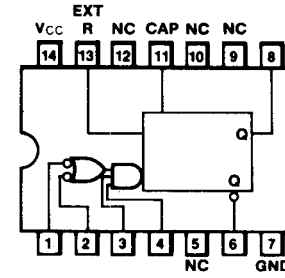
DIGITAL - TTL

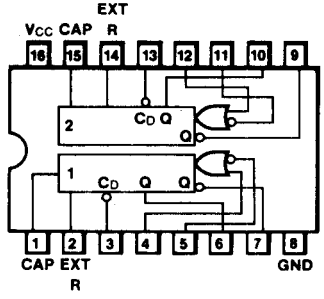
D40
9600



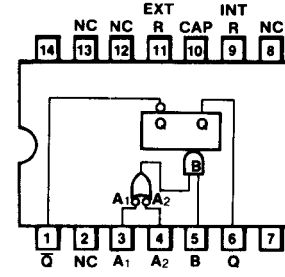
D41
9601



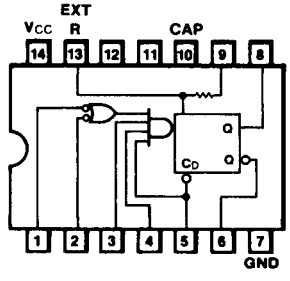
D42
9602, 96L02,
96S02, 96LS02



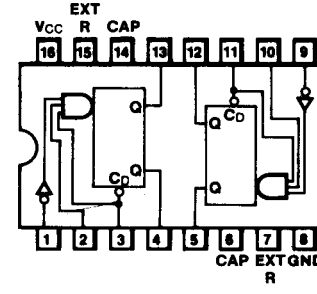
D43
9603/74121



D44
54/74122



D45
54/74123



13
(0732) 50144
Sevenoaks
Jamyn

TTL

COUNTERS (Cont'd)

Item	Function	DEVICE NO.	Modulo	Parallel Load[1]	Clock Transition	Max Clock Rate MHz (Typ)	Clock to Q Output Delay ns (Typ)	Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
1	Up/Down	**54LS[2]/74LS568**	10 Presettable	S	⌐	—	—	—	D99	9Z
2	Up/Down	**54LS[2]/74LS569**	16 Presettable	S	⌐	—	—	—	D99	9Z
3	Rate Multiplier	**54/7497**	M.f./64	—	⌐	32	20	400	D187	4L,7B,9B
4	Rate Multiplier	**54/74167**	M.f./10	—	⌐	32	20	325	D188	4L,7B,9B

MONOSTABLES (ONE-SHOTS)

Item	Function	DEVICE NO.	Pulse Width Variation (%)		No. of Inputs		Resettable	Min Output (tw) ns	Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
			vs. Temp	vs. V_{CC}	Positive	Negative					
5	Single Retriggerable	**9600**	±1.5	±1.5	3	2	X	75	125	D40	3I,6A
6	Single Retriggerable	**9601**	±2.7	±1.0	2	2	—	50	125	D41	3I,6A,9A
7	Dual Retriggerable	**9602**	±1.5	±1.5	1	1	X	72	250	D42	4L,6B,9B
8	Dual Retriggerable	**96L02**	±0.4	±1.5	1	1	X	110	50	D42	4L,6B,9B
9	Dual Retriggerable	**96S02**	±0.2	±0.2	1	1	X	27	250	D42	4L,6B,9B
10	Single Non-Retriggerable	**9603,54/74121**	±0.2	±0.15	1	2	—	40	90	D43	3I,6A,9A
11	Single Retriggerable	**54/74122**	±2.7	±1.0	2	2	X	45	115	D44	3I,6A,9A
12	Dual Retriggerable	**54/74123**	±2.7	±1.0	1	1	X	45	230	D45	4L,6B,9B
13	Dual Retriggerable	**96LS02**	±0.5	±0.7	1	1	X	35	175	D42	4L,6B,9B

1. A = asynchronous, S = synchronous
2. To be announced

(0732) 50144
Sevenoaks
Jamyn