



DESCRIPTION

A24C16 provides 16384 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 2048 words of 8 bits each.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The A24C16 is available in SOP8, TSSOP8, DFN8, DIP8 and TSOT-25 packages.

ORDERING INFORMATION

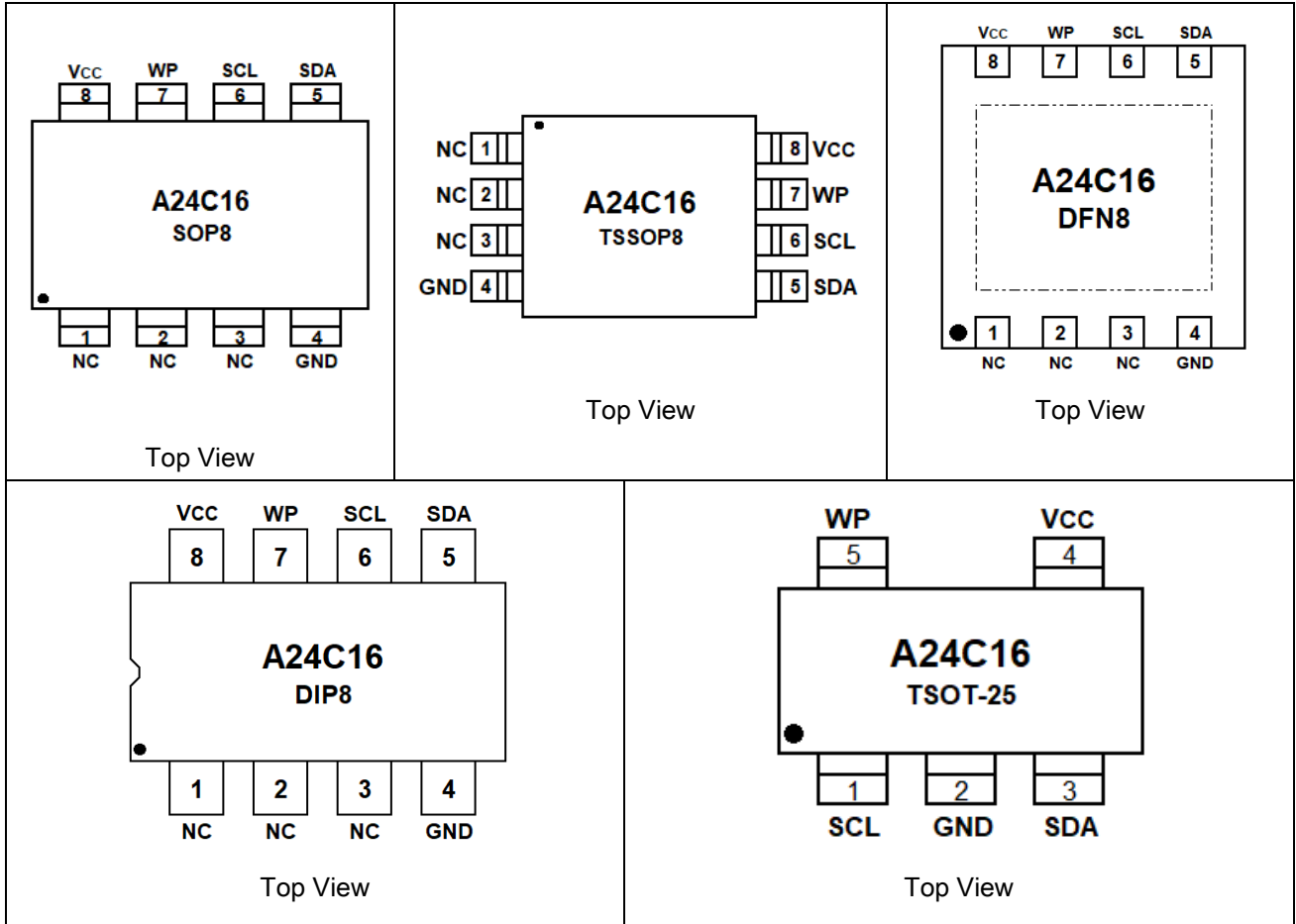
Package Type	Part Number	
SOP8 SPQ: 2,500pcs/Reel	M8	A24C16M8R
		A24C16M8VR
TSSOP8 SPQ: 3,000pcs/Reel	TMX8	A24C16TMX8R
		A24C16TMX8VR
DFN8 SPQ: 3,000pcs/Reel	J8	A24C16J8R
		A24C16J8VR
DIP8 SPQ: 50pcs/Tube	P8	A24C16P8U
		A24C16P8VU
TSOT-25 SPQ: 3,000pcs/Reel	TE5	A24C16TE5R
		A24C16TE5VR
Note	V: Halogen Free Package R: Tape & Reel U: Tube	
AiT provides all RoHS products		

FEATURES

- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
16k bits (2048 X 8) of EEPROM
Page size: 16 bytes
- Single supply voltage and high speed:1MHz
Random and sequential Read modes
- Write:
Byte Write within 3 ms
Page Write within 3 ms
Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High reliability
Endurance: 1 Million Write Cycles
Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
HBM 8000V
- Available in SOP8, TSSOP8, DFN8, DIP8 and TSOT-25 packages



PIN DESCRIPTION



Pin #					Symbol	Type	Functions
SOP8	TSSOP8	DFN8	DIP8	TSOT-25			
1	1	1	1	-	NC	I	Not connected
2	2	2	2	-	NC	I	Not connected
3	3	3	3	-	NC	I	Not connected
4	4	4	4	2	GND	P	Ground
5	5	5	5	3	SDA	I/O	Serial Data
6	6	6	6	1	SCL	I	Serial Clock Input
7	7	7	7	5	WP	I	Write Protect
8	8	8	8	4	Vcc	P	Power Supply



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V ~ +6.5V
Input / Output Voltage	GND-0.3V ~ V _{CC} +0.3V
Operating Ambient Temperature	-40°C~ +85°C
Storage Temperature	-65°C ~ +150°C
Electrostatic Pulse (Human Body Model)	8000V

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

Applicable over recommended operating range from: T_A = 25°C, f = 1.0MHz, V_{CC} = +1.7V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input / Output Capacitance (SDA)	C _{I/O}	V _{I/O} =0V	-	-	8	pF
Input Capacitance (A1, A2, SCL)	C _{IN}	V _{IN} =0V	-	-	6	pF



DC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range from: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$, unless otherwise noted

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC1}	@400kHz	1.7	-	5.5	V
Supply Voltage	V_{CC2}	@1MHz	2.5	-	5.5	V
Supply Current $V_{CC} = 5.0\text{V}$	I_{CC1}	Read at 400kHz	-	0.14	0.3	mA
Supply Current $V_{CC} = 5.0\text{V}$	I_{CC2}	Write at 400kHz	-	0.28	0.5	mA
Supply Current $V_{CC} = 5.0\text{V}$	I_{SB1}	$V_{IN} = V_{CC}$ or V_{SS}	-	0.03	0.5	μA
Input Leakage Current	I_{LI}	$V_{IN} = V_{CC}$ or V_{SS}	-	0.10	1.0	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{CC}$ or V_{SS}	-	0.05	1.0	μA
Input Low Level	V_{IL1}	$V_{CC} = 1.7\text{V}$ to 5.5V	-0.3	-	$V_{CC} \times 0.3$	V
Input High Level	V_{IH1}	$V_{CC} = 1.7\text{V}$ to 5.5V	$V_{CC} \times 0.7$	-	$V_{CC} + 0.3$	V
Output Low Level $V_{CC} = 1.7\text{V}$	V_{OL1}	$I_{OL} = 0.15\text{mA}$	-	-	0.2	V
Output Low Level $V_{CC} = 5.0\text{V}$	V_{OL2}	$I_{OL} = 3.0\text{mA}$	-	-	0.4	V

AC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range from: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$, $C_L = 1$ TTL Gate and 100pF , unless otherwise noted

Parameter	Symbol	$1.7\text{V} \leq V_{CC} < 2.5\text{V}$			$2.5\text{V} \leq V_{CC} < 5.5\text{V}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	f_{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	1.3	-	-	0.5	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.26	-	-	μs
Noise Suppression Time	t_i	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	-	-	0.9	-	-	0.45	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.3	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD,STA}$	0.6	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU,STA}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD,DAT}$	0	-	-	0	-	-	μs
Data In Setup Time	$t_{SU,DAT}$	100	-	-	100	-	-	ns
Inputs Rise Time ^{NOTE1}	t_R	-	-	0.3	-	-	0.12	μs
Inputs Fall Time ^{NOTE1}	t_F	-	-	0.3	-	-	0.12	μs
Stop Setup Time	$t_{SU,STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	1.9	3	-	1.9	3	ms
5.0V, 25°C, Byte Mode ^{NOTE1}	Endurance	1M	-	-	1M	-	-	Write Cycles

NOTE1: This parameter is characterized and is not 100% tested.

NOTE2: AC measurement conditions: R_L (connects to V_{CC}): $1.3\text{k}\Omega$

Input pulse voltages: $0.3 V_{CC}$ to $0.7 V_{CC}$

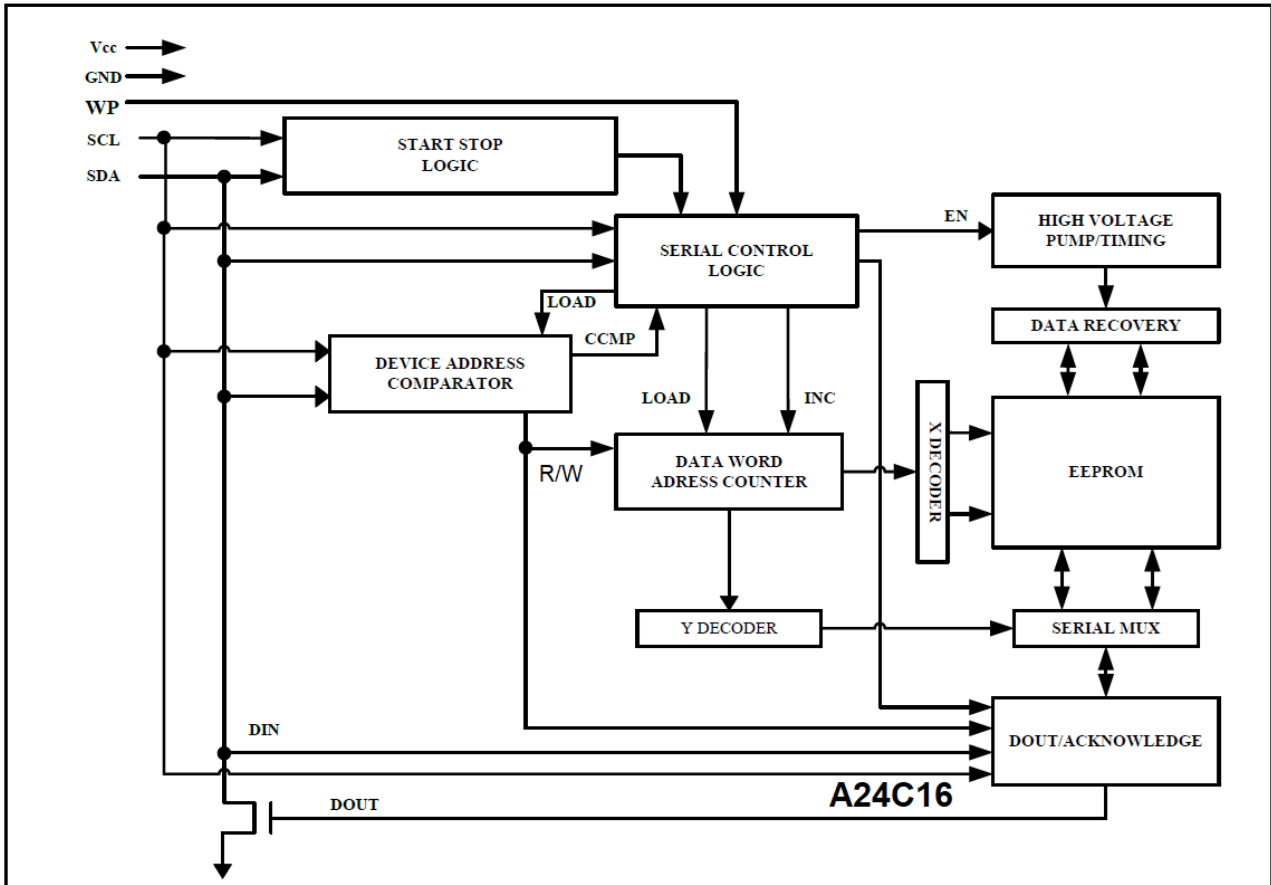
Input rise and fall time: 50ns

Input and output timing reference voltages: $0.5 V_{CC}$

The value of R_L should be concerned according to the actual loading on the user's system.



BLOCK DIAGRAM





DETAILED INFORMATION

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The A24C16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected and operates as shown in the following and operates as shown in the following Table 1.

Table1: Write Protect

WP Pin Status	A24C16
At V _{CC}	Full Array
At GND	Normal Read/Write Operations



FUNCTIONAL DESCRIPTION

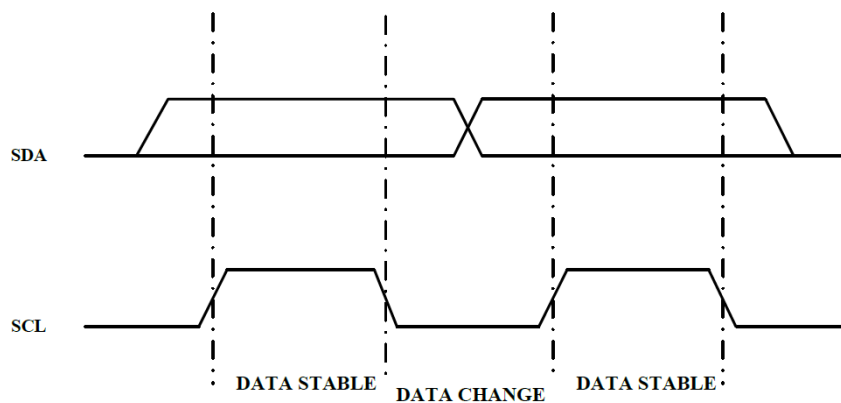
1. Memory Organization

A24C16, 16k SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16k requires an 11-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

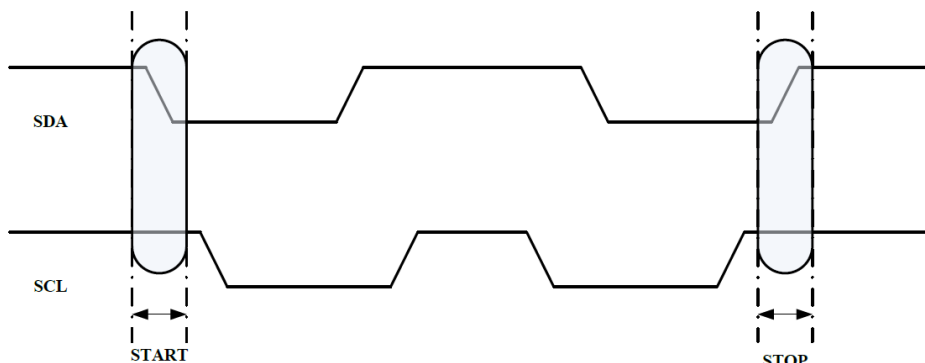
Figure 1 Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2).

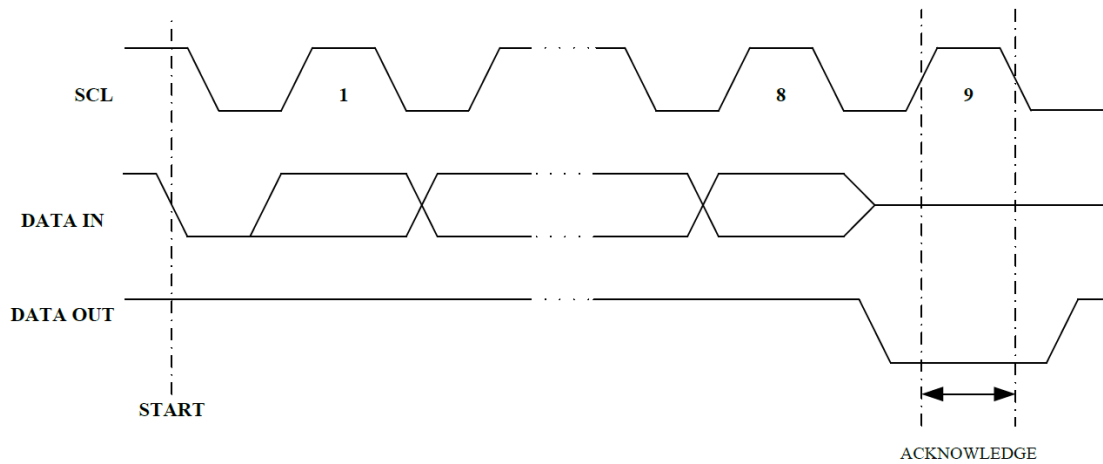
Figure 2 Start and Stop Definition





ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 3 Output Acknowledge



STANDBY MODE: The A24C16 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

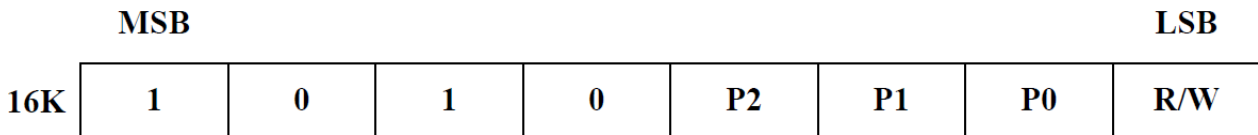
1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.



3. Device Addressing

The 16k EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4).

Figure 4 Device Address



The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 16k does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4k, 8k and 16k devices should be considered the most significant bits of the data word address which follows.

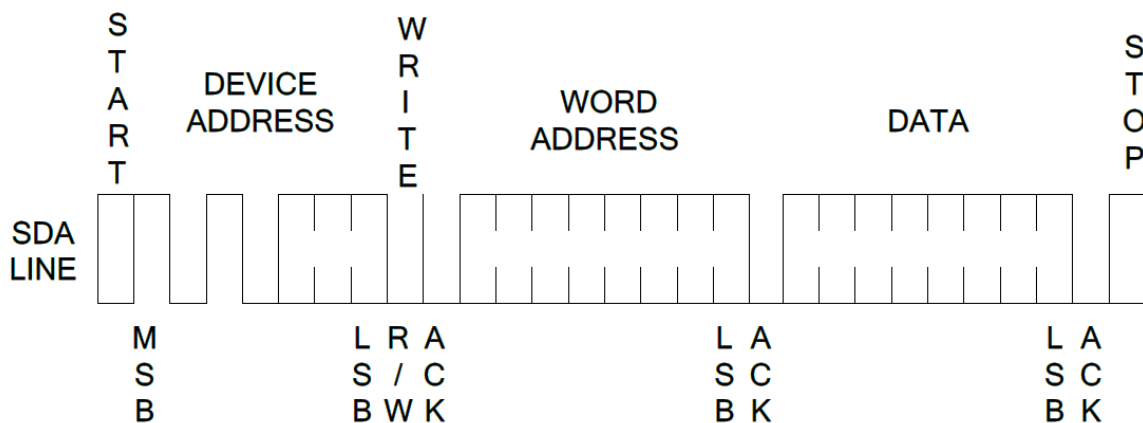
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

4. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

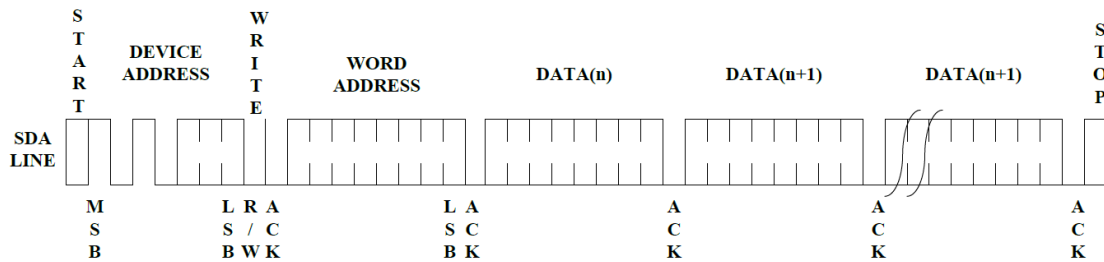
Figure 5 Byte Write





PAGE WRITE: The 16k EEPROM is capable of 16-byte page writes. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6).

Figure 6 Page Write



The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

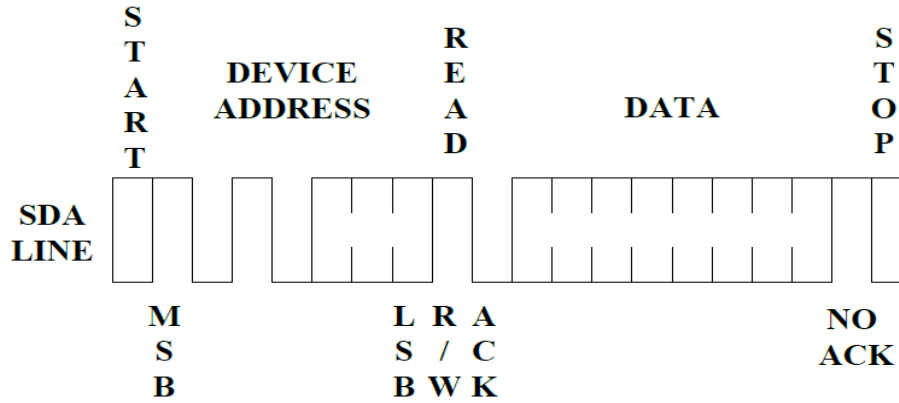
5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

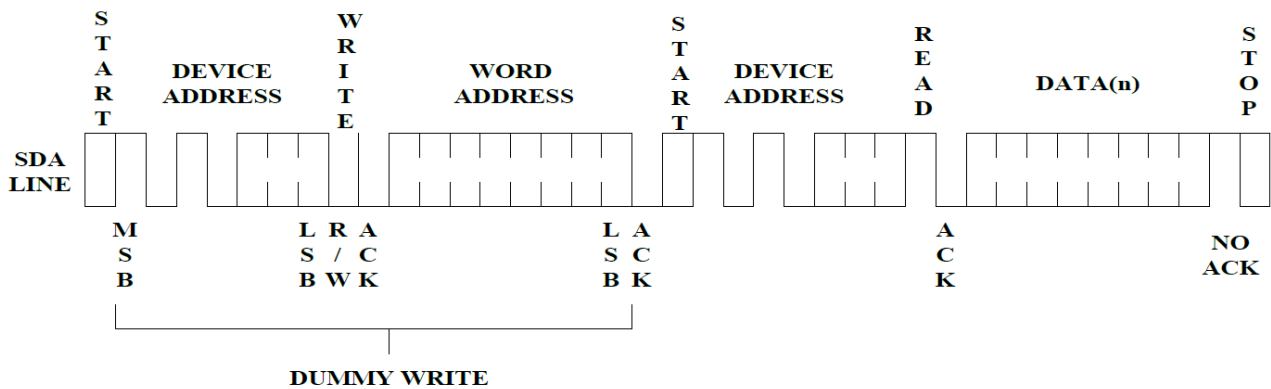


Figure 7 Current Address Read



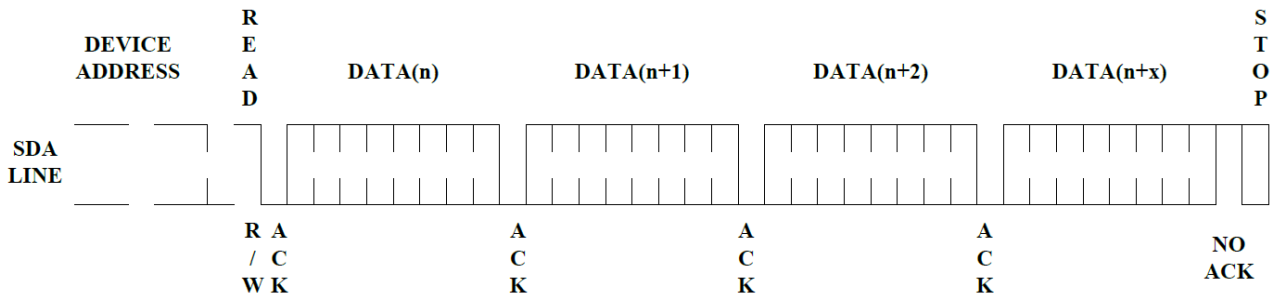
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8)

Figure 8 Random Read



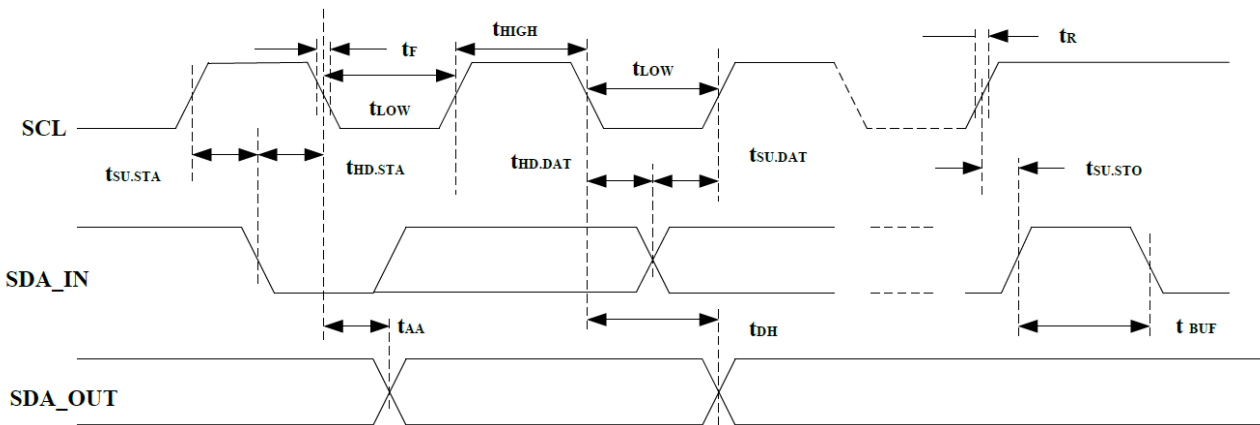
SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9).

Figure 9 Sequential Read



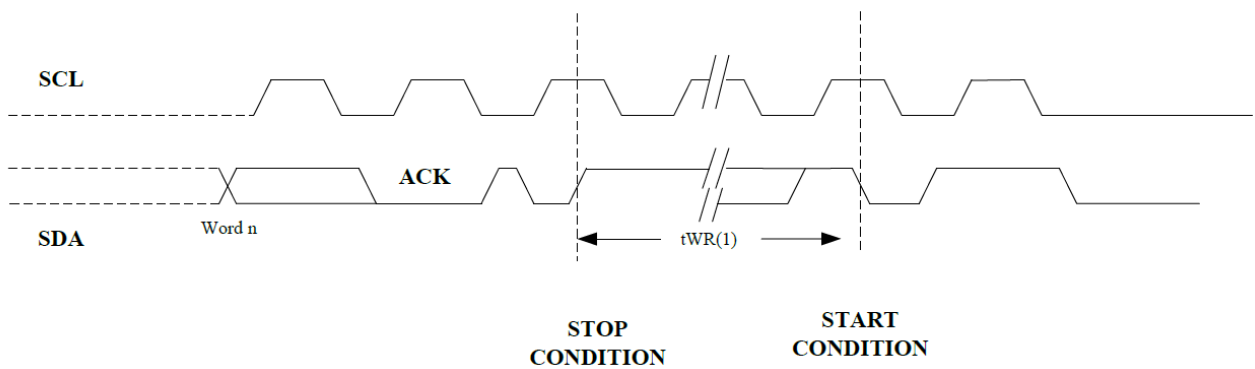
BUS TIMING

Figure 10 SCL: Serial Clock, SDA: Serial Data I/O



WRITE CYCLE TIMING

Figure 11 SCL: Serial Clock, SDA: Serial Data I/O

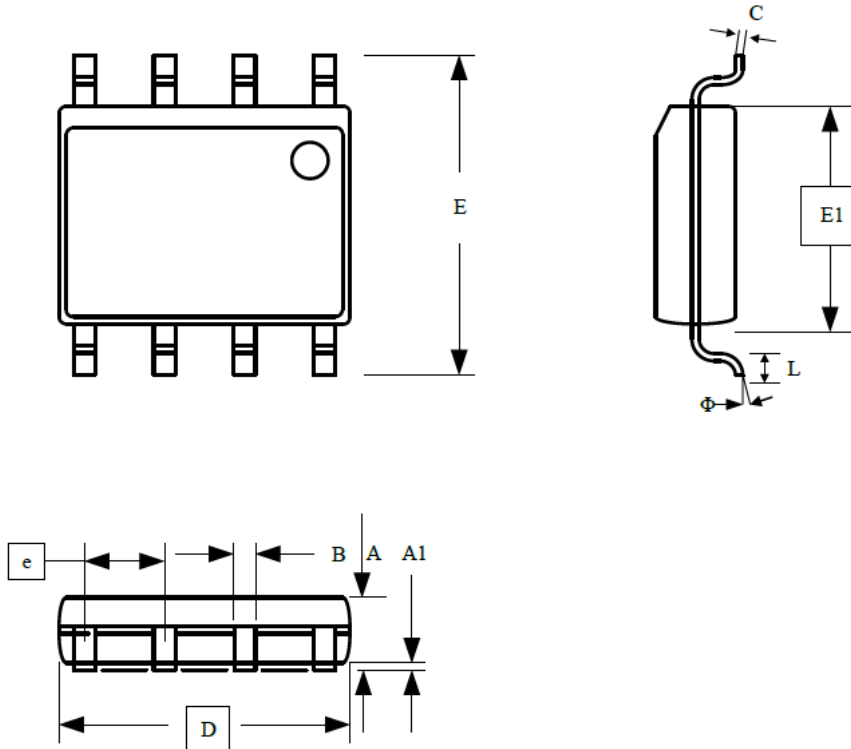


NOTE: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.



PACKAGE INFORMATION

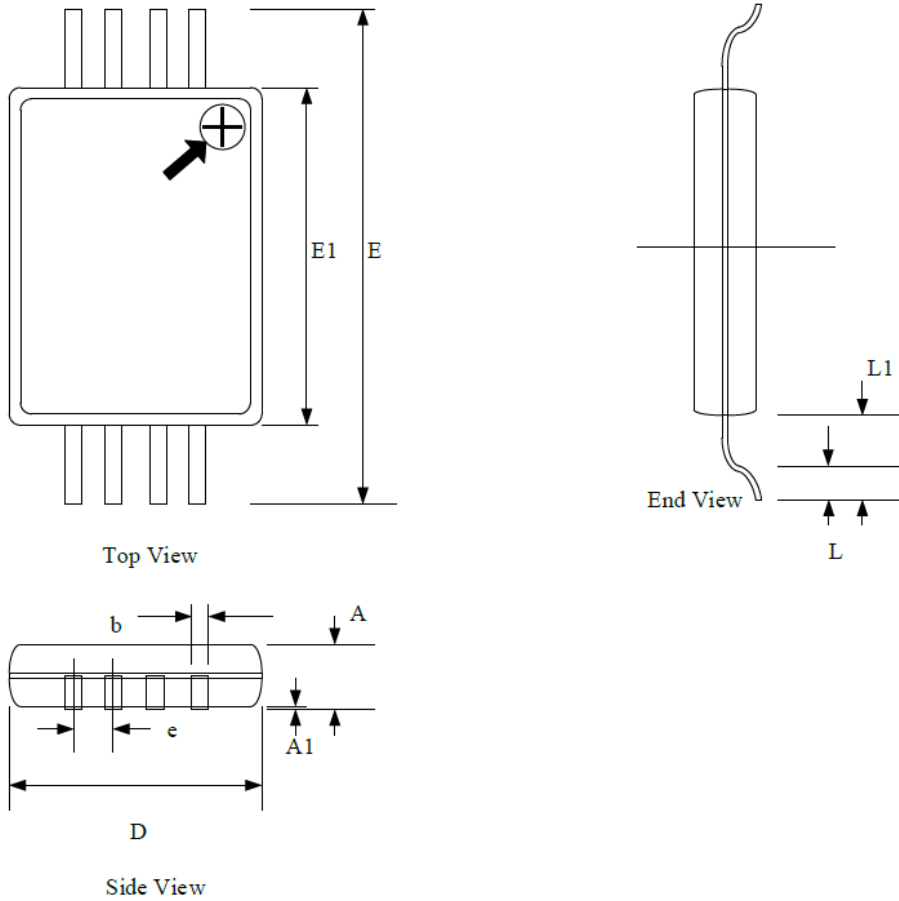
Dimension in SOP8 (Unit: mm)



Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.23
B	0.39	0.48
C	0.21	0.26
D	4.70	5.10
E1	3.70	4.10
E	5.80	6.20
e	1.27BSC	
L	0.50	0.80
θ	0°	8°



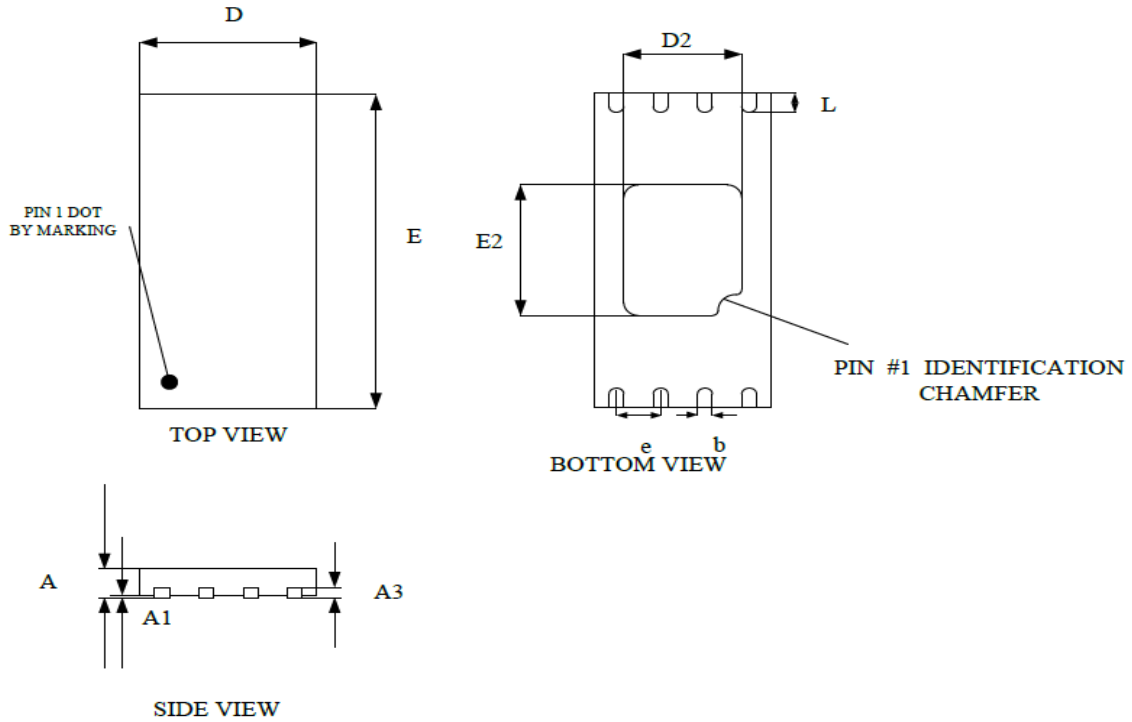
Dimension in TSSOP8 Package (Unit: mm)



Symbol	Min	Max
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
A	-	1.20
A1	0.05	0.15
b	0.21	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	



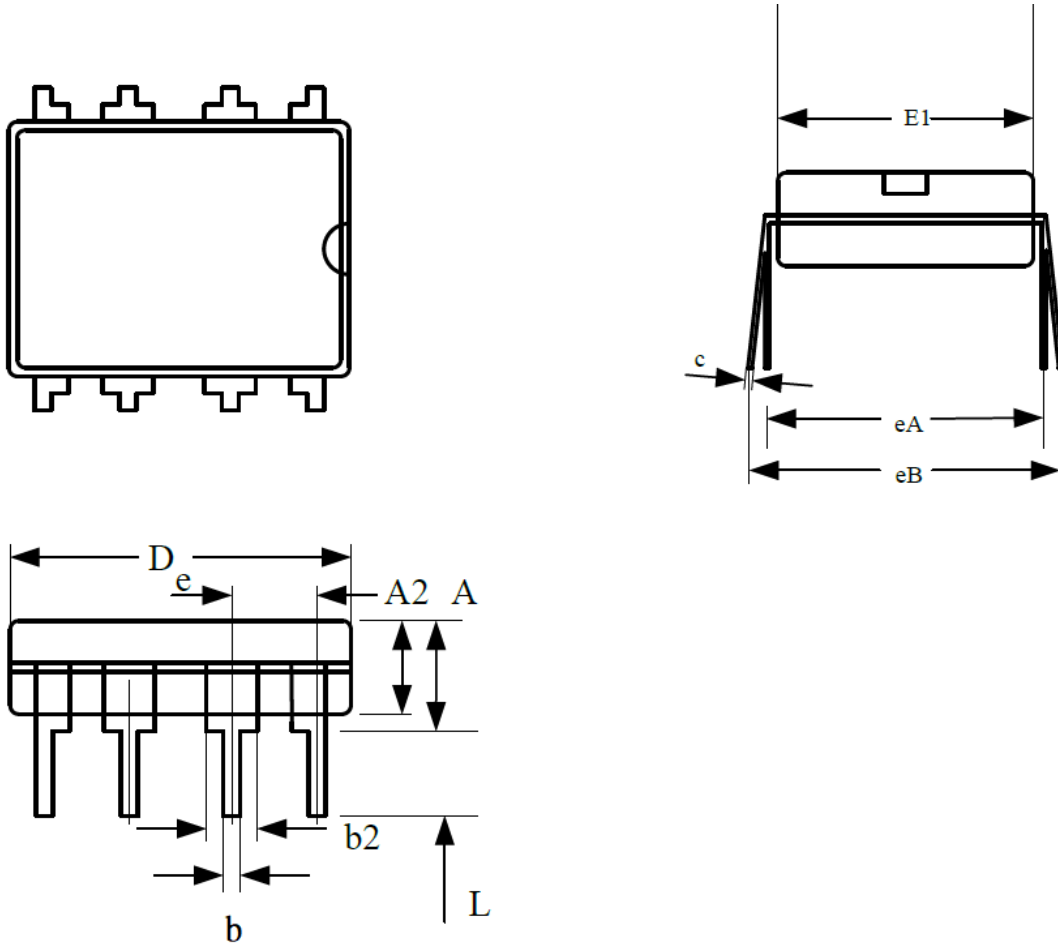
Dimension in DFN8 (Unit: mm)



Symbol	Min	Max
A	0.50	0.60
A1	0.00	0.05
A3	0.15 REF	
D	1.95	2.05
E	2.95	3.05
b	0.20	0.30
L	0.20	0.40
D2	1.25	1.50
E2	1.15	1.40
e	0.50 BSC	



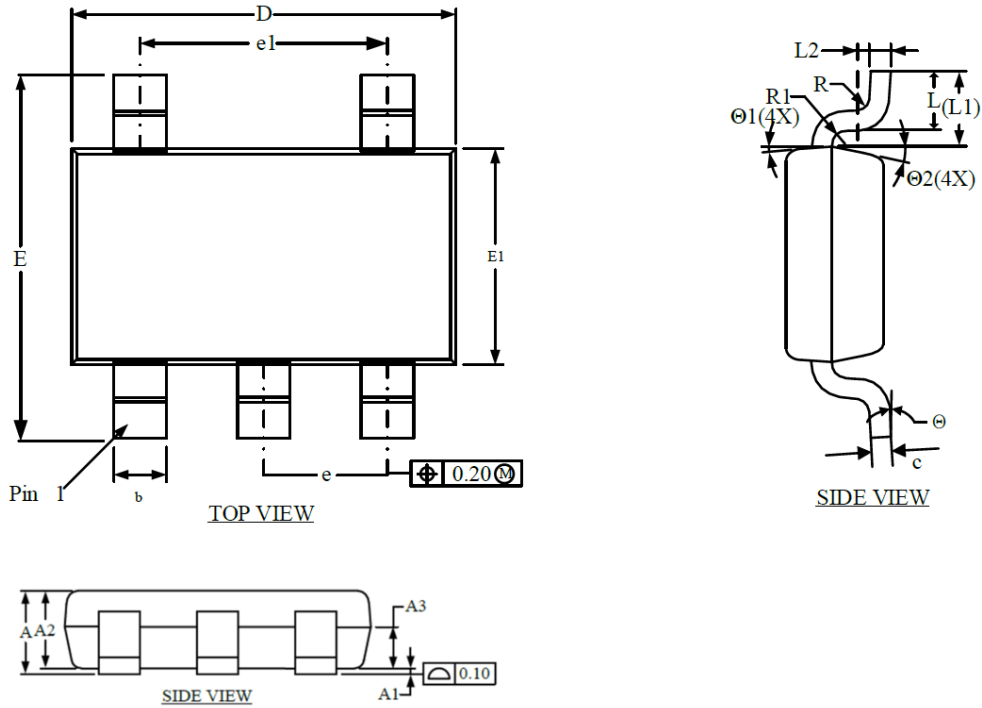
Dimension in DIP8 (Unit: inches)



Symbol	Min	Max
A	3.60	4.00
A2	3.20	3.40
b	0.44	0.53
b2	1.52 BSC	
c	0.24	0.32
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.30
L	3.00 BSC	



Dimension in TSOT-25 (Unit: mm)



Symbol	Min	Max
A	-	0.90
A1	0.00	0.10
A2	0.65	0.85
A3	0.35	0.45
b	0.30	0.50
c	0.14	0.20
D	2.85	3.05
E	2.65	2.95
E1	1.60	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60
L1	0.575REF	
L2	0.258BSC	
R	-	0.25
R1	-	0.25
θ	0°	8°
θ1	3°	7°
θ2	10°	14°



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