

ProASIC3 Flash Family FPGAs

with Optional Soft ARM[®] Support



Features and Benefits

High Capacity

- 15 k to 1 M System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live at Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance

- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI[†]

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except ARM-enabled ProASIC[®]3 devices) via JTAG (IEEE 1532-compliant)[†]
- FlashLock[®] to Secure FPGA Contents

Low Power

- Core Voltage for Low Power
- Support for 1.5 V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (A3P250 and above)

- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X[†] and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (A3P250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparring I/Os[†]
- Programmable Output Slew Rate[†] and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC3 Family

Clock Conditioning Circuit (CCC) and PLL[†]

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback
- Wide Input Frequency Range (1.5 MHz to 350 MHz)

Embedded Memory[†]

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (x1, x2, x4, x9, and x18 organizations)[†]
- True Dual-Port SRAM (except x18)

ARM Processor Support in ProASIC3 FPGAs

- M1 and M7 ProASIC3 Devices—Cortex-M1 and CoreMP7 Soft Processor Available with or without Debug

ProASIC3 Product Family

| ProASIC3 Devices | A3P015 | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|--------------------------------|--------|--------|--------|--------|------------------------|---------------|---------------|---------------|
| ARM7 Devices ¹ | | | | | | | | M7A3P1000 |
| Cortex-M1 Devices ¹ | | | | | M1A3P250 | M1A3P400 | M1A3P600 | M1A3P1000 |
| System Gates | 15 k | 30 k | 60 k | 125 k | 250 k | 400 k | 600 k | 1 M |
| Typical Equivalent Macrocells | 128 | 256 | 512 | 1,024 | – | – | – | – |
| VersaTiles (D-flip-flops) | 384 | 768 | 1,536 | 3,072 | 6,144 | 9,216 | 13,824 | 24,576 |
| RAM kbits (1,024 bits) | – | – | 18 | 36 | 36 | 54 | 108 | 144 |
| 4,608-Bit Blocks | – | – | 4 | 8 | 8 | 12 | 24 | 32 |
| FlashROM Bits | 1 k | 1 k | 1 k | 1 k | 1 k | 1 k | 1 k | 1 k |
| Secure (AES) ISP ² | – | – | Yes | Yes | Yes | Yes | Yes | Yes |
| Integrated PLL in CCCs | – | – | 1 | 1 | 1 | 1 | 1 | 1 |
| VersaNet Globals ³ | 6 | 6 | 18 | 18 | 18 | 18 | 18 | 18 |
| I/O Banks | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 4 |
| Maximum User I/Os | 49 | 81 | 96 | 133 | 157 | 194 | 235 | 300 |
| Package Pins | | | | | | | | |
| QFN | QN68 | QN132 | QN132 | QN132 | QN132 ⁵ | | | |
| VQFP | | VQ100 | VQ100 | VQ100 | VQ100 | | | |
| TQFP | | | TQ144 | TQ144 | | | | |
| PQFP | | | | PQ208 | PQ208 | PQ208 | PQ208 | PQ208 |
| FBGA | | | FG144 | FG144 | FG144/256 ⁵ | FG144/256/484 | FG144/256/484 | FG144/256/484 |

Notes:

1. Refer to the [CoreMP7 datasheet](#) or [Cortex-M1 product brief](#) for more information.
2. AES is not available for ARM-enabled ProASIC3 devices.
3. Six chip (main) and three quadrant global networks are available for A3P060 and above.
4. For higher densities and support of additional features, refer to the [ProASIC3E Flash Family FPGAs handbook](#).
5. The M1A3P250 device does not support this package.

[†] A3P015 and A3P030 devices do not support this feature.

[‡] Supported only by A3P015 and A3P030 devices.

I/Os Per Package ¹

| ProASIC3 Devices | A3P015 | A3P030 | A3P060 | A3P125 | A3P250 ³ | A3P400 ³ | A3P600 | A3P1000 | | | | |
|-------------------|------------------|------------------|------------------|------------------|-------------------------------|------------------------|-------------------------------|------------------------|-------------------------------|------------------------|-------------------------------|------------------------|
| ARM7 Devices | | | | | | | | M7A3P1000 | | | | |
| Cortex-M1 Devices | | | | | M1A3P250 ^{3,6} | M1A3P400 ³ | M1A3P600 | M1A3P1000 | | | | |
| Package | I/O Type | | | | | | | | | | | |
| | Single-Ended I/O | Single-Ended I/O | Single-Ended I/O | Single-Ended I/O | Single-Ended I/O ² | Differential I/O Pairs | Single-Ended I/O ² | Differential I/O Pairs | Single-Ended I/O ² | Differential I/O Pairs | Single-Ended I/O ² | Differential I/O Pairs |
| QN68 | 49 | - | - | - | - | - | - | - | - | - | - | - |
| QN132 | - | 81 | 80 | 84 | 87 | 19 | - | - | - | - | - | - |
| VQ100 | - | 77 | 71 | 71 | 68 | 13 | - | - | - | - | - | - |
| TQ144 | - | - | 91 | 100 | - | - | - | - | - | - | - | - |
| PQ208 | - | - | - | 133 | 151 | 34 | 151 | 34 | 154 | 35 | 154 | 35 |
| FG144 | - | - | 96 | 97 | 97 | 24 | 97 | 25 | 97 | 25 | 97 | 25 |
| FG256 | - | - | - | - | 157 | 38 | 178 | 38 | 177 | 43 | 177 | 44 |
| FG484 | - | - | - | - | - | - | 194 | 38 | 235 | 60 | 300 | 74 |

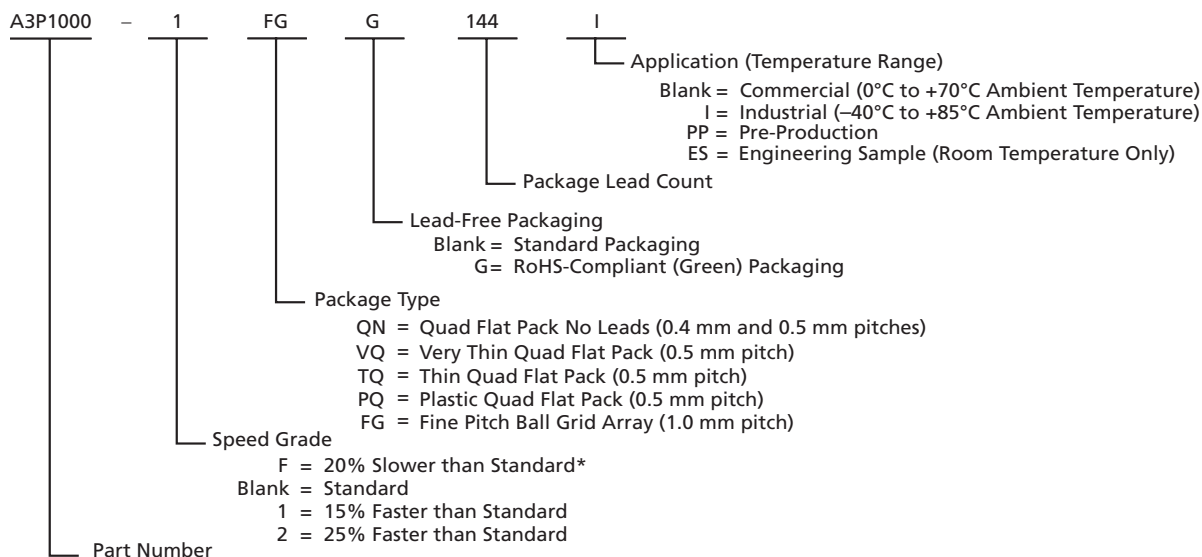
Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3 Flash Family FPGAs handbook](#) to ensure complying with design and board migration requirements.
2. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
3. For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15. Refer to the [ProASIC3 Flash Family FPGAs handbook](#) for position assignments of the 15 LVPECL pairs.
4. FG256 and FG484 are footprint-compatible packages.
5. "G" indicates RoHS-compliant packages. Refer to "[ProASIC3 Ordering Information](#)" on page III for the location of the "G" in the part number.
6. The M1A3P250 device does not support FG256 or QN132 packages.

Table 1-1 • ProASIC3 FPGAs Package Sizes Dimensions

| Package | QN68 | QN132 | VQ100 | TQ144 | PQ208 | FG144 | FG256 | FG484 |
|---------------------------------|-------|-------|---------|---------|---------|---------|---------|---------|
| Length x Width (mm\mm) | 8 x 8 | 8 x 8 | 14 x 14 | 20 x 20 | 28 x 28 | 13 x 13 | 17 x 17 | 23 x 23 |
| Nominal Area (mm ²) | 64 | 64 | 196 | 400 | 784 | 169 | 289 | 529 |
| Pitch (mm) | 0.4 | 0.5 | 0.5 | 0.5 | 0.5 | 1.0 | 1.0 | 1.0 |
| Height (mm) | 0.90 | 0.75 | 1.00 | 1.40 | 3.40 | 1.45 | 1.60 | 2.23 |

ProASIC3 Ordering Information



ProASIC3 Devices

A3P015 = 15,000 System Gates
 A3P030 = 30,000 System Gates
 A3P060 = 60,000 System Gates
 A3P125 = 125,000 System Gates
 A3P250 = 250,000 System Gates
 A3P400 = 400,000 System Gates
 A3P600 = 600,000 System Gates
 A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with ARM7

M7A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with Cortex-M1

M1A3P250 = 250,000 System Gates
 M1A3P400 = 400,000 System Gates
 M1A3P600 = 600,000 System Gates
 M1A3P1000 = 1,000,000 System Gates

* The DC and switching characteristics for the -F speed grade targets are based only on simulation. The characteristics provided for the -F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The -F speed grade is only supported in the commercial temperature range.

Temperature Grade Offerings

| Package | A3P015 | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|-------------------|--------|--------|--------|--------|----------|----------|----------|-----------|
| ARM7 Devices | | | | | | | | M7A3P1000 |
| Cortex-M1 Devices | | | | | M1A3P250 | M1A3P400 | M1A3P600 | M1A3P1000 |
| QN68 | C, I | - | - | - | - | - | - | - |
| QN132 | - | C, I | C, I | C, I | C, I | - | - | - |
| VQ100 | - | C, I | C, I | C, I | C, I | - | - | - |
| TQ144 | - | - | C, I | C, I | - | - | - | - |
| PQ208 | - | - | - | C, I | C, I | C, I | C, I | C, I |
| FG144 | - | - | C, I | C, I | C, I | C, I | C, I | C, I |
| FG256 | - | - | - | - | C, I | C, I | C, I | C, I |
| FG484 | - | - | - | - | - | C, I | C, I | C, I |

Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature
2. I = Industrial temperature range: -40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

| Temperature Grade | -F ¹ | Std. | -1 | -2 |
|-------------------|-----------------|------|----|----|
| C ² | ✓ | ✓ | ✓ | ✓ |
| I ³ | - | ✓ | ✓ | ✓ |

Notes:

1. The DC and switching characteristics for the -F speed grade targets are based only on simulation. The characteristics provided for the -F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The -F speed grade is only supported in the commercial temperature range.
2. C = Commercial temperature range: 0°C to 70°C ambient temperature
3. I = Industrial temperature range: -40°C to 85°C ambient temperature

References made to ProASIC3 devices also apply to ARM-enabled ProASIC3 devices. The ARM-enabled part numbers start with M7 (CoreMP7) and M1 (Cortex-M1).

Contact your local Actel representative for device availability: <http://www.actel.com/contact/default.aspx>.

A3P015 and A3P030

The A3P015 and A3P030 are architecturally compatible; there are no RAM or PLL features.

1 – ProASIC3 Device Family Overview

General Description

ProASIC3, the third-generation family of Actel flash FPGAs, offers performance, density, and features beyond those of the ProASIC^{PLUS} family. Nonvolatile flash technology gives ProASIC3 devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The A3P015 and A3P030 devices have no PLL or RAM support. ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

ProASIC3 devices support the ARM7 soft IP core and Cortex-M1 devices. The ARM-enabled devices have Actel ordering numbers that begin with M7A3P (CoreMP7) and M1A3P (Cortex-M1) and do not support AES decryption.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3 devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3 devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3 device cannot be read back, although secure design verification is possible.

ARM-enabled ProASIC3 devices do not support user-controlled AES security mechanisms. Since the ARM core must be protected at all times, AES encryption is always on for the core logic, so bitstreams are always encrypted. There is no user access to encryption for the FlashROM programming data.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A ProASIC3 device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based ProASIC3 devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

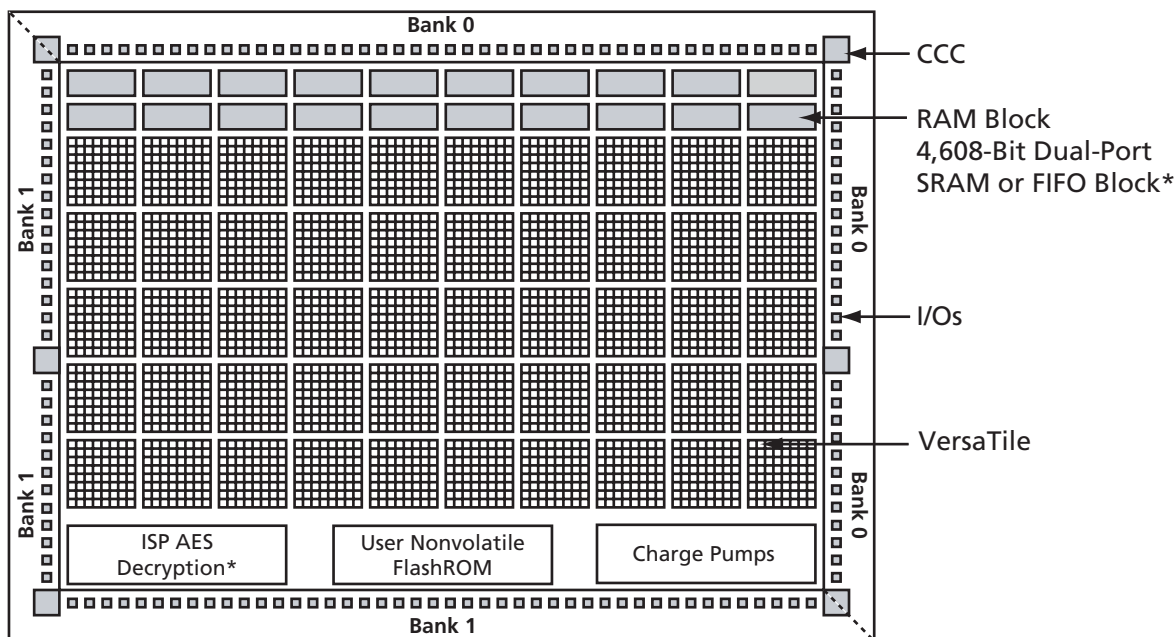
Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVC MOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure



* Not supported by A3P015 and A3P030 devices

Figure 1-1 • ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)

[†] The A3P015 and A3P030 do not support PLL or SRAM.

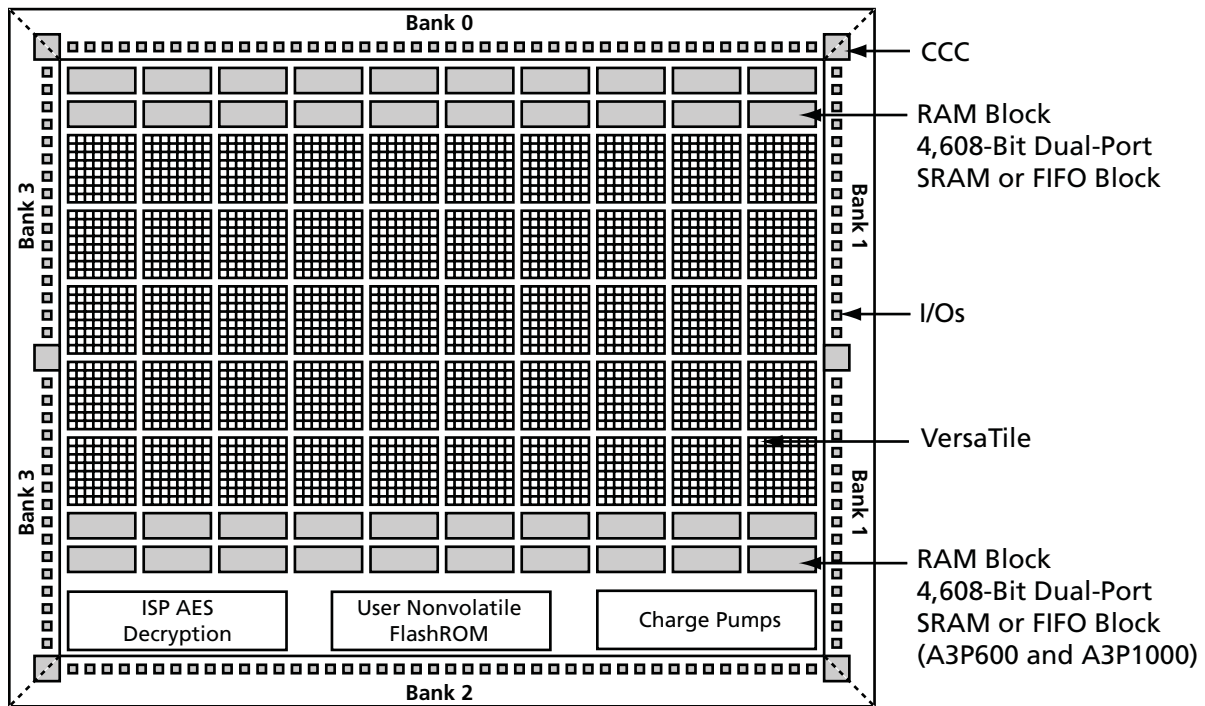


Figure 1-2 • ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250, A3P600, and A3P1000)

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3 devices via an IEEE 1532 JTAG interface.

VersaTiles

The ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

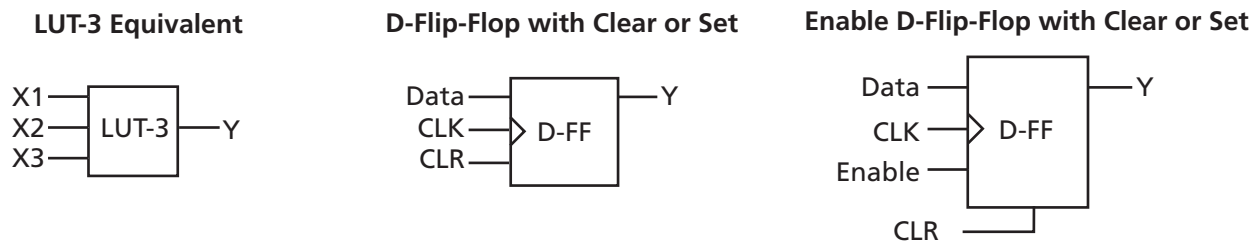


Figure 1-3 • VersaTile Configurations

User Nonvolatile FlashROM

Actel ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3 development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from -7.56 ns to $+11.12$ ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0° , 90° , 180° , and 270° . Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = $50\% \pm 1.5\%$ or better (for PLL only)
- Low output jitter: worst case $< 2.5\% \times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = $300 \mu\text{s}$ (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of $40 \text{ ps} \times (350 \text{ MHz} / f_{OUT_CCC})$ (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Part Number and Revision Date

Part Number 51700097-001-1

Revised February 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v1.0) | Page |
|----------------------------------|---|------|
| 51700097-001-1 | This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | |
| 51700097-001-0 (January 2008) | This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated: "Features and Benefits" "ProASIC3 Ordering Information" "Temperature Grade Offerings" "ProASIC3 Product Family" "A3P015 and A3P030" note "Introduction and Overview" | N/A |
| | The "ProASIC3 FPGAs Package Sizes Dimensions" table is new. | II |
| | In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | III |
| | In the "General Description" section, the number of I/Os was updated from 288 to 300. | 1-1 |
| v2.2 (July 2007) | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700097-001-0. | N/A |

| Previous Version | Changes in Current Version (v1.0) | Page | | | | | | | |
|---------------------------------|--|---------------------|---------|-----------------|-------|-----------------|-------|---------|-------|
| v2.1 (May 2007) | The M7 and M1 device part numbers have been updated in Table 1 • ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix". | i, ii, iii, iii, iv | | | | | | | |
| | The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections. | iii, iii, iv | | | | | | | |
| v2.0 (April 2007) | In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz). | i | | | | | | | |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | i | | | | | | | |
| | In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated. | ii | | | | | | | |
| Advance v0.7 (January 2007) | In the "Packaging Tables", Ambient was deleted. | ii | | | | | | | |
| | Ambient was deleted from the "Speed Grade and Temperature Grade Matrix". | iv | | | | | | | |
| Advance v0.6 (April 2006) | In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77. | ii | | | | | | | |
| Advance v0.5 (January 2006) | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A | | | | | | | |
| | The term flow-through was changed to pass-through. | N/A | | | | | | | |
| | Table 1 was updated to include the QN132. | ii | | | | | | | |
| | The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated. | ii | | | | | | | |
| | "Automotive ProASIC3 Ordering Information" was updated with the QN132. | iii | | | | | | | |
| | "Temperature Grade Offerings" was updated with the QN132. | iii | | | | | | | |
| Advance v0.4 (November 2005) | The "I/Os Per Package" table was updated for the following devices and packages: | ii | | | | | | | |
| | <table border="0"> <thead> <tr> <th>Device</th> <th>Package</th> </tr> </thead> <tbody> <tr> <td>A3P250/M7ACP250</td> <td>VQ100</td> </tr> <tr> <td>A3P250/M7ACP250</td> <td>FG144</td> </tr> <tr> <td>A3P1000</td> <td>FG256</td> </tr> </tbody> </table> | Device | Package | A3P250/M7ACP250 | VQ100 | A3P250/M7ACP250 | FG144 | A3P1000 | FG256 |
| Device | Package | | | | | | | | |
| A3P250/M7ACP250 | VQ100 | | | | | | | | |
| A3P250/M7ACP250 | FG144 | | | | | | | | |
| A3P1000 | FG256 | | | | | | | | |
| Advance v0.3 | M7 device information is new. | N/A | | | | | | | |
| | The I/O counts in the "I/Os Per Package" table were updated. | ii | | | | | | | |
| Advance v0.2 | The "I/Os Per Package" table was updated. | ii | | | | | | | |

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

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The Actel products described in this advance status document may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.



2 – ProASIC3 DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2](#) on [page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

| Symbol | Parameter | Limits | Units |
|-------------------------------|-------------------------------------|---|-------|
| V _{CC} | DC core supply voltage | –0.3 to 1.65 | V |
| V _{JTAG} | JTAG DC voltage | –0.3 to 3.75 | V |
| V _{PUMP} | Programming voltage | –0.3 to 3.75 | V |
| V _{CCPLL} | Analog power supply (PLL) | –0.3 to 1.65 | V |
| V _{CCI} | DC I/O output buffer supply voltage | –0.3 to 3.75 | V |
| V _{MV} | DC I/O input buffer supply voltage | –0.3 to 3.75 | V |
| V _I | I/O input voltage | –0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V _{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| T _{STG} ² | Storage temperature | –65 to +150 | °C |
| T _J ² | Junction temperature | +125 | °C |

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4](#) on [page 2-3](#).
2. For flash programming and retention maximum limits, refer to [Table 2-3](#) on [page 2-2](#), and for recommended operating limits, refer to [Table 2-2](#) on [page 2-2](#).

Table 2-2 • Recommended Operating Conditions ¹

| Symbol | Parameter | Commercial | Industrial | Units | |
|---------------------------------------|-------------------------------------|-------------------------|---------------------------|--------------|---|
| T _A | Ambient temperature | 0 to +70 ^{4,6} | -40 to +85 ^{5,6} | °C | |
| V _{CC} | 1.5 V DC core supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| V _{JTAG} | JTAG DC voltage | 1.4 to 3.6 | 1.4 to 3.6 | V | |
| V _{PUMP} | Programming voltage | Programming Mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation ³ | 0 to 3.6 | 0 to 3.6 | V |
| V _{CCPLL} | Analog power supply (PLL) | 1.4 to 1.6 | 1.4 to 1.6 | V | |
| V _{CCI} and VMV ² | 1.5 V DC supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| | 1.8 V DC supply voltage | 1.7 to 1.9 | 1.7 to 1.9 | V | |
| | 2.5 V DC supply voltage | 2.3 to 2.7 | 2.3 to 2.7 | V | |
| | 3.3 V DC supply voltage | 3.0 to 3.6 | 3.0 to 3.6 | V | |
| | LVDS/B-LVDS/M-LVDS differential I/O | 2.375 to 2.625 | 2.375 to 2.625 | V | |
| | LVPECL differential I/O | 3.0 to 3.6 | 3.0 to 3.6 | V | |

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19. VMV and V_{CCI} should be at the same voltage within a given I/O bank.
3. V_{PUMP} can be left floating during operation (not programming mode).
4. Maximum T_J = 85°C.
5. Maximum T_J = 100°C.
6. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature ¹

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature T _{STG} (°C) ² | Maximum Operating Junction Temperature T _J (°C) ² |
|---------------|--------------------|-------------------------------------|--|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits ¹

| V _{CCI} and VMV | Average V _{CCI} -GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ² | Maximum Overshoot/Undershoot ² |
|--------------------------|--|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC[®]3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#).

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points ([Figure 2-1 on page 2-4](#)).
2. V_{CCI} > V_{CC} - 0.75 V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until V_{CC} and V_{CCPLLX} exceed brownout activation levels. The V_{CC} activation level is specified as 1.1 V worst-case (see [Figure 2-1 on page 2-4](#) for more details).

When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the

Power-Up/Down Behavior of Low-Power Flash Devices chapter of the handbook for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

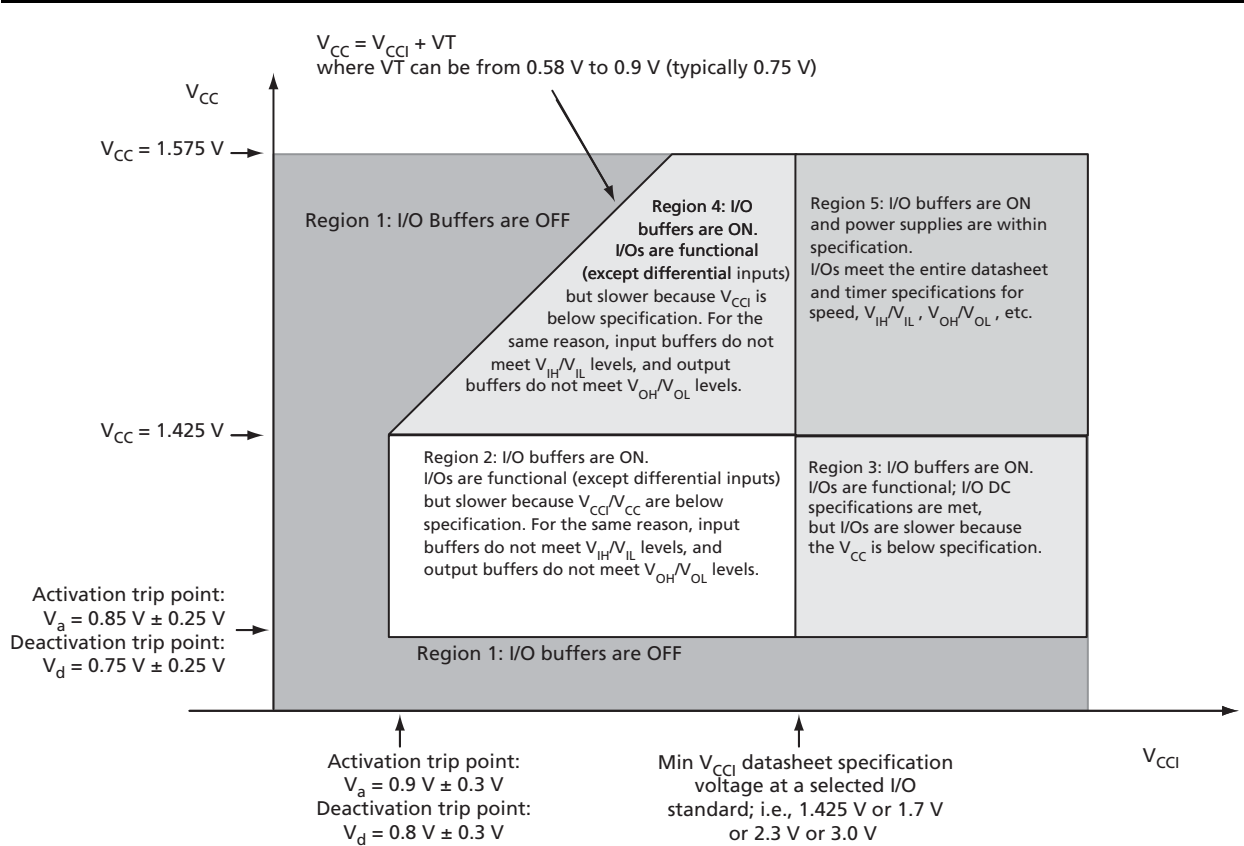


Figure 2-1 • I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 2-1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 1.463 \text{ W}$$

EQ 2-2

Table 2-5 • Package Thermal Resistivities

| Package Type | Device | Pin Count | θ_{jc} | θ_{ja} | | | Units |
|-----------------------------------|-------------|-----------|---------------|---------------|--------------|--------------|-------|
| | | | | Still Air | 200 ft./min. | 500 ft./min. | |
| Quad Flat No Lead | A3P030 | 132 | 0.4 | 21.4 | 16.8 | 15.3 | C/W |
| | A3P060 | 132 | 0.3 | 21.2 | 16.6 | 15.0 | C/W |
| | A3P125 | 132 | 0.2 | 21.1 | 16.5 | 14.9 | C/W |
| | A3P250 | 132 | 0.1 | 21.0 | 16.4 | 14.8 | C/W |
| Very Thin Quad Flat Pack (VQFP) | All devices | 100 | 10.0 | 35.3 | 29.4 | 27.1 | C/W |
| Thin Quad Flat Pack (TQFP) | All devices | 144 | 11.0 | 33.5 | 28.0 | 25.7 | C/W |
| Plastic Quad Flat Pack (PQFP) | All devices | 208 | 8.0 | 26.1 | 22.5 | 20.8 | C/W |
| PQFP with embedded heatspreader | All devices | 208 | 3.8 | 16.2 | 13.3 | 11.9 | C/W |
| Fine Pitch Ball Grid Array (FBGA) | See note* | 144 | 3.8 | 26.9 | 22.9 | 21.5 | C/W |
| | See note* | 256 | 3.8 | 26.6 | 22.8 | 21.5 | C/W |
| | See note* | 484 | 3.2 | 20.5 | 17.0 | 15.9 | C/W |
| | A3P1000 | 144 | 6.3 | 31.6 | 26.2 | 24.2 | C/W |
| | A3P1000 | 256 | 6.6 | 28.1 | 24.4 | 22.7 | C/W |
| | A3P1000 | 484 | 8.0 | 23.3 | 19.0 | 16.7 | C/W |

* This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$)

| Array Voltage V_{CC} (V) | Junction Temperature ($^\circ\text{C}$) | | | | | |
|----------------------------|---|-------------------|--------------------|--------------------|--------------------|---------------------|
| | -40°C | 0°C | 25°C | 70°C | 85°C | 110°C |
| 1.425 | 0.87 | 0.92 | 0.95 | 1.00 | 1.02 | 1.05 |
| 1.500 | 0.83 | 0.88 | 0.90 | 0.95 | 0.97 | 0.99 |
| 1.575 | 0.80 | 0.85 | 0.87 | 0.92 | 0.93 | 0.96 |

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

| | A3P015 | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|--------------------------------|--------|--------|--------|--------|--------|--------|--------|---------|
| Typical (25°C) | 2 mA | 2 mA | 2 mA | 2 mA | 3 mA | 3 mA | 5 mA | 8 mA |
| Max. (Commercial) | 10 mA | 10 mA | 10 mA | 10 mA | 20 mA | 20 mA | 30 mA | 50 mA |
| Max. (Industrial) | 15 mA | 15 mA | 15 mA | 15 mA | 30 mA | 30 mA | 45 mA | 75 mA |

Notes:

- I_{DD} Includes V_{CC} , V_{PUMP} , V_{CC1} , and VMV currents. Values do not include I/O static contribution, which is shown in [Table 2-11](#) and [Table 2-12](#) on [page 2-8](#).
- $-F$ speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.

Power per I/O Pin

Table 2-8 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Advanced I/O Banks

| | VMV (V) | Static Power P_{DC2} (mW) ¹ | Dynamic Power P_{AC9} ($\mu\text{W}/\text{MHz}$) ² |
|-----------------------------|---------|--|---|
| Single-Ended | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 3.3 | – | 16.69 |
| 2.5 V LVCMOS | 2.5 | – | 5.12 |
| 1.8 V LVCMOS | 1.8 | – | 2.13 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.45 |
| 3.3 V PCI | 3.3 | – | 18.11 |
| 3.3 V PCI-X | 3.3 | – | 18.11 |
| Differential | | | |
| LVDS | 2.5 | 2.26 | 1.20 |
| LVPECL | 3.3 | 5.72 | 1.87 |

Notes:

- P_{DC2} is the static power (where applicable) measured on VMV.
- P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

**Table 2-9 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks**

| | VMV (V) | Static Power P_{DC2} (mW) ¹ | Dynamic Power P_{AC9} (μ W/MHz) ² |
|-----------------------------|---------|---|--|
| Single-Ended | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 3.3 | – | 16.72 |
| 2.5 V LVCMOS | 2.5 | – | 5.14 |
| 1.8 V LVCMOS | 1.8 | – | 2.13 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.48 |
| 3.3 V PCI | 3.3 | – | 18.13 |
| 3.3 V PCI-X | 3.3 | – | 18.13 |

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

**Table 2-10 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard I/O Banks**

| | VMV (V) | Static Power P_{DC2} (mW) ¹ | Dynamic Power P_{AC9} (μ W/MHz) ² |
|-----------------------------|---------|---|--|
| Single-Ended | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 3.3 | – | 16.79 |
| 2.5 V LVCMOS | 2.5 | – | 5.19 |
| 1.8 V LVCMOS | 1.8 | – | 2.18 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.52 |

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
1. P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

**Table 2-11 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Advanced I/O Banks**

| | C_{LOAD} (pF) | V_{CCI} (V) | Static Power P_{DC3} (mW) ² | Dynamic Power P_{AC10} (μ W/MHz) ³ |
|--------------------------------|-----------------|---------------|---|---|
| Single-Ended | | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 468.67 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 267.48 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 149.46 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 103.12 |
| 3.3 V PCI | 10 | 3.3 | – | 201.02 |
| 3.3 V PCI-X | 10 | 3.3 | – | 201.02 |
| Differential | | | | |
| LVDS | – | 2.5 | 7.74 | 88.92 |
| LVPECL | – | 3.3 | 19.54 | 166.52 |

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on V_{CCI} .
3. P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI} .

**Table 2-12 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings¹
Applicable to Standard Plus I/O Banks**

| | C_{LOAD} (pF) | V_{CCI} (V) | Static Power P_{DC3} (mW) ² | Dynamic Power P_{AC10} (μ W/MHz) ³ |
|--------------------------------|-----------------|---------------|---|---|
| Single-Ended | | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 452.67 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 258.32 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 133.59 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 92.84 |
| 3.3 V PCI | 10 | 3.3 | – | 184.92 |
| 3.3 V PCI-X | 10 | 3.3 | – | 184.92 |

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on V_{MV} .
3. P_{AC10} is the total dynamic power measured on V_{CC} and V_{MV} .

**Table 2-13 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings¹
Applicable to Standard I/O Banks**

| | C_{LOAD} (pF) | V_{CCI} (V) | Static Power P_{DC3} (mW) ² | Dynamic Power P_{AC10} (μ W/MHz) ³ |
|--------------------------------|-----------------|---------------|---|---|
| Single-Ended | | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 431.08 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 247.36 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 128.46 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 89.46 |

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on V_{CCI} .
3. P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI} .

Power Consumption of Various Internal Resources

Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices

| Parameter | Definition | Device Specific Dynamic Contributions ($\mu\text{W}/\text{MHz}$) | | | | | | | |
|-------------------|--|---|--------|--------|--------|--------|--------|--------|--------|
| | | A3P1000 | A3P600 | A3P400 | A3P250 | A3P125 | A3P060 | A3P030 | A3P015 |
| P _{AC1} | Clock contribution of a Global Rib | 14.50 | 12.80 | 12.80 | 11.00 | 11.00 | 9.30 | 9.30 | 9.30 |
| P _{AC2} | Clock contribution of a Global Spine | 2.48 | 1.85 | 1.35 | 1.58 | 0.81 | 0.81 | 0.41 | 0.41 |
| P _{AC3} | Clock contribution of a VersaTile row | 0.81 | | | | | | | |
| P _{AC4} | Clock contribution of a VersaTile used as a sequential module | 0.12 | | | | | | | |
| P _{AC5} | First contribution of a VersaTile used as a sequential module | 0.07 | | | | | | | |
| P _{AC6} | Second contribution of a VersaTile used as a sequential module | 0.29 | | | | | | | |
| P _{AC7} | Contribution of a VersaTile used as a combinatorial Module | 0.29 | | | | | | | |
| P _{AC8} | Average contribution of a routing net | 0.70 | | | | | | | |
| P _{AC9} | Contribution of an I/O input pin (standard dependent) | See Table 2-8 on page 2-6 through Table 2-10 on page 2-7. | | | | | | | |
| P _{AC10} | Contribution of an I/O output pin (standard dependent) | See Table 2-11 on page 2-8 through Table 2-13 on page 2-9. | | | | | | | |
| P _{AC11} | Average contribution of a RAM block during a read operation | 25.00 | | | | | | | |
| P _{AC12} | Average contribution of a RAM block during a write operation | 30.00 | | | | | | | |
| P _{AC13} | Dynamic contribution for PLL | 2.60 | | | | | | | |

Note: *For a different output load, drive strength, or slew rate, Actel recommends using the Actel Power spreadsheet calculator or SmartPower tool in Libero® Integrated Design Environment (IDE) software.

Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices

| Parameter | Definition | Device Specific Static Power (mW) | | | | | | | |
|------------------|--|--|--------|--------|--------|--------|--------|--------|--------|
| | | A3P1000 | A3P600 | A3P400 | A3P250 | A3P125 | A3P060 | A3P030 | A3P015 |
| P _{DC1} | Array static power in Active mode | See Table 2-7 on page 2-6. | | | | | | | |
| P _{DC2} | I/O input pin static power (standard-dependent) | See Table 2-8 on page 2-6 through Table 2-10 on page 2-7. | | | | | | | |
| P _{DC3} | I/O output pin static power (standard-dependent) | See Table 2-11 on page 2-8 through Table 2-13 on page 2-9. | | | | | | | |
| P _{DC4} | Static PLL contribution | 2.55 mW | | | | | | | |
| P _{DC5} | Bank quiescent power (V _{CCI} -dependent) | See Table 2-7 on page 2-6. | | | | | | | |

Note: *For a different output load, drive strength, or slew rate, Actel recommends using the Actel

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-16 on page 2-14](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-17 on page 2-14](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-17 on page 2-14](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in [Table 2-16 on page 2-14](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in [Table 2-16 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-16 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-16 on page 2-14](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-17 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-17 on page 2-14](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-16 • Toggle Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|------------|----------------------------------|-----------|
| α_1 | Toggle rate of VersaTile outputs | 10% |
| α_2 | I/O buffer toggle rate | 10% |

Table 2-17 • Enable Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|-----------|--------------------------------------|-----------|
| β_1 | I/O output buffer enable rate | 100% |
| β_2 | RAM enable rate for read operations | 12.5% |
| β_3 | RAM enable rate for write operations | 12.5% |

User I/O Characteristics

Timing Model

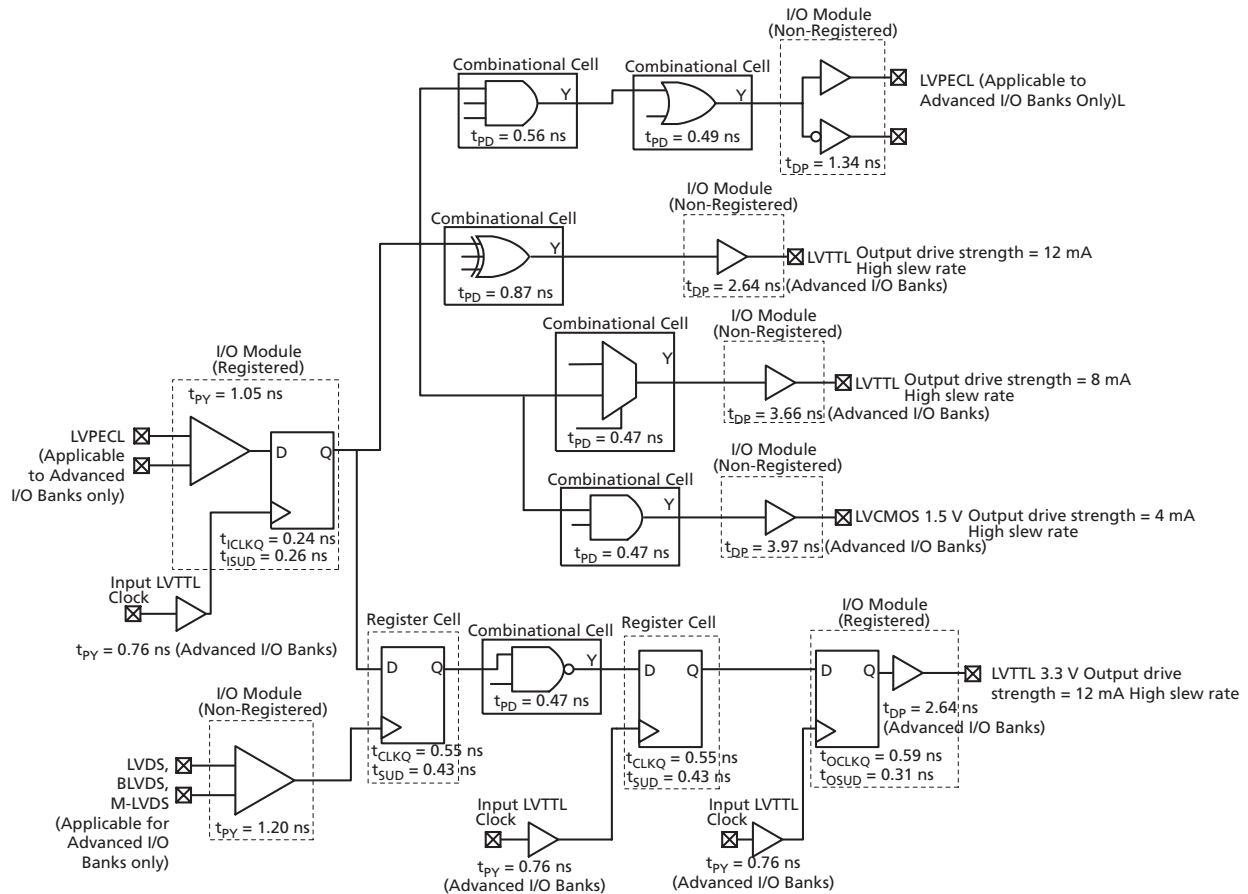


Figure 2-2 • Timing Model

Operating Conditions: -2 Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst Case
 $V_{CC} = 1.425$ V

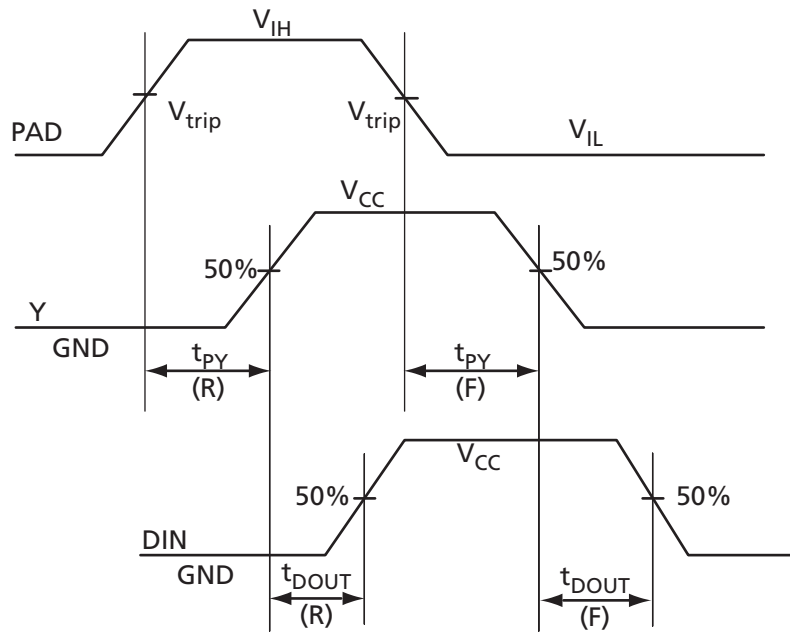
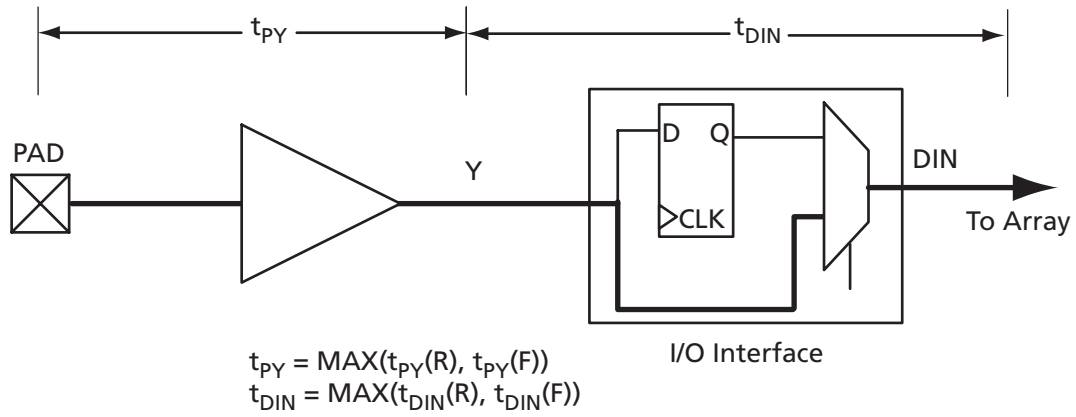


Figure 2-3 • Input Buffer Timing Model and Delays (example)

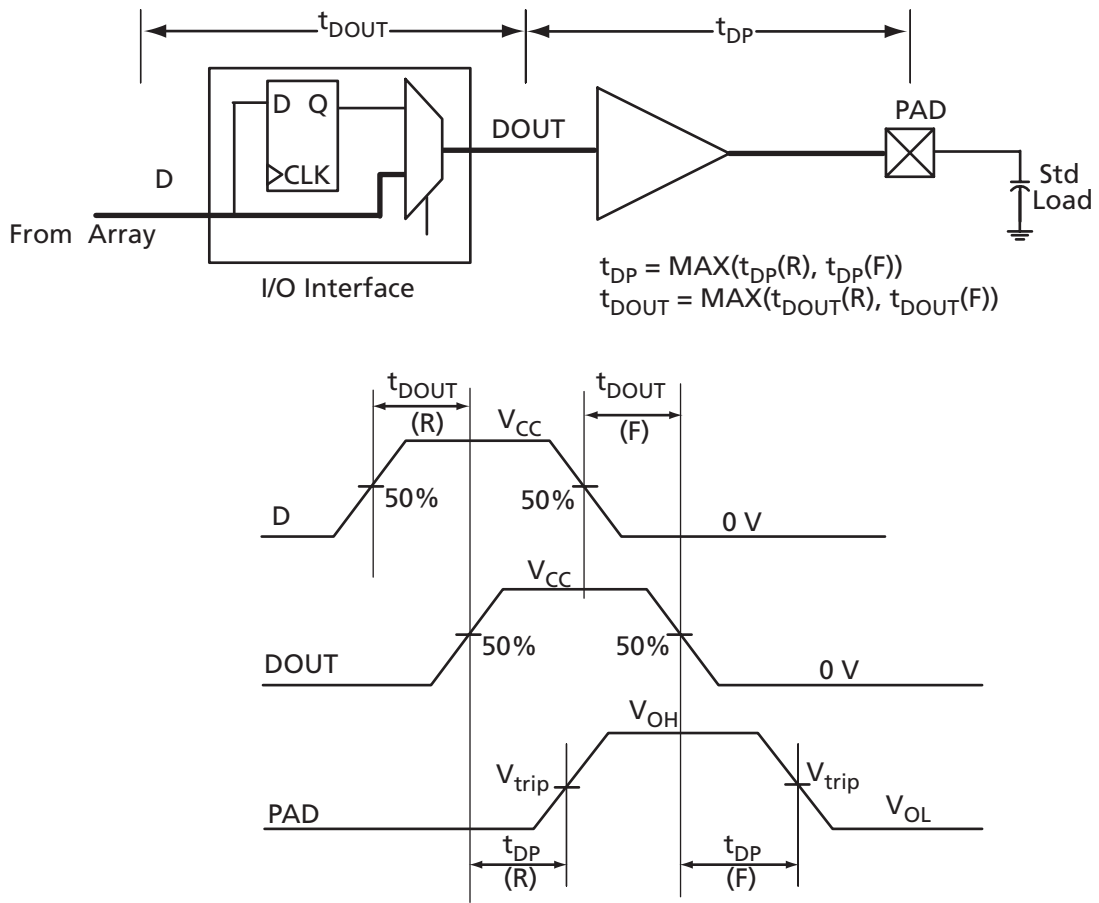


Figure 2-4 • Output Buffer Model and Delays (example)

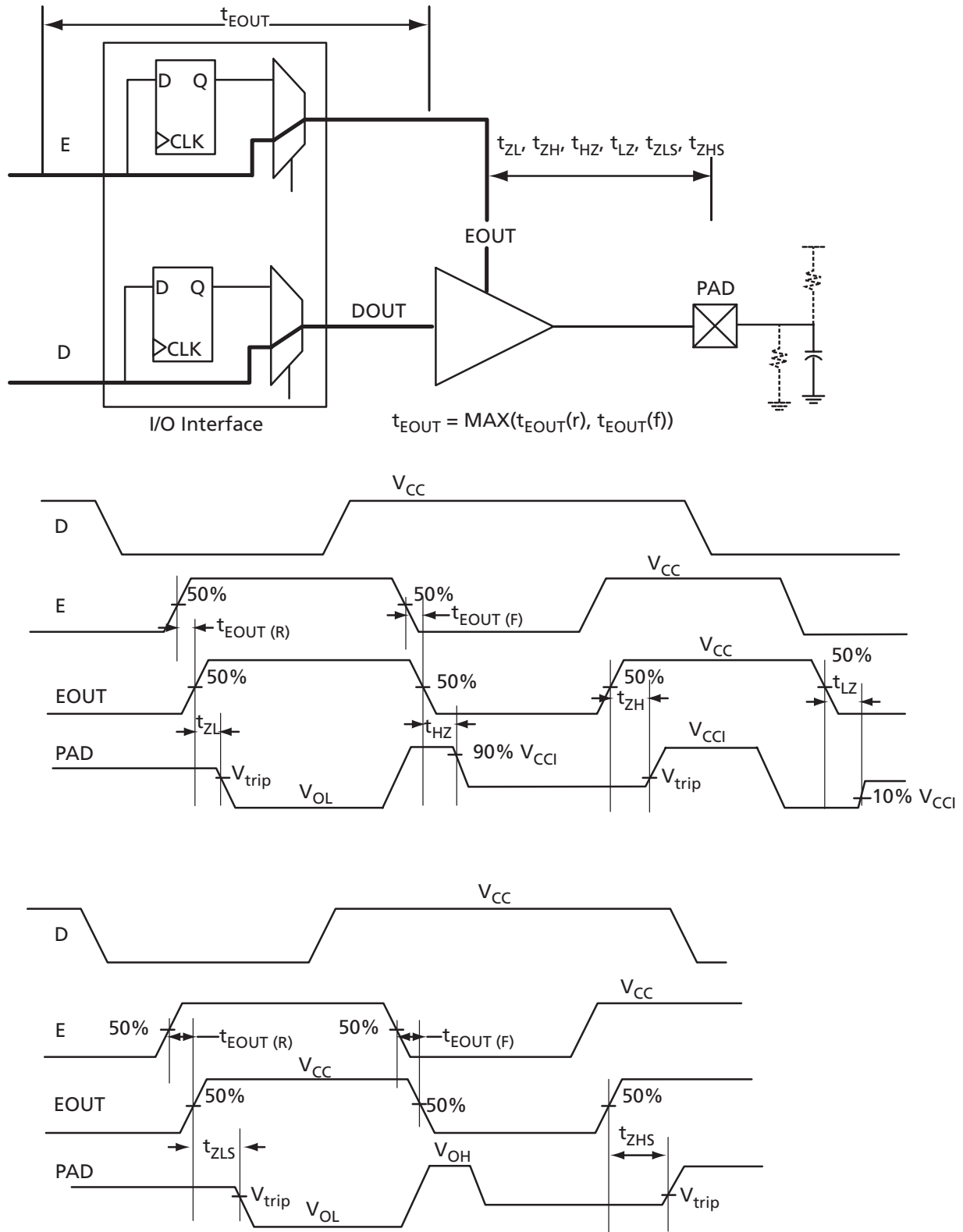


Figure 2-5 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Advanced I/O Banks

| I/O Standard | Drive Strength | Slew Rate | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} |
|--------------------------------|--------------------------|-----------|-----------------|-------------------------|-------------------------|--------|-------------------------|-------------------------|-----------------|-----------------|
| | | | Min, V | Max, V | Min, V | Max, V | Max, V | Min, V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | -0.3 | 0.35 * V _{CC1} | 0.65 * V _{CC1} | 3.6 | 0.45 | V _{CC1} - 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | -0.3 | 0.30 * V _{CC1} | 0.7 * V _{CC1} | 3.6 | 0.25 * V _{CC1} | 0.75 * V _{CC1} | 12 | 12 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | |

Note: Currents are measured at 85°C junction temperature.

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard Plus I/O Banks

| I/O Standard | Drive Strength | Slew Rate | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} |
|--------------------------------|--------------------------|-----------|-----------------|-------------------------|-------------------------|--------|-------------------------|-------------------------|-----------------|-----------------|
| | | | Min, V | Max, V | Min, V | Max, V | Max, V | Min, V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 8 mA | High | -0.3 | 0.35 * V _{CC1} | 0.65 * V _{CC1} | 3.6 | 0.45 | V _{CC1} - 0.45 | 8 | 8 |
| 1.5 V LVCMOS | 4 mA | High | -0.3 | 0.30 * V _{CC1} | 0.7 * V _{CC1} | 3.6 | 0.25 * V _{CC1} | 0.75 * V _{CC1} | 4 | 4 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | |

Note: Currents are measured at 85°C junction temperature.

Table 2-20 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard I/O Banks

| I/O Standard | Drive Strength | Slew Rate | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} |
|--------------------------------|----------------|-----------|-----------------|-------------------------|-------------------------|--------|-------------------------|-------------------------|-----------------|-----------------|
| | | | Min, V | Max, V | Min, V | Max, V | Max, V | Min, V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 8 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 |
| 2.5 V LVCMOS | 8 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 |
| 1.8 V LVCMOS | 4 mA | High | -0.3 | 0.35 * V _{CC1} | 0.65 * V _{CC1} | 3.6 | 0.45 | V _{CC1} - 0.45 | 4 | 4 |
| 1.5 V LVCMOS | 2 mA | High | -0.3 | 0.30 * V _{CC1} | 0.7 * V _{CC1} | 3.6 | 0.25 * V _{CC1} | 0.75 * V _{CC1} | 2 | 2 |

Note: Currents are measured at 85°C junction temperature.

**Table 2-21 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions**

| DC I/O Standards | Commercial ¹ | | Industrial ² | |
|-----------------------------|-------------------------|-----------------|-------------------------|-----------------|
| | I _{IL} | I _{IH} | I _{IL} | I _{IH} |
| | μA | μA | μA | μA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V PCI | 10 | 10 | 15 | 15 |
| 3.3 V PCI-X | 10 | 10 | 15 | 15 |

Notes:

1. Commercial range ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • Summary of AC Measuring Points

| Standard | Measuring Trip Point (V _{trip}) |
|-----------------------------|---|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 1.4 V |
| 2.5 V LVCMOS | 1.2 V |
| 1.8 V LVCMOS | 0.90 V |
| 1.5 V LVCMOS | 0.75 V |
| 3.3 V PCI | 0.285 * V _{CC1} (RR) |
| | 0.615 * V _{CC1} (FF) |
| 3.3 V PCI-X | 0.285 * V _{CC1} (RR) |
| | 0.615 * V _{CC1} (FF) |

Table 2-23 • I/O AC Parameter Definitions

| Parameter | Parameter Definition |
|-------------------|---|
| t _{DP} | Data to Pad delay through the Output Buffer |
| t _{PY} | Pad to Data delay through the Input Buffer |
| t _{DOUT} | Data to Output Buffer delay through the I/O interface |
| t _{EOUT} | Enable to Output Buffer Tristate Control delay through the I/O interface |
| t _{DIN} | Input Buffer to Data delay through the I/O interface |
| t _{HZ} | Enable to Pad delay through the Output Buffer—HIGH to Z |
| t _{ZH} | Enable to Pad delay through the Output Buffer—Z to HIGH |
| t _{LZ} | Enable to Pad delay through the Output Buffer—LOW to Z |
| t _{ZL} | Enable to Pad delay through the Output Buffer—Z to LOW |
| t _{ZHS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH |
| t _{ZLS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW |



Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$,
 Worst Case $V_{CCI} = 3.0\text{ V}$
 Advanced I/O Banks

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | t_{DOUT} (ns) | t_{DP} (ns) | t_{DIN} (ns) | t_{PY} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | t_{ZLS} (ns) | t_{ZHS} (ns) | Units |
|--------------------------------|---------------------|-----------|----------------------|--------------------------------|-----------------|---------------|----------------|---------------|-----------------|---------------|---------------|---------------|---------------|----------------|----------------|-------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 | High | 35 | – | 0.49 | 2.64 | 0.03 | 0.76 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 2.5 V LVCMOS | 12 | High | 35 | – | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 1.8 V LVCMOS | 12 | High | 35 | – | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |
| 1.5 V LVCMOS | 12 | High | 35 | – | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 3.3 V PCI | Per PCI spec. | High | 10 | 25 ² | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |
| 3.3 V PCI-X | Per PCI-X spec. | High | 10 | 25 ² | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |
| LVDS | 24 | High | – | – | 0.49 | 1.37 | 0.03 | 1.20 | – | – | – | – | – | – | – | n |
| LVPECL | 24 | High | – | – | 0.49 | 1.34 | 0.03 | 1.05 | – | – | – | – | – | – | – | ns |

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-10 on page 2-56](#) for connectivity. This resistor is not required during normal operation.

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Standard Plus I/O Banks

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor | t_{DOUT} (ns) | t_{DP} (ns) | t_{DIN} (ns) | t_{PY} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | t_{ZLS} (ns) | t_{ZHS} (ns) | Units |
|-----------------------------|---------------------|-----------|----------------------|-------------------|-----------------|---------------|----------------|---------------|-----------------|---------------|---------------|---------------|---------------|----------------|----------------|-------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 mA | High | 35 pF | – | 0.49 | 2.36 | 0.03 | 0.75 | 0.32 | 2.40 | 1.93 | 2.08 | 2.41 | 4.07 | 3.60 | ns |
| 2.5 V LVCMOS | 12 mA | High | 35 pF | – | 0.49 | 2.39 | 0.03 | 0.97 | 0.32 | 2.44 | 2.35 | 2.11 | 2.32 | 4.11 | 4.02 | ns |
| 1.8 V LVCMOS | 8 mA | High | 35 pF | – | 0.49 | 3.03 | 0.03 | 0.90 | 0.32 | 2.87 | 3.03 | 2.19 | 2.32 | 4.54 | 4.70 | ns |
| 1.5 V LVCMOS | 4 mA | High | 35 pF | – | 0.49 | 3.61 | 0.03 | 1.06 | 0.32 | 3.35 | 3.61 | 2.26 | 2.34 | 5.02 | 5.28 | ns |
| 3.3 V PCI | Per PCI spec. | High | 10 pF | 25 ² | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |
| 3.3 V PCI-X | Per PCI-X spec. | High | 10 pF | 25 ² | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-10 on page 2-56](#) for connectivity. This resistor is not required during normal operation.

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Standard I/O Banks

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor | t_{DOUT} (ns) | t_{DP} (ns) | t_{DIN} (ns) | t_{PY} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | Units |
|-----------------------------|---------------------|-----------|----------------------|-------------------|-----------------|---------------|----------------|---------------|-----------------|---------------|---------------|---------------|---------------|-------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 8 mA | High | 35 pF | – | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 2.5 V LVCMOS | 8 mA | High | 35 pF | – | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 1.8 V LVCMOS | 4 mA | High | 35 pF | – | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |
| 1.5 V LVCMOS | 2 mA | High | 35 pF | – | 0.49 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-10 on page 2-56](#) for connectivity. This resistor is not required during normal operation.



Detailed I/O DC Characteristics

Table 2-27 • Input Capacitance

| Symbol | Definition | Conditions | Min. | Max. | Units |
|-------------|------------------------------------|-----------------------------------|------|------|-------|
| C_{IN} | Input capacitance | $V_{IN} = 0, f = 1.0 \text{ MHz}$ | | 8 | pF |
| C_{INCLK} | Input capacitance on the clock pin | $V_{IN} = 0, f = 1.0 \text{ MHz}$ | | 8 | pF |

**Table 2-28 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks**

| Standard | Drive Strength | $R_{PULL-DOWN}$ (Ω) ² | $R_{PULL-UP}$ (Ω) ³ |
|-----------------------------|-----------------------------|--|--|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CC} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/libis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-29 • I/O Output Buffer Maximum Resistances ¹
Applicable to Standard Plus I/O Banks

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-----------------------------|-----------------------------|--|--|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 25 | 75 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CC} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/libis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-30 • I/O Output Buffer Maximum Resistances¹
 Applicable to Standard I/O Banks

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-----------------------------|----------------|--|--|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CC} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/libis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances
 Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

| V _{CC} | R _(WEAK PULL-UP) ¹ (Ω) | | R _(WEAK PULL-DOWN) ² (Ω) | |
|-----------------|---|------|---|-------|
| | Min. | Max. | Min. | Max. |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (V_{OLspec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK PULL-UP-MIN)}$

**Table 2-32 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Advanced I/O Banks**

| | Drive Strength | I_{OSL} (mA)* | I_{OSH} (mA)* |
|-----------------------------|-----------------------------|-----------------|-----------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 127 | 132 |
| | 24 mA | 181 | 268 |
| 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 127 | 132 |
| | 24 mA | 181 | 268 |
| 2.5 V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| | 16 mA | 87 | 83 |
| | 24 mA | 124 | 169 |
| 1.8 V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 51 | 45 |
| | 12 mA | 74 | 91 |
| | 16 mA | 74 | 91 |
| 1.5 V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| | 6 mA | 39 | 32 |
| | 8 mA | 55 | 66 |
| | 12 mA | 55 | 66 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

* $T_J = 100^\circ\text{C}$

**Table 2-33 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Standard Plus I/O Banks**

| | Drive Strength | I_{OSL} (mA)* | I_{OSH} (mA)* |
|-----------------------------|-----------------------------|-----------------|-----------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 109 | 103 |
| 2.5 V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| 1.8 V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 44 | 35 |
| 1.5 V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

* $T_J = 100^\circ\text{C}$

**Table 2-34 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Standard I/O Banks**

| | Drive Strength | I_{OSL} (mA)* | I_{OSH} (mA)* |
|-----------------------------|----------------|-----------------|-----------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| 2.5 V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| 1.8 V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| 1.5 V LVCMOS | 2 mA | 16 | 13 |

* $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event before Failure

| Temperature | Time before Failure |
|-------------|---------------------|
| -40°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |
| 110°C | 3 months |

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|-------------------------------|-----------------------------|-----------------------------|------------------|
| LVTTL/LVCMOS | No requirement | 10 ns * | 20 years (110°C) |
| LVDS/B-LVDS/ M-LVDS/LVPECL | No requirement | 10 ns * | 10 years (100°C) |

* The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-37 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

| 3.3 V LVTTTL / 3.3 V LVCMOS | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|--------------------------------|----------|---------|----------|---------|----------|----------|----------|----------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA^2 | μA^2 |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 10 | 10 |
| 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-38 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

| 3.3 V LVTTTL / 3.3 V LVCMOS | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|--------------------------------|----------|---------|----------|---------|----------|----------|----------|----------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA^2 | μA^2 |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 109 | 103 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-39 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

| 3.3 V LVTTTL / 3.3 V LVCMOS | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|--------------------------------|----------|---------|----------|---------|----------|----------|----------|----------|-----------------------|-----------------------|-----------|-----------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA^2 | μA^2 |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

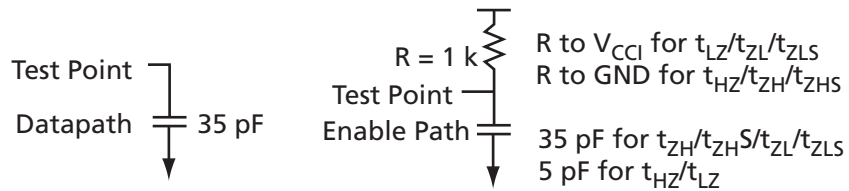


Figure 2-6 • AC Loading

Table 2-40 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|------------------------|
| 0 | 3.3 | 1.4 | 35 |

* Measuring point = V_{trip}. See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | -F | 0.79 | 9.20 | 0.05 | 1.22 | 0.51 | 9.37 | 7.91 | 3.18 | 3.14 | 12.05 | 10.60 | ns |
| | Std. | 0.66 | 7.66 | 0.04 | 1.02 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | -1 | 0.56 | 6.51 | 0.04 | 0.86 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | -2 | 0.49 | 5.72 | 0.03 | 0.76 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 6 mA | -F | 0.79 | 5.89 | 0.05 | 1.22 | 0.51 | 6.00 | 4.89 | 3.59 | 3.85 | 8.69 | 7.57 | ns |
| | Std. | 0.66 | 4.91 | 0.04 | 1.02 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | -1 | 0.56 | 4.17 | 0.04 | 0.86 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | -2 | 0.49 | 3.66 | 0.03 | 0.76 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 8 mA | -F | 0.79 | 5.89 | 0.05 | 1.22 | 0.51 | 6.00 | 4.89 | 3.59 | 3.85 | 8.69 | 7.57 | ns |
| | Std. | 0.66 | 4.91 | 0.04 | 1.02 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | -1 | 0.56 | 4.17 | 0.04 | 0.86 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | -2 | 0.49 | 3.66 | 0.03 | 0.76 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 12 mA | -F | 0.79 | 4.24 | 0.05 | 1.22 | 0.51 | 4.32 | 3.39 | 3.86 | 4.30 | 7.01 | 6.08 | ns |
| | Std. | 0.66 | 3.53 | 0.04 | 1.02 | 0.43 | 3.60 | 2.82 | 3.21 | 3.58 | 5.83 | 5.06 | ns |
| | -1 | 0.56 | 3.00 | 0.04 | 0.86 | 0.36 | 3.06 | 2.40 | 2.73 | 3.05 | 4.96 | 4.30 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.76 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 16 mA | -F | 0.79 | 4.00 | 0.05 | 1.22 | 0.51 | 4.08 | 3.08 | 3.92 | 4.42 | 6.76 | 5.77 | ns |
| | Std. | 0.66 | 3.33 | 0.04 | 1.02 | 0.43 | 3.39 | 2.56 | 3.26 | 3.68 | 5.63 | 4.80 | ns |
| | -1 | 0.56 | 2.83 | 0.04 | 0.86 | 0.36 | 2.89 | 2.18 | 2.77 | 3.13 | 4.79 | 4.08 | ns |
| | -2 | 0.49 | 2.49 | 0.03 | 0.76 | 0.32 | 2.53 | 1.91 | 2.44 | 2.75 | 4.20 | 3.58 | ns |
| 24 mA | -F | 0.79 | 3.69 | 0.05 | 1.22 | 0.51 | 3.76 | 2.54 | 3.99 | 4.88 | 6.45 | 5.23 | ns |
| | Std. | 0.66 | 3.08 | 0.04 | 1.02 | 0.43 | 3.13 | 2.12 | 3.32 | 4.06 | 5.37 | 4.35 | ns |
| | -1 | 0.56 | 2.62 | 0.04 | 0.86 | 0.36 | 2.66 | 1.80 | 2.83 | 3.45 | 4.57 | 3.70 | ns |
| | -2 | 0.49 | 2.30 | 0.03 | 0.76 | 0.32 | 2.34 | 1.58 | 2.48 | 3.03 | 4.01 | 3.25 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | -F | 0.79 | 12.32 | 0.05 | 1.22 | 0.51 | 12.55 | 10.69 | 3.18 | 2.95 | 15.23 | 13.37 | ns |
| | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | -1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | -2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | -F | 0.79 | 8.74 | 0.05 | 1.22 | 0.51 | 8.90 | 7.55 | 3.58 | 3.65 | 11.59 | 10.23 | ns |
| | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | -1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | -2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | -F | 0.79 | 8.74 | 0.05 | 1.22 | 0.51 | 8.90 | 7.55 | 3.58 | 3.65 | 11.59 | 10.23 | ns |
| | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | -1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | -2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | -F | 0.79 | 6.70 | 0.05 | 1.22 | 0.51 | 6.83 | 5.85 | 3.85 | 4.10 | 9.51 | 8.54 | ns |
| | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | -1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | -2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | -F | 0.79 | 6.25 | 0.05 | 1.22 | 0.51 | 6.37 | 5.48 | 3.91 | 4.22 | 9.06 | 8.17 | ns |
| | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | -1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | -2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | -F | 0.79 | 5.83 | 0.05 | 1.22 | 0.51 | 5.93 | 5.46 | 3.98 | 4.67 | 8.62 | 8.15 | ns |
| | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-43 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | -F | 0.79 | 8.65 | 0.05 | 1.20 | 0.51 | 8.81 | 7.55 | 2.73 | 2.81 | 11.50 | 10.24 | ns |
| | Std. | 0.66 | 7.20 | 0.04 | 1.00 | 0.43 | 7.34 | 6.29 | 2.27 | 2.34 | 9.57 | 8.52 | ns |
| | -1 | 0.56 | 6.13 | 0.04 | 0.85 | 0.36 | 6.24 | 5.35 | 1.93 | 1.99 | 8.14 | 7.25 | ns |
| | -2 | 0.49 | 5.38 | 0.03 | 0.75 | 0.32 | 5.48 | 4.69 | 1.70 | 1.75 | 7.15 | 6.36 | ns |
| 6 mA | -F | 0.79 | 5.41 | 0.05 | 1.20 | 0.51 | 5.51 | 4.58 | 3.10 | 3.45 | 8.19 | 7.27 | ns |
| | Std. | 0.66 | 4.50 | 0.04 | 1.00 | 0.43 | 4.58 | 3.82 | 2.58 | 2.88 | 6.82 | 6.05 | ns |
| | -1 | 0.56 | 3.83 | 0.04 | 0.85 | 0.36 | 3.90 | 3.25 | 2.19 | 2.45 | 5.80 | 5.15 | ns |
| | -2 | 0.49 | 3.36 | 0.03 | 0.75 | 0.32 | 3.42 | 2.85 | 1.92 | 2.15 | 5.09 | 4.52 | ns |
| 8 mA | -F | 0.79 | 5.41 | 0.05 | 1.20 | 0.51 | 5.51 | 4.58 | 3.10 | 3.45 | 8.19 | 7.27 | ns |
| | Std. | 0.66 | 4.50 | 0.04 | 1.00 | 0.43 | 4.58 | 3.82 | 2.58 | 2.88 | 6.82 | 6.05 | ns |
| | -1 | 0.56 | 3.83 | 0.04 | 0.85 | 0.36 | 3.90 | 3.25 | 2.19 | 2.45 | 5.80 | 5.15 | ns |
| | -2 | 0.49 | 3.36 | 0.03 | 0.75 | 0.32 | 3.42 | 2.85 | 1.92 | 2.15 | 5.09 | 4.52 | ns |
| 12 mA | -F | 0.79 | 3.80 | 0.05 | 1.20 | 0.51 | 3.87 | 3.10 | 3.35 | 3.87 | 6.55 | 5.79 | ns |
| | Std. | 0.66 | 3.16 | 0.04 | 1.00 | 0.43 | 3.22 | 2.58 | 2.79 | 3.22 | 5.45 | 4.82 | ns |
| | -1 | 0.56 | 2.69 | 0.04 | 0.85 | 0.36 | 2.74 | 2.20 | 2.37 | 2.74 | 4.64 | 4.10 | ns |
| | -2 | 0.49 | 2.36 | 0.03 | 0.75 | 0.32 | 2.40 | 1.93 | 2.08 | 2.41 | 4.07 | 3.60 | ns |
| 16 mA | -F | 0.79 | 3.80 | 0.05 | 1.20 | 0.51 | 3.87 | 3.10 | 3.35 | 3.87 | 6.55 | 5.79 | ns |
| | Std. | 0.66 | 3.16 | 0.04 | 1.00 | 0.43 | 3.22 | 2.58 | 2.79 | 3.22 | 5.45 | 4.82 | ns |
| | -1 | 0.56 | 2.69 | 0.04 | 0.85 | 0.36 | 2.74 | 2.20 | 2.37 | 2.74 | 4.64 | 4.10 | ns |
| | -2 | 0.49 | 2.36 | 0.03 | 0.75 | 0.32 | 2.40 | 1.93 | 2.08 | 2.41 | 4.07 | 3.60 | ns |

Notes:

1. Software default selection highlighted in gray.
1. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-44 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | –F | 0.79 | 11.63 | 0.05 | 1.20 | 0.51 | 11.84 | 10.12 | 2.74 | 2.65 | 14.53 | 12.81 | ns |
| | Std. | 0.66 | 9.68 | 0.04 | 1.00 | 0.43 | 9.86 | 8.42 | 2.28 | 2.21 | 12.09 | 10.66 | ns |
| | –1 | 0.56 | 8.23 | 0.04 | 0.85 | 0.36 | 8.39 | 7.17 | 1.94 | 1.88 | 10.29 | 9.07 | ns |
| | –2 | 0.49 | 7.23 | 0.03 | 0.75 | 0.32 | 7.36 | 6.29 | 1.70 | 1.65 | 9.03 | 7.96 | ns |
| 6 mA | –F | 0.79 | 8.05 | 0.05 | 1.20 | 0.51 | 8.20 | 7.07 | 3.10 | 3.29 | 10.88 | 9.76 | ns |
| | Std. | 0.66 | 6.70 | 0.04 | 1.00 | 0.43 | 6.82 | 5.89 | 2.58 | 2.74 | 9.06 | 8.12 | ns |
| | –1 | 0.56 | 5.70 | 0.04 | 0.85 | 0.36 | 5.80 | 5.01 | 2.20 | 2.33 | 7.71 | 6.91 | ns |
| | –2 | 0.49 | 5.00 | 0.03 | 0.75 | 0.32 | 5.10 | 4.40 | 1.93 | 2.05 | 6.76 | 6.06 | ns |
| 8 mA | –F | 0.79 | 8.05 | 0.05 | 1.20 | 0.51 | 8.20 | 7.07 | 3.10 | 3.29 | 10.88 | 9.76 | ns |
| | Std. | 0.66 | 6.70 | 0.04 | 1.00 | 0.43 | 6.82 | 5.89 | 2.58 | 2.74 | 9.06 | 8.12 | ns |
| | –1 | 0.56 | 5.70 | 0.04 | 0.85 | 0.36 | 5.80 | 5.01 | 2.20 | 2.33 | 7.71 | 6.91 | ns |
| | –2 | 0.49 | 5.00 | 0.03 | 0.75 | 0.32 | 5.10 | 4.40 | 1.93 | 2.05 | 6.76 | 6.06 | ns |
| 12 mA | –F | 0.79 | 6.06 | 0.05 | 1.20 | 0.51 | 6.18 | 5.42 | 3.35 | 3.70 | 8.86 | 8.10 | ns |
| | Std. | 0.66 | 5.05 | 0.04 | 1.00 | 0.43 | 5.14 | 4.51 | 2.79 | 3.08 | 7.38 | 6.75 | ns |
| | –1 | 0.56 | 4.29 | 0.04 | 0.85 | 0.36 | 4.37 | 3.84 | 2.38 | 2.62 | 6.28 | 5.74 | ns |
| | –2 | 0.49 | 3.77 | 0.03 | 0.75 | 0.32 | 3.84 | 3.37 | 2.09 | 2.30 | 5.51 | 5.04 | ns |
| 16 mA | –F | 0.79 | 6.06 | 0.05 | 1.20 | 0.51 | 6.18 | 5.42 | 3.35 | 3.70 | 8.86 | 8.10 | ns |
| | Std. | 0.66 | 5.05 | 0.04 | 1.00 | 0.43 | 5.14 | 4.51 | 2.79 | 3.08 | 7.38 | 6.75 | ns |
| | –1 | 0.56 | 4.29 | 0.04 | 0.85 | 0.36 | 4.37 | 3.84 | 2.38 | 2.62 | 6.28 | 5.74 | ns |
| | –2 | 0.49 | 3.77 | 0.03 | 0.75 | 0.32 | 3.84 | 3.37 | 2.09 | 2.30 | 5.51 | 5.04 | |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-45 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | -F | 0.79 | 8.49 | 0.05 | 1.20 | 0.51 | 8.65 | 7.48 | 2.49 | 2.58 | ns |
| | Std. | 0.66 | 7.07 | 0.04 | 1.00 | 0.43 | 7.20 | 6.23 | 2.07 | 2.15 | ns |
| | -1 | 0.56 | 6.01 | 0.04 | 0.85 | 0.36 | 6.12 | 5.30 | 1.76 | 1.83 | ns |
| | -2 | 0.49 | 5.28 | 0.03 | 0.75 | 0.32 | 5.37 | 4.65 | 1.55 | 1.60 | ns |
| 4 mA | -F | 0.79 | 8.49 | 0.05 | 1.20 | 0.51 | 8.65 | 7.48 | 2.49 | 2.58 | ns |
| | Std. | 0.66 | 7.07 | 0.04 | 1.00 | 0.43 | 7.20 | 6.23 | 2.07 | 2.15 | ns |
| | -1 | 0.56 | 6.01 | 0.04 | 0.85 | 0.36 | 6.12 | 5.30 | 1.76 | 1.83 | ns |
| | -2 | 0.49 | 5.28 | 0.03 | 0.75 | 0.32 | 5.37 | 4.65 | 1.55 | 1.60 | ns |
| 6 mA | -F | 0.79 | 5.30 | 0.05 | 1.20 | 0.51 | 5.40 | 4.51 | 2.88 | 3.23 | ns |
| | Std. | 0.66 | 4.41 | 0.04 | 1.00 | 0.43 | 4.49 | 3.75 | 2.39 | 2.69 | ns |
| | -1 | 0.56 | 3.75 | 0.04 | 0.85 | 0.36 | 3.82 | 3.19 | 2.04 | 2.29 | ns |
| | -2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 8 mA | -F | 0.79 | 5.30 | 0.05 | 1.20 | 0.51 | 5.40 | 4.51 | 2.88 | 3.23 | ns |
| | Std. | 0.66 | 4.41 | 0.04 | 1.00 | 0.43 | 4.49 | 3.75 | 2.39 | 2.69 | ns |
| | -1 | 0.56 | 3.75 | 0.04 | 0.85 | 0.36 | 3.82 | 3.19 | 2.04 | 2.29 | ns |
| | -2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-46 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | –F | 0.79 | 11.37 | 0.05 | 1.20 | 0.51 | 11.58 | 10.26 | 2.49 | 2.45 | ns |
| | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | –1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | –2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 4 mA | –F | 0.79 | 11.37 | 0.05 | 1.20 | 0.51 | 11.58 | 10.26 | 2.49 | 2.45 | ns |
| | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | –1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | –2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 6 mA | –F | 0.79 | 7.89 | 0.05 | 1.20 | 0.51 | 8.04 | 7.19 | 2.88 | 3.09 | ns |
| | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | –1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | –2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |
| 8 mA | –F | 0.79 | 7.89 | 0.05 | 1.20 | 0.51 | 8.04 | 7.19 | 2.88 | 3.09 | ns |
| | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | –1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | –2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V-tolerant input buffer and push-pull output buffer.

Table 2-47 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

| 2.5 V LVCMOS | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} | I _{OSL} | I _{OSH} | I _{IL} | I _{IH} |
|--------------|-----------------|---------|-----------------|---------|-----------------|-----------------|-----------------|-----------------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA ² | μA ² |
| 2 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-48 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

| 2.5 V LVCMOS | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} | I _{OSL} | I _{OSH} | I _{IL} | I _{IH} |
|--------------|-----------------|---------|-----------------|---------|-----------------|-----------------|-----------------|-----------------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA ² | μA ² |
| 2 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-49 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

| 2.5 V LVCMOS Drive Strength | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|--------------------------------|----------|---------|----------|---------|----------|----------|----------|----------|-----------------------|-----------------------|-----------|-----------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA^2 | μA^2 |
| 2 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 16 | 18 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 32 | 37 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

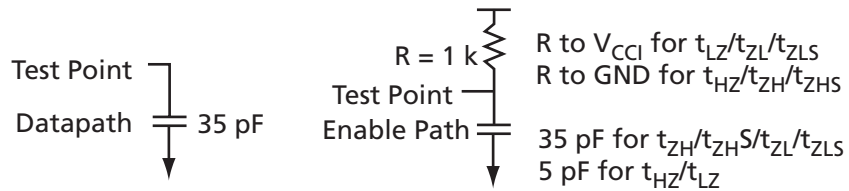


Figure 2-7 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | C_{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|
| 0 | 2.5 | 1.2 | 35 |

* Measuring point = V_{trip} . See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-51 • 2.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | -F | 0.72 | 10.41 | 0.05 | 1.57 | 0.51 | 9.41 | 10.41 | 3.22 | 2.77 | 12.09 | 13.09 | ns |
| | Std. | 0.60 | 8.66 | 0.04 | 1.31 | 0.43 | 7.83 | 8.66 | 2.68 | 2.30 | 10.07 | 10.90 | ns |
| | -1 | 0.51 | 7.37 | 0.04 | 1.11 | 0.36 | 6.66 | 7.37 | 2.28 | 1.96 | 8.56 | 9.27 | ns |
| | -2 | 0.45 | 6.47 | 0.03 | 0.98 | 0.32 | 5.85 | 6.47 | 2.00 | 1.72 | 7.52 | 8.14 | ns |
| 6 mA | -F | 0.72 | 6.21 | 0.05 | 1.57 | 0.51 | 6.05 | 6.21 | 3.66 | 3.60 | 8.74 | 8.89 | ns |
| | Std. | 0.60 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | -1 | 0.51 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | -2 | 0.45 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 8 mA | -F | 0.72 | 6.21 | 0.05 | 1.57 | 0.51 | 6.05 | 6.21 | 3.66 | 3.60 | 8.74 | 8.89 | ns |
| | Std. | 0.60 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | -1 | 0.51 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | -2 | 0.45 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 12 mA | -F | 0.72 | 4.28 | 0.05 | 1.57 | 0.51 | 4.36 | 4.12 | 3.97 | 4.13 | 7.04 | 6.81 | ns |
| | Std. | 0.60 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | -1 | 0.51 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | -2 | 0.45 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 16 mA | -F | 0.72 | 4.03 | 0.05 | 1.57 | 0.51 | 4.10 | 3.68 | 4.04 | 4.26 | 6.79 | 6.36 | ns |
| | Std. | 0.60 | 3.35 | 0.04 | 1.31 | 0.43 | 3.41 | 3.06 | 3.36 | 3.55 | 5.65 | 5.30 | ns |
| | -1 | 0.51 | 2.85 | 0.04 | 1.11 | 0.36 | 2.90 | 2.60 | 2.86 | 3.02 | 4.81 | 4.51 | ns |
| | -2 | 0.45 | 2.50 | 0.03 | 0.98 | 0.32 | 2.55 | 2.29 | 2.51 | 2.65 | 4.22 | 3.96 | ns |
| 24 mA | -F | 0.72 | 3.71 | 0.05 | 1.57 | 0.51 | 3.78 | 2.93 | 4.13 | 4.80 | 6.47 | 5.62 | ns |
| | Std. | 0.60 | 3.09 | 0.04 | 1.31 | 0.43 | 3.15 | 2.44 | 3.44 | 4.00 | 5.38 | 4.68 | ns |
| | -1 | 0.51 | 2.63 | 0.04 | 1.11 | 0.36 | 2.68 | 2.08 | 2.92 | 3.40 | 4.58 | 3.98 | ns |
| | -2 | 0.45 | 2.31 | 0.03 | 0.98 | 0.32 | 2.35 | 1.82 | 2.57 | 2.98 | 4.02 | 3.49 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-52 • 2.5 V LVC MOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | –F | 0.72 | 13.69 | 0.05 | 1.57 | 0.51 | 13.48 | 13.69 | 3.22 | 2.65 | 16.16 | 16.38 | ns |
| | Std. | 0.60 | 11.40 | 0.04 | 1.31 | 0.43 | 11.22 | 11.40 | 2.68 | 2.20 | 13.45 | 13.63 | ns |
| | –1 | 0.51 | 9.69 | 0.04 | 1.11 | 0.36 | 9.54 | 9.69 | 2.28 | 1.88 | 11.44 | 11.60 | ns |
| | –2 | 0.45 | 8.51 | 0.03 | 0.98 | 0.32 | 8.38 | 8.51 | 2.00 | 1.65 | 10.05 | 10.18 | ns |
| 6 mA | –F | 0.72 | 9.56 | 0.05 | 1.57 | 0.51 | 9.74 | 9.39 | 3.66 | 3.47 | 12.43 | 12.07 | ns |
| | Std. | 0.60 | 7.96 | 0.04 | 1.31 | 0.43 | 8.11 | 7.81 | 3.05 | 2.89 | 10.34 | 10.05 | ns |
| | –1 | 0.51 | 6.77 | 0.04 | 1.11 | 0.36 | 6.90 | 6.65 | 2.59 | 2.46 | 8.80 | 8.55 | ns |
| | –2 | 0.45 | 5.94 | 0.03 | 0.98 | 0.32 | 6.05 | 5.84 | 2.28 | 2.16 | 7.72 | 7.50 | ns |
| 8 mA | –F | 0.72 | 9.56 | 0.05 | 1.57 | 0.51 | 9.74 | 9.39 | 3.66 | 3.47 | 12.43 | 12.07 | ns |
| | Std. | 0.60 | 7.96 | 0.04 | 1.31 | 0.43 | 8.11 | 7.81 | 3.05 | 2.89 | 10.34 | 10.05 | ns |
| | –1 | 0.51 | 6.77 | 0.04 | 1.11 | 0.36 | 6.90 | 6.65 | 2.59 | 2.46 | 8.80 | 8.55 | ns |
| | –2 | 0.45 | 5.94 | 0.03 | 0.98 | 0.32 | 6.05 | 5.84 | 2.28 | 2.16 | 7.72 | 7.50 | ns |
| 12 mA | –F | 0.72 | 7.42 | 0.05 | 1.57 | 0.51 | 7.56 | 7.11 | 3.97 | 3.99 | 10.25 | 9.80 | ns |
| | Std. | 0.60 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | –1 | 0.51 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | –2 | 0.45 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |
| 16 mA | –F | 0.72 | 6.92 | 0.05 | 1.57 | 0.51 | 7.05 | 6.64 | 4.04 | 4.13 | 9.74 | 9.32 | ns |
| | Std. | 0.60 | 5.76 | 0.04 | 1.31 | 0.43 | 5.87 | 5.53 | 3.36 | 3.44 | 8.11 | 7.76 | ns |
| | –1 | 0.51 | 4.90 | 0.04 | 1.11 | 0.36 | 4.99 | 4.70 | 2.86 | 2.92 | 6.90 | 6.60 | ns |
| | –2 | 0.45 | 4.30 | 0.03 | 0.98 | 0.32 | 4.38 | 4.13 | 2.51 | 2.57 | 6.05 | 5.80 | ns |
| 24 mA | –F | 0.72 | 6.61 | 0.05 | 1.57 | 0.51 | 6.61 | 6.61 | 4.13 | 4.65 | 9.30 | 9.30 | ns |
| | Std. | 0.60 | 5.51 | 0.04 | 1.31 | 0.43 | 5.50 | 5.51 | 3.43 | 3.87 | 7.74 | 7.74 | ns |
| | –1 | 0.51 | 4.68 | 0.04 | 1.11 | 0.36 | 4.68 | 4.68 | 2.92 | 3.29 | 6.58 | 6.59 | ns |
| | –2 | 0.45 | 4.11 | 0.03 | 0.98 | 0.32 | 4.11 | 4.11 | 2.56 | 2.89 | 5.78 | 5.78 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-53 • 2.5 V LVC MOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | -F | 0.79 | 9.94 | 0.05 | 1.56 | 0.51 | 8.90 | 9.94 | 2.70 | 2.49 | 11.58 | 12.63 | ns |
| | Std. | 0.66 | 8.28 | 0.04 | 1.30 | 0.43 | 7.41 | 8.28 | 2.25 | 2.07 | 9.64 | 10.51 | ns |
| | -1 | 0.56 | 7.04 | 0.04 | 1.10 | 0.36 | 6.30 | 7.04 | 1.92 | 1.76 | 8.20 | 8.94 | ns |
| | -2 | 0.49 | 6.18 | 0.03 | 0.97 | 0.32 | 5.53 | 6.18 | 1.68 | 1.55 | 7.20 | 7.85 | ns |
| 6 mA | -F | 0.79 | 5.83 | 0.05 | 1.56 | 0.51 | 5.58 | 5.83 | 3.11 | 3.26 | 8.27 | 8.52 | ns |
| | Std. | 0.66 | 4.85 | 0.04 | 1.30 | 0.43 | 4.65 | 4.85 | 2.59 | 2.71 | 6.88 | 7.09 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 1.10 | 0.36 | 3.95 | 4.13 | 2.20 | 2.31 | 5.85 | 6.03 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.97 | 0.32 | 3.47 | 3.62 | 1.93 | 2.02 | 5.14 | 5.29 | ns |
| 8 mA | -F | 0.79 | 5.83 | 0.05 | 1.56 | 0.51 | 5.58 | 5.83 | 3.11 | 3.26 | 8.27 | 8.52 | ns |
| | Std. | 0.66 | 4.85 | 0.04 | 1.30 | 0.43 | 4.65 | 4.85 | 2.59 | 2.71 | 6.88 | 7.09 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 1.10 | 0.36 | 3.95 | 4.13 | 2.20 | 2.31 | 5.85 | 6.03 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.97 | 0.32 | 3.47 | 3.62 | 1.93 | 2.02 | 5.14 | 5.29 | ns |
| 12 mA | -F | 0.79 | 3.85 | 0.05 | 1.56 | 0.51 | 3.92 | 3.77 | 3.39 | 3.74 | 6.61 | 6.46 | ns |
| | Std. | 0.66 | 3.21 | 0.04 | 1.30 | 0.43 | 3.27 | 3.14 | 2.82 | 3.11 | 5.50 | 5.38 | ns |
| | -1 | 0.56 | 2.73 | 0.04 | 1.10 | 0.36 | 2.78 | 2.67 | 2.40 | 2.65 | 4.68 | 4.57 | ns |
| | -2 | 0.49 | 2.39 | 0.03 | 0.97 | 0.32 | 2.44 | 2.35 | 2.11 | 2.32 | 4.11 | 4.02 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-54 • 2.5 V LVC MOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | –F | 0.79 | 13.02 | 0.05 | 1.56 | 0.51 | 12.78 | 13.02 | 2.71 | 2.39 | 15.46 | 15.71 | ns |
| | Std. | 0.66 | 10.84 | 0.04 | 1.30 | 0.43 | 10.64 | 10.84 | 2.26 | 1.99 | 12.87 | 13.08 | ns |
| | –1 | 0.56 | 9.22 | 0.04 | 1.10 | 0.36 | 9.05 | 9.22 | 1.92 | 1.69 | 10.95 | 11.12 | ns |
| | –2 | 0.49 | 8.10 | 0.03 | 0.97 | 0.32 | 7.94 | 8.10 | 1.68 | 1.49 | 9.61 | 9.77 | ns |
| 6 mA | –F | 0.79 | 8.85 | 0.05 | 1.56 | 0.51 | 9.01 | 8.84 | 3.11 | 3.14 | 11.70 | 11.53 | ns |
| | Std. | 0.66 | 7.37 | 0.04 | 1.30 | 0.43 | 7.50 | 7.36 | 2.59 | 2.61 | 9.74 | 9.60 | ns |
| | –1 | 0.56 | 6.27 | 0.04 | 1.10 | 0.36 | 6.38 | 6.26 | 2.20 | 2.22 | 8.29 | 8.16 | ns |
| | –2 | 0.49 | 5.50 | 0.03 | 0.97 | 0.32 | 5.60 | 5.50 | 1.93 | 1.95 | 7.27 | 7.17 | ns |
| 8 mA | –F | 0.79 | 8.85 | 0.05 | 1.56 | 0.51 | 9.01 | 8.84 | 3.11 | 3.14 | 11.70 | 11.53 | ns |
| | Std. | 0.66 | 7.37 | 0.04 | 1.30 | 0.43 | 7.50 | 7.36 | 2.59 | 2.61 | 9.74 | 9.60 | ns |
| | –1 | 0.56 | 6.27 | 0.04 | 1.10 | 0.36 | 6.38 | 6.26 | 2.20 | 2.22 | 8.29 | 8.16 | ns |
| | –2 | 0.49 | 5.50 | 0.03 | 0.97 | 0.32 | 5.60 | 5.50 | 1.93 | 1.95 | 7.27 | 7.17 | ns |
| 12 mA | –F | 0.79 | 6.76 | 0.05 | 1.56 | 0.51 | 6.89 | 6.61 | 3.40 | 3.62 | 9.57 | 9.30 | ns |
| | Std. | 0.66 | 5.63 | 0.04 | 1.30 | 0.43 | 5.73 | 5.51 | 2.83 | 3.01 | 7.97 | 7.74 | ns |
| | –1 | 0.56 | 4.79 | 0.04 | 1.10 | 0.36 | 4.88 | 4.68 | 2.41 | 2.56 | 6.78 | 6.59 | ns |
| | –2 | 0.49 | 4.20 | 0.03 | 0.97 | 0.32 | 4.28 | 4.11 | 2.11 | 2.25 | 5.95 | 5.78 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-55 • 2.5 V LVC MOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | -F | 0.79 | 9.86 | 0.05 | 1.55 | 0.51 | 8.70 | 9.86 | 2.44 | 2.29 | ns |
| | Std. | 0.66 | 8.20 | 0.04 | 1.29 | 0.43 | 7.24 | 8.20 | 2.03 | 1.91 | ns |
| | -1 | 0.56 | 6.98 | 0.04 | 1.10 | 0.36 | 6.16 | 6.98 | 1.73 | 1.62 | ns |
| | -2 | 0.49 | 6.13 | 0.03 | 0.96 | 0.32 | 5.41 | 6.13 | 1.52 | 1.43 | ns |
| 4 mA | -F | 0.79 | 9.86 | 0.05 | 1.55 | 0.51 | 8.70 | 9.86 | 2.44 | 2.29 | ns |
| | Std. | 0.66 | 8.20 | 0.04 | 1.29 | 0.43 | 7.24 | 8.20 | 2.03 | 1.91 | ns |
| | -1 | 0.56 | 6.98 | 0.04 | 1.10 | 0.36 | 6.16 | 6.98 | 1.73 | 1.62 | ns |
| | -2 | 0.49 | 6.13 | 0.03 | 0.96 | 0.32 | 5.41 | 6.13 | 1.52 | 1.43 | ns |
| 6 mA | -F | 0.79 | 5.72 | 0.05 | 1.55 | 0.51 | 5.47 | 5.72 | 2.86 | 3.07 | ns |
| | Std. | 0.66 | 4.77 | 0.04 | 1.29 | 0.43 | 4.55 | 4.77 | 2.38 | 2.55 | ns |
| | -1 | 0.56 | 4.05 | 0.04 | 1.10 | 0.36 | 3.87 | 4.05 | 2.03 | 2.17 | ns |
| | -2 | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 8 mA | -F | 0.79 | 5.72 | 0.05 | 1.55 | 0.51 | 5.47 | 5.72 | 2.86 | 3.07 | ns |
| | Std. | 0.66 | 4.77 | 0.04 | 1.29 | 0.43 | 4.55 | 4.77 | 2.38 | 2.55 | ns |
| | -1 | 0.56 | 4.05 | 0.04 | 1.10 | 0.36 | 3.87 | 4.05 | 2.03 | 2.17 | ns |
| | -2 | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-56 • 2.5 V LVCMOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | –F | 0.79 | 13.21 | 0.05 | 1.55 | 0.51 | 12.46 | 13.21 | 2.44 | 2.20 | ns |
| | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | –1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | –2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 4 mA | –F | 0.79 | 13.21 | 0.05 | 1.55 | 0.51 | 12.46 | 13.21 | 2.44 | 2.20 | ns |
| | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | –1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | –2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 6 mA | –F | 0.79 | 9.01 | 0.05 | 1.55 | 0.51 | 8.84 | 9.01 | 2.87 | 2.96 | ns |
| | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |
| 8 mA | –F | 0.79 | 9.01 | 0.05 | 1.55 | 0.51 | 8.84 | 9.01 | 2.87 | 2.96 | ns |
| | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-57 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

| 1.8 V LVCMOS | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} | I _{OSL} | I _{OSH} | I _{IL} | I _{IH} |
|-----------------|-----------------|-------------------------|-------------------------|---------|-----------------|-------------------------|-----------------|-----------------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA ² | μA ² |
| 2 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-58 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

| 1.8 V LVCMOS | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} | I _{OSL} | I _{OSH} | I _{IL} | I _{IH} |
|-----------------|-----------------|-------------------------|-------------------------|---------|-----------------|-------------------------|-----------------|-----------------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA ² | μA ² |
| 2 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * V _{CCI} | 0.65 * V _{CCI} | 3.6 | 0.45 | V _{CCI} - 0.45 | 8 | 8 | 44 | 35 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-59 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks**

| 1.8 V LVCMOS | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|-----------------|----------|------------------|------------------|---------|----------|------------------|----------|----------|-----------------------|-----------------------|-----------|-----------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA^2 | μA^2 |
| 2 mA | -0.3 | $0.35 * V_{CC1}$ | $0.65 * V_{CC1}$ | 3.6 | 0.45 | $V_{CC1} - 0.45$ | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | -0.3 | $0.35 * V_{CC1}$ | $0.65 * V_{CC1}$ | 3.6 | 0.45 | $V_{CC1} - 0.45$ | 4 | 4 | 17 | 22 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

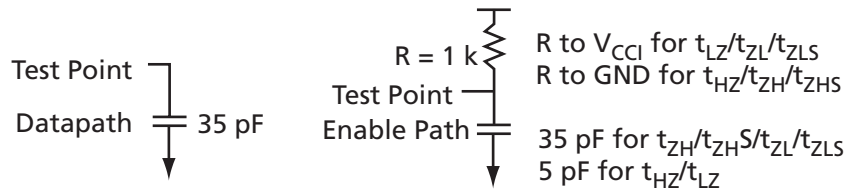


Figure 2-8 • AC Loading

Table 2-60 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | C_{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|
| 0 | 1.8 | 0.9 | 35 |

* Measuring point = V_{trip} . See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-61 • 1.8 V LVC MOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | -F | 0.79 | 14.25 | 0.05 | 1.46 | 0.51 | 10.97 | 14.25 | 3.33 | 1.99 | 13.66 | 16.94 | ns |
| | Std. | 0.66 | 11.86 | 0.04 | 1.22 | 0.43 | 9.14 | 11.86 | 2.77 | 1.66 | 11.37 | 14.10 | ns |
| | -1 | 0.56 | 10.09 | 0.04 | 1.04 | 0.36 | 7.77 | 10.09 | 2.36 | 1.41 | 9.67 | 11.99 | ns |
| | -2 | 0.49 | 8.86 | 0.03 | 0.91 | 0.32 | 6.82 | 8.86 | 2.07 | 1.24 | 8.49 | 10.53 | ns |
| 4 mA | -F | 0.79 | 8.31 | 0.05 | 1.46 | 0.51 | 7.04 | 8.31 | 3.87 | 3.41 | 9.73 | 10.99 | ns |
| | Std. | 0.66 | 6.91 | 0.04 | 1.22 | 0.43 | 5.86 | 6.91 | 3.22 | 2.84 | 8.10 | 9.15 | ns |
| | -1 | 0.56 | 5.88 | 0.04 | 1.04 | 0.36 | 4.99 | 5.88 | 2.74 | 2.41 | 6.89 | 7.78 | ns |
| | -2 | 0.49 | 5.16 | 0.03 | 0.91 | 0.32 | 4.38 | 5.16 | 2.41 | 2.12 | 6.05 | 6.83 | ns |
| 6 mA | -F | 0.79 | 5.34 | 0.05 | 1.46 | 0.51 | 5.02 | 5.34 | 4.24 | 4.06 | 7.71 | 8.03 | ns |
| | Std. | 0.66 | 4.45 | 0.04 | 1.22 | 0.43 | 4.18 | 4.45 | 3.53 | 3.38 | 6.42 | 6.68 | ns |
| | -1 | 0.56 | 3.78 | 0.04 | 1.04 | 0.36 | 3.56 | 3.78 | 3.00 | 2.88 | 5.46 | 5.69 | ns |
| | -2 | 0.49 | 3.32 | 0.03 | 0.91 | 0.32 | 3.12 | 3.32 | 2.64 | 2.53 | 4.79 | 4.99 | ns |
| 8 mA | -F | 0.79 | 4.71 | 0.05 | 1.46 | 0.51 | 4.72 | 4.71 | 4.32 | 4.23 | 7.40 | 7.40 | ns |
| | Std. | 0.66 | 3.92 | 0.04 | 1.22 | 0.43 | 3.93 | 3.92 | 3.60 | 3.52 | 6.16 | 6.16 | ns |
| | -1 | 0.56 | 3.34 | 0.04 | 1.04 | 0.36 | 3.34 | 3.34 | 3.06 | 3.00 | 5.24 | 5.24 | ns |
| | -2 | 0.49 | 2.93 | 0.03 | 0.91 | 0.32 | 2.93 | 2.93 | 2.69 | 2.63 | 4.60 | 4.60 | ns |
| 12 mA | -F | 0.79 | 4.24 | 0.05 | 1.46 | 0.51 | 4.32 | 3.65 | 4.45 | 4.90 | 7.01 | 6.34 | ns |
| | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | -1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |
| 16 mA | -F | 0.79 | 4.24 | 0.05 | 1.46 | 0.51 | 4.32 | 3.65 | 4.45 | 4.90 | 7.01 | 6.34 | ns |
| | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | -1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-62 • 1.8 V LVC MOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | –F | 0.79 | 18.66 | 0.05 | 1.46 | 0.51 | 16.95 | 18.66 | 3.34 | 1.92 | 19.64 | 21.34 | ns |
| | Std. | 0.66 | 15.53 | 0.04 | 1.22 | 0.43 | 14.11 | 15.53 | 2.78 | 1.60 | 16.35 | 17.77 | ns |
| | –1 | 0.56 | 13.21 | 0.04 | 1.04 | 0.36 | 12.01 | 13.21 | 2.36 | 1.36 | 13.91 | 15.11 | ns |
| | –2 | 0.49 | 11.60 | 0.03 | 0.91 | 0.32 | 10.54 | 11.60 | 2.07 | 1.19 | 12.21 | 13.27 | ns |
| 4 mA | –F | 0.79 | 12.58 | 0.05 | 1.46 | 0.51 | 12.51 | 12.58 | 3.88 | 3.28 | 15.19 | 15.27 | ns |
| | Std. | 0.66 | 10.48 | 0.04 | 1.22 | 0.43 | 10.41 | 10.48 | 3.23 | 2.73 | 12.65 | 12.71 | ns |
| | –1 | 0.56 | 8.91 | 0.04 | 1.04 | 0.36 | 8.86 | 8.91 | 2.75 | 2.33 | 10.76 | 10.81 | ns |
| | –2 | 0.49 | 7.82 | 0.03 | 0.91 | 0.32 | 7.77 | 7.82 | 2.41 | 2.04 | 9.44 | 9.49 | ns |
| 6 mA | –F | 0.79 | 9.67 | 0.05 | 1.46 | 0.51 | 9.85 | 9.42 | 4.25 | 3.93 | 12.53 | 12.11 | ns |
| | Std. | 0.66 | 8.05 | 0.04 | 1.22 | 0.43 | 8.20 | 7.84 | 3.54 | 3.27 | 10.43 | 10.08 | ns |
| | –1 | 0.56 | 6.85 | 0.04 | 1.04 | 0.36 | 6.97 | 6.67 | 3.01 | 2.78 | 8.88 | 8.57 | ns |
| | –2 | 0.49 | 6.01 | 0.03 | 0.91 | 0.32 | 6.12 | 5.86 | 2.64 | 2.44 | 7.79 | 7.53 | ns |
| 8 mA | –F | 0.79 | 9.01 | 0.05 | 1.46 | 0.51 | 9.18 | 8.77 | 4.33 | 4.10 | 11.87 | 11.45 | ns |
| | Std. | 0.66 | 7.50 | 0.04 | 1.22 | 0.43 | 7.64 | 7.30 | 3.61 | 3.41 | 9.88 | 9.53 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.04 | 0.36 | 6.50 | 6.21 | 3.07 | 2.90 | 8.40 | 8.11 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.91 | 0.32 | 5.71 | 5.45 | 2.69 | 2.55 | 7.38 | 7.12 | ns |
| 12 mA | –F | 0.79 | 8.76 | 0.05 | 1.46 | 0.51 | 8.69 | 8.76 | 4.45 | 4.74 | 11.38 | 11.45 | ns |
| | Std. | 0.66 | 7.29 | 0.04 | 1.22 | 0.43 | 7.23 | 7.29 | 3.71 | 3.95 | 9.47 | 9.53 | ns |
| | –1 | 0.56 | 6.20 | 0.04 | 1.04 | 0.36 | 6.15 | 6.20 | 3.15 | 3.36 | 8.06 | 8.11 | ns |
| | –2 | 0.49 | 5.45 | 0.03 | 0.91 | 0.32 | 5.40 | 5.45 | 2.77 | 2.95 | 7.07 | 7.12 | ns |
| 16 mA | –F | 0.79 | 8.76 | 0.05 | 1.46 | 0.51 | 8.69 | 8.76 | 4.45 | 4.74 | 11.38 | 11.45 | ns |
| | Std. | 0.66 | 7.29 | 0.04 | 1.22 | 0.43 | 7.23 | 7.29 | 3.71 | 3.95 | 9.47 | 9.53 | ns |
| | –1 | 0.56 | 6.20 | 0.04 | 1.04 | 0.36 | 6.15 | 6.20 | 3.15 | 3.36 | 8.06 | 8.11 | ns |
| | –2 | 0.49 | 5.45 | 0.03 | 0.91 | 0.32 | 5.40 | 5.45 | 2.77 | 2.95 | 7.07 | 7.12 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-63 • 1.8 V LVC MOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | -F | 0.79 | 13.61 | 0.05 | 1.44 | 0.51 | 10.48 | 13.61 | 2.70 | 1.83 | 13.17 | 16.30 | ns |
| | Std. | 0.66 | 11.33 | 0.04 | 1.20 | 0.43 | 8.72 | 11.33 | 2.24 | 1.52 | 10.96 | 13.57 | ns |
| | -1 | 0.56 | 9.64 | 0.04 | 1.02 | 0.36 | 7.42 | 9.64 | 1.91 | 1.29 | 9.32 | 11.54 | ns |
| | -2 | 0.49 | 8.46 | 0.03 | 0.90 | 0.32 | 6.51 | 8.46 | 1.68 | 1.14 | 8.18 | 10.13 | ns |
| 4 mA | -F | 0.79 | 7.79 | 0.05 | 1.44 | 0.51 | 6.58 | 7.79 | 3.18 | 3.13 | 9.27 | 10.47 | ns |
| | Std. | 0.66 | 6.48 | 0.04 | 1.20 | 0.43 | 5.48 | 6.48 | 2.65 | 2.60 | 7.72 | 8.72 | ns |
| | -1 | 0.56 | 5.51 | 0.04 | 1.02 | 0.36 | 4.66 | 5.51 | 2.25 | 2.21 | 6.56 | 7.42 | ns |
| | -2 | 0.49 | 4.84 | 0.03 | 0.90 | 0.32 | 4.09 | 4.84 | 1.98 | 1.94 | 5.76 | 6.51 | ns |
| 6 mA | -F | 0.79 | 4.88 | 0.05 | 1.44 | 0.51 | 4.61 | 4.88 | 3.52 | 3.73 | 7.30 | 7.56 | ns |
| | Std. | 0.66 | 4.06 | 0.04 | 1.20 | 0.43 | 3.84 | 4.06 | 2.93 | 3.10 | 6.07 | 6.30 | ns |
| | -1 | 0.56 | 3.45 | 0.04 | 1.02 | 0.36 | 3.27 | 3.45 | 2.49 | 2.64 | 5.17 | 5.36 | ns |
| | -2 | 0.49 | 3.03 | 0.03 | 0.90 | 0.32 | 2.87 | 3.03 | 2.19 | 2.32 | 4.54 | 4.70 | ns |
| 8 mA | -F | 0.79 | 4.88 | 0.05 | 1.44 | 0.51 | 4.61 | 4.88 | 3.52 | 3.73 | 7.30 | 7.56 | ns |
| | Std. | 0.66 | 4.06 | 0.04 | 1.20 | 0.43 | 3.84 | 4.06 | 2.93 | 3.10 | 6.07 | 6.30 | ns |
| | -1 | 0.56 | 3.45 | 0.04 | 1.02 | 0.36 | 3.27 | 3.45 | 2.49 | 2.64 | 5.17 | 5.36 | ns |
| | -2 | 0.49 | 3.03 | 0.03 | 0.90 | 0.32 | 2.87 | 3.03 | 2.19 | 2.32 | 4.54 | 4.70 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-64 • 1.8 V LVC MOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | -F | 0.79 | 17.78 | 0.05 | 1.44 | 0.51 | 16.21 | 17.78 | 2.70 | 1.76 | 18.90 | 20.47 | ns |
| | Std. | 0.66 | 14.80 | 0.04 | 1.20 | 0.43 | 13.49 | 14.80 | 2.25 | 1.46 | 15.73 | 17.04 | ns |
| | -1 | 0.56 | 12.59 | 0.04 | 1.02 | 0.36 | 11.48 | 12.59 | 1.91 | 1.25 | 13.38 | 14.49 | ns |
| | -2 | 0.49 | 11.05 | 0.03 | 0.90 | 0.32 | 10.08 | 11.05 | 1.68 | 1.09 | 11.75 | 12.72 | ns |
| 4 mA | -F | 0.79 | 11.89 | 0.05 | 1.44 | 0.51 | 11.69 | 11.89 | 3.19 | 3.00 | 14.38 | 14.58 | ns |
| | Std. | 0.66 | 9.90 | 0.04 | 1.20 | 0.43 | 9.73 | 9.90 | 2.65 | 2.50 | 11.97 | 12.13 | ns |
| | -1 | 0.56 | 8.42 | 0.04 | 1.02 | 0.36 | 8.28 | 8.42 | 2.26 | 2.12 | 10.18 | 10.32 | ns |
| | -2 | 0.49 | 7.39 | 0.03 | 0.90 | 0.32 | 7.27 | 7.39 | 1.98 | 1.86 | 8.94 | 9.06 | ns |
| 6 mA | -F | 0.79 | 8.93 | 0.05 | 1.44 | 0.51 | 9.10 | 8.79 | 3.53 | 3.59 | 11.79 | 11.48 | ns |
| | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | -1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | -2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |
| 8 mA | -F | 0.79 | 8.93 | 0.05 | 1.44 | 0.51 | 9.10 | 8.79 | 3.53 | 3.59 | 11.79 | 11.48 | ns |
| | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | -1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | -2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-65 • 1.8 V LVC MOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | -F | 0.79 | 13.47 | 0.05 | 1.44 | 0.51 | 10.25 | 13.47 | 2.39 | 1.45 | ns |
| | Std. | 0.66 | 11.21 | 0.04 | 1.20 | 0.43 | 8.53 | 11.21 | 1.99 | 1.21 | ns |
| | -1 | 0.56 | 9.54 | 0.04 | 1.02 | 0.36 | 7.26 | 9.54 | 1.69 | 1.03 | ns |
| | -2 | 0.49 | 8.37 | 0.03 | 0.90 | 0.32 | 6.37 | 8.37 | 1.49 | 0.90 | ns |
| 4 mA | -F | 0.79 | 7.62 | 0.05 | 1.44 | 0.51 | 6.46 | 7.62 | 2.89 | 2.98 | ns |
| | Std. | 0.66 | 6.34 | 0.04 | 1.20 | 0.43 | 5.38 | 6.34 | 2.41 | 2.48 | ns |
| | -1 | 0.56 | 5.40 | 0.04 | 1.02 | 0.36 | 4.58 | 5.40 | 2.05 | 2.11 | ns |
| | -2 | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Table 2-66 • 1.8 V LVCMOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | –F | 0.79 | 18.03 | 0.05 | 1.44 | 0.51 | 15.80 | 18.03 | 2.40 | 2.40 | ns |
| | Std. | 0.66 | 15.01 | 0.04 | 1.20 | 0.43 | 13.15 | 15.01 | 1.99 | 1.99 | ns |
| | –1 | 0.56 | 12.77 | 0.04 | 1.02 | 0.36 | 11.19 | 12.77 | 1.70 | 1.70 | ns |
| | –2 | 0.49 | 11.21 | 0.03 | 0.90 | 0.32 | 9.82 | 11.21 | 1.49 | 1.49 | ns |
| 4 mA | –F | 0.79 | 12.13 | 0.05 | 1.44 | 0.51 | 11.48 | 12.13 | 2.90 | 2.85 | ns |
| | Std. | 0.66 | 10.10 | 0.04 | 1.20 | 0.43 | 9.55 | 10.10 | 2.41 | 2.37 | ns |
| | –1 | 0.56 | 8.59 | 0.04 | 1.02 | 0.36 | 8.13 | 8.59 | 2.05 | 2.02 | ns |
| | –2 | 0.49 | 7.54 | 0.03 | 0.90 | 0.32 | 7.13 | 7.54 | 1.80 | 1.77 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-67 • Minimum and Maximum DC Input and Output Levels
 Applicable to Advanced I/O Banks

| 1.5 V LVCMOS | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|--------------|----------|------------------|-----------------|---------|------------------|------------------|----------|----------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA^2 | μA^2 |
| 2 mA | –0.3 | $0.30 * V_{CCI}$ | $0.7 * V_{CCI}$ | 3.6 | $0.25 * V_{CCI}$ | $0.75 * V_{CCI}$ | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | –0.3 | $0.30 * V_{CCI}$ | $0.7 * V_{CCI}$ | 3.6 | $0.25 * V_{CCI}$ | $0.75 * V_{CCI}$ | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | –0.3 | $0.30 * V_{CCI}$ | $0.7 * V_{CCI}$ | 3.6 | $0.25 * V_{CCI}$ | $0.75 * V_{CCI}$ | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | –0.3 | $0.30 * V_{CCI}$ | $0.7 * V_{CCI}$ | 3.6 | $0.25 * V_{CCI}$ | $0.75 * V_{CCI}$ | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | –0.3 | $0.30 * V_{CCI}$ | $0.7 * V_{CCI}$ | 3.6 | $0.25 * V_{CCI}$ | $0.75 * V_{CCI}$ | 12 | 12 | 55 | 66 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-68 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks**

| 1.5 V LVCMOS | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} | I _{OSL} | I _{OSH} | I _{IL} | I _{IH} |
|-----------------|-----------------|-------------------------|------------------------|---------|-------------------------|-------------------------|-----------------|-----------------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA ² | μA ² |
| 2 mA | -0.3 | 0.30 * V _{CC1} | 0.7 * V _{CC1} | 3.6 | 0.25 * V _{CC1} | 0.75 * V _{CC1} | 2 | 2 | 0 | 0 | 10 | 10 |
| 4 mA | -0.3 | 0.30 * V _{CC1} | 0.7 * V _{CC1} | 3.6 | 0.25 * V _{CC1} | 0.75 * V _{CC1} | 4 | 4 | 0 | 0 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-69 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks**

| 1.5 V LVCMOS | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} | I _{OH} | I _{OSL} | I _{OSH} | I _{IL} | I _{IH} |
|-----------------|-----------------|-------------------------|------------------------|---------|-------------------------|-------------------------|-----------------|-----------------|-----------------------|-----------------------|-----------------|-----------------|
| | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA ¹ | Max., mA ¹ | μA ² | μA ² |
| 2 mA | -0.3 | 0.30 * V _{CC1} | 0.7 * V _{CC1} | 3.6 | 0.25 * V _{CC1} | 0.75 * V _{CC1} | 2 | 2 | 13 | 16 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

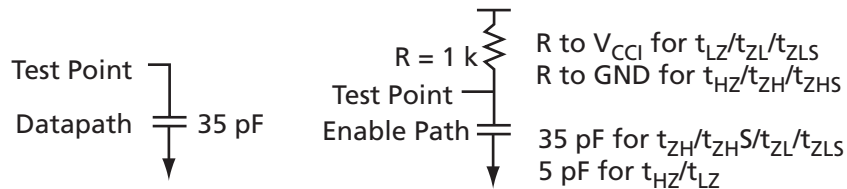


Figure 2-9 • AC Loading

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|------------------------|
| 0 | 1.5 | 0.75 | 35 |

* Measuring point = V_{trip}. See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-71 • 1.5 V LVCMOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | –F | 0.79 | 10.05 | 0.05 | 1.73 | 0.51 | 8.20 | 10.05 | 4.07 | 3.32 | 10.88 | 12.73 | ns |
| | Std. | 0.66 | 8.36 | 0.04 | 1.44 | 0.43 | 6.82 | 8.36 | 3.39 | 2.77 | 9.06 | 10.60 | ns |
| | –1 | 0.56 | 7.11 | 0.04 | 1.22 | 0.36 | 5.80 | 7.11 | 2.88 | 2.35 | 7.71 | 9.02 | ns |
| | –2 | 0.49 | 6.24 | 0.03 | 1.07 | 0.32 | 5.10 | 6.24 | 2.53 | 2.06 | 6.76 | 7.91 | ns |
| 4 mA | –F | 0.79 | 6.38 | 0.05 | 1.73 | 0.51 | 5.83 | 6.38 | 4.49 | 4.09 | 8.51 | 9.07 | ns |
| | Std. | 0.66 | 5.31 | 0.04 | 1.44 | 0.43 | 4.85 | 5.31 | 3.74 | 3.40 | 7.09 | 7.55 | ns |
| | –1 | 0.56 | 4.52 | 0.04 | 1.22 | 0.36 | 4.13 | 4.52 | 3.18 | 2.89 | 6.03 | 6.42 | ns |
| | –2 | 0.49 | 3.97 | 0.03 | 1.07 | 0.32 | 3.62 | 3.97 | 2.79 | 2.54 | 5.29 | 5.64 | ns |
| 6 mA | –F | 0.79 | 5.61 | 0.05 | 1.73 | 0.51 | 5.46 | 5.61 | 4.59 | 4.28 | 8.15 | 8.29 | ns |
| | Std. | 0.66 | 4.67 | 0.04 | 1.44 | 0.43 | 4.55 | 4.67 | 3.82 | 3.56 | 6.78 | 6.90 | ns |
| | –1 | 0.56 | 3.97 | 0.04 | 1.22 | 0.36 | 3.87 | 3.97 | 3.25 | 3.03 | 5.77 | 5.87 | ns |
| | –2 | 0.49 | 3.49 | 0.03 | 1.07 | 0.32 | 3.40 | 3.49 | 2.85 | 2.66 | 5.07 | 5.16 | ns |
| 8 mA | –F | 0.79 | 4.90 | 0.05 | 1.73 | 0.51 | 4.99 | 4.30 | 4.74 | 5.05 | 7.68 | 6.98 | ns |
| | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 12 mA | –F | 0.79 | 4.90 | 0.05 | 1.73 | 0.51 | 4.99 | 4.30 | 4.74 | 5.05 | 7.68 | 6.98 | ns |
| | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-72 • 1.5 V LVCMOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Advanced I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | –F | 0.79 | 15.36 | 0.05 | 1.73 | 0.51 | 15.39 | 15.36 | 4.08 | 3.18 | 18.07 | 18.04 | ns |
| | Std. | 0.66 | 12.78 | 0.04 | 1.44 | 0.43 | 12.81 | 12.78 | 3.40 | 2.64 | 15.05 | 15.02 | ns |
| | –1 | 0.56 | 10.87 | 0.04 | 1.22 | 0.36 | 10.90 | 10.87 | 2.89 | 2.25 | 12.80 | 12.78 | ns |
| | –2 | 0.49 | 9.55 | 0.03 | 1.07 | 0.32 | 9.57 | 9.55 | 2.54 | 1.97 | 11.24 | 11.22 | ns |
| 4 mA | –F | 0.79 | 12.02 | 0.05 | 1.73 | 0.51 | 12.25 | 11.47 | 4.50 | 3.93 | 14.93 | 14.15 | ns |
| | Std. | 0.66 | 10.01 | 0.04 | 1.44 | 0.43 | 10.19 | 9.55 | 3.75 | 3.27 | 12.43 | 11.78 | ns |
| | –1 | 0.56 | 8.51 | 0.04 | 1.22 | 0.36 | 8.67 | 8.12 | 3.19 | 2.78 | 10.57 | 10.02 | ns |
| | –2 | 0.49 | 7.47 | 0.03 | 1.07 | 0.32 | 7.61 | 7.13 | 2.80 | 2.44 | 9.28 | 8.80 | ns |
| 6 mA | –F | 0.79 | 11.21 | 0.05 | 1.73 | 0.51 | 11.42 | 10.68 | 4.60 | 4.12 | 14.11 | 13.37 | ns |
| | Std. | 0.66 | 9.33 | 0.04 | 1.44 | 0.43 | 9.51 | 8.89 | 3.83 | 3.43 | 11.74 | 11.13 | ns |
| | –1 | 0.56 | 7.94 | 0.04 | 1.22 | 0.36 | 8.09 | 7.56 | 3.26 | 2.92 | 9.99 | 9.47 | ns |
| | –2 | 0.49 | 6.97 | 0.03 | 1.07 | 0.32 | 7.10 | 6.64 | 2.86 | 2.56 | 8.77 | 8.31 | ns |
| 8 mA | –F | 0.79 | 10.70 | 0.05 | 1.73 | 0.51 | 10.90 | 10.68 | 4.75 | 4.86 | 13.59 | 13.37 | ns |
| | Std. | 0.66 | 8.91 | 0.04 | 1.44 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | –1 | 0.56 | 7.58 | 0.04 | 1.22 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | –2 | 0.49 | 6.65 | 0.03 | 1.07 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |
| 12 mA | –F | 0.79 | 10.70 | 0.05 | 1.73 | 0.51 | 10.90 | 10.68 | 4.75 | 4.86 | 13.59 | 13.37 | ns |
| | Std. | 0.66 | 8.91 | 0.04 | 1.44 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | –1 | 0.56 | 7.58 | 0.04 | 1.22 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | –2 | 0.49 | 6.65 | 0.03 | 1.07 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-73 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | -F | 0.79 | 9.41 | 0.05 | 1.71 | 0.51 | 7.71 | 9.41 | 3.25 | 3.06 | 10.40 | 12.09 | ns |
| | Std. | 0.66 | 7.83 | 0.04 | 1.42 | 0.43 | 6.42 | 7.83 | 2.71 | 2.55 | 8.65 | 10.07 | ns |
| | -1 | 0.56 | 6.66 | 0.04 | 1.21 | 0.36 | 5.46 | 6.66 | 2.31 | 2.17 | 7.36 | 8.56 | ns |
| | -2 | 0.49 | 5.85 | 0.03 | 1.06 | 0.32 | 4.79 | 5.85 | 2.02 | 1.90 | 6.46 | 7.52 | ns |
| 4 mA | -F | 0.79 | 5.81 | 0.05 | 1.71 | 0.51 | 5.39 | 5.81 | 3.64 | 3.76 | 8.08 | 8.50 | ns |
| | Std. | 0.66 | 4.84 | 0.04 | 1.42 | 0.43 | 4.49 | 4.84 | 3.03 | 3.13 | 6.72 | 7.08 | ns |
| | -1 | 0.56 | 4.12 | 0.04 | 1.21 | 0.36 | 3.82 | 4.12 | 2.58 | 2.66 | 5.72 | 6.02 | ns |
| | -2 | 0.49 | 3.61 | 0.03 | 1.06 | 0.32 | 3.35 | 3.61 | 2.26 | 2.34 | 5.02 | 5.28 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-74 • 1.5 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard Plus I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | -F | 0.79 | 14.51 | 0.05 | 1.71 | 0.51 | 14.42 | 14.51 | 3.26 | 2.91 | 17.11 | 17.20 | ns |
| | Std. | 0.66 | 12.08 | 0.04 | 1.42 | 0.43 | 12.01 | 12.08 | 2.72 | 2.43 | 14.24 | 14.31 | ns |
| | -1 | 0.56 | 10.27 | 0.04 | 1.21 | 0.36 | 10.21 | 10.27 | 2.31 | 2.06 | 12.12 | 12.18 | ns |
| | -2 | 0.49 | 9.02 | 0.03 | 1.06 | 0.32 | 8.97 | 9.02 | 2.03 | 1.81 | 10.64 | 10.69 | ns |
| 4 mA | -F | 0.79 | 11.15 | 0.05 | 1.71 | 0.51 | 11.35 | 10.71 | 3.65 | 3.60 | 14.04 | 13.40 | ns |
| | Std. | 0.66 | 9.28 | 0.04 | 1.42 | 0.43 | 9.45 | 8.91 | 3.04 | 3.00 | 11.69 | 11.15 | ns |
| | -1 | 0.56 | 7.89 | 0.04 | 1.21 | 0.36 | 8.04 | 7.58 | 2.58 | 2.55 | 9.94 | 9.49 | ns |
| | -2 | 0.49 | 6.93 | 0.03 | 1.06 | 0.32 | 7.06 | 6.66 | 2.27 | 2.24 | 8.73 | 8.33 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-75 • 1.5 V LVCMOS High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | -F | 0.79 | 9.18 | 0.05 | 1.70 | 0.51 | 7.58 | 9.18 | 2.94 | 2.94 | ns |
| | Std. | 0.66 | 7.65 | 0.04 | 1.42 | 0.43 | 6.31 | 7.65 | 2.45 | 2.45 | ns |
| | -1 | 0.56 | 6.50 | 0.04 | 1.21 | 0.36 | 5.37 | 6.50 | 2.08 | 2.08 | ns |
| | -2 | 0.49 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-76 • 1.5 V LVCMOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/O Banks

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | -F | 0.79 | 14.81 | 0.05 | 1.70 | 0.51 | 14.17 | 14.81 | 2.94 | 2.79 | ns |
| | Std. | 0.66 | 12.33 | 0.04 | 1.42 | 0.43 | 11.79 | 12.33 | 2.45 | 2.32 | ns |
| | -1 | 0.56 | 10.49 | 0.04 | 1.21 | 0.36 | 10.03 | 10.49 | 2.08 | 1.98 | ns |
| | -2 | 0.49 | 9.21 | 0.03 | 1.06 | 0.32 | 8.81 | 9.21 | 1.83 | 1.73 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-77 • Minimum and Maximum DC Input and Output Levels

| 3.3 V PCI/PCI-X | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|-----------------------|----------------|--------|----------|--------|----------|----------|----------|----------|----------------------|----------------------|-----------------|-----------------|
| Drive Strength | Min, V | Max, V | Min, V | Max, V | Max, V | Min, V | mA | mA | Max, mA ¹ | Max, mA ¹ | μA^2 | μA^2 |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 2-10.

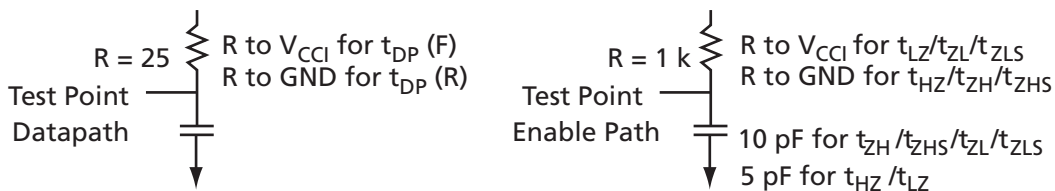


Figure 2-10 • AC Loading



AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-78.

Table 2-78 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|--|------------------------|
| 0 | 3.3 | 0.285 * V _{CCI} for t _{DP(R)} 0.615 * V _{CCI} for t _{DP(F)} | 10 |

* Measuring point = V_{trip}. See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-79 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| -F | 0.79 | 3.22 | 0.05 | 1.04 | 0.51 | 3.28 | 2.34 | 3.86 | 4.30 | 5.97 | 5.03 | ns |
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | ns |
| -1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | ns |
| -2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-80 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| -F | 0.79 | 2.77 | 0.05 | 1.02 | 0.51 | 2.82 | 2.05 | 3.35 | 3.87 | 5.51 | 4.73 | ns |
| Std. | 0.66 | 2.31 | 0.04 | 0.85 | 0.43 | 2.35 | 1.70 | 2.79 | 3.22 | 4.59 | 3.94 | ns |
| -1 | 0.56 | 1.96 | 0.04 | 0.72 | 0.36 | 2.00 | 1.45 | 2.37 | 2.74 | 3.90 | 3.35 | ns |
| -2 | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-11](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

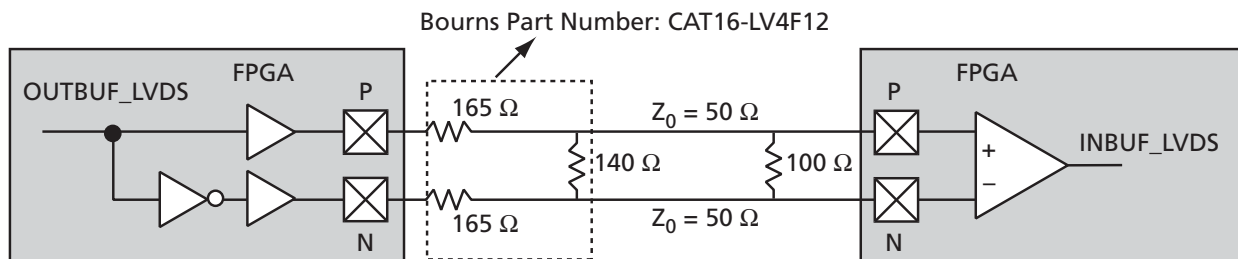


Figure 2-11 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-81 • LVDS Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|------------------------------|---|-------|-------|-------|-------|
| V _{CCI} | Supply Voltage ¹ | 2.375 | 2.5 | 2.625 | V |
| V _{OL} | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| V _{OH} | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| I _{OL} ⁴ | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| I _{OH} ⁴ | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| V _I | Input Voltage | 0 | | 2.925 | V |
| I _{IH} ³ | Input High Leakage Current | | | 10 | μA |
| I _{IL} ³ | Input Low Leakage Current | | | 10 | μA |
| V _{ODIFF} | Differential Output Voltage | 250 | 350 | 450 | mV |
| V _{OCM} | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| V _{ICM} | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| V _{IDIFF} | Input Differential Voltage ² | 100 | 350 | | mV |

Notes:

- ±5%
- Differential input voltage = ±350 mV.
- Currents are measured at 85°C junction temperature.
- I_{OL}/I_{OH} defined by V_{ODIFF}/(Resistor Network).

Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) |
|---------------|----------------|----------------------|
| 1.075 | 1.325 | Cross point |

* Measuring point = V_{trip}. See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-83 • LVDS

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------|
| -F | 0.79 | 2.20 | 0.05 | 1.92 | ns |
| Std. | 0.66 | 1.83 | 0.04 | 1.60 | ns |
| -1 | 0.56 | 1.56 | 0.04 | 1.36 | ns |
| -2 | 0.49 | 1.37 | 0.03 | 1.20 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-12. The input and output buffer delays are available in the LVDS section in Table 2-83.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$ given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").

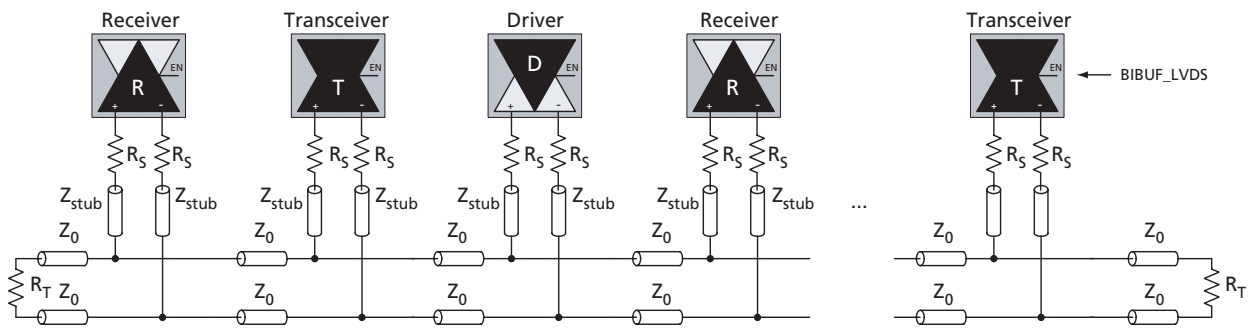


Figure 2-12 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

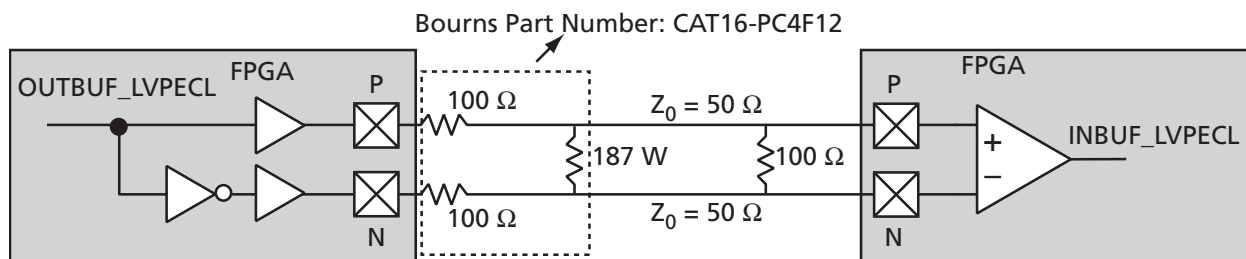


Figure 2-13 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-84 • Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|------------------|--------------------------------|-------|------|-------|------|-------|------|-------|
| V_{CCI} | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| V_{OL} | Output LOW Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| V_{OH} | Output HIGH Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| V_{IL}, V_{IH} | Input LOW, Input HIGH Voltages | 0 | 3.3 | 0 | 3.6 | 0 | 3.9 | V |
| V_{ODIFF} | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| V_{OCM} | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| V_{ICM} | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| V_{IDIFF} | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

Table 2-85 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) |
|---------------|----------------|----------------------|
| 1.64 | 1.94 | Cross point |

* Measuring point = V_{trip} . See Table 2-22 on page 2-20 for a complete table of trip points.

Timing Characteristics

Table 2-86 • LVPECL

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{pY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| -F | 0.79 | 2.16 | 0.05 | 1.69 | ns |
| Std. | 0.66 | 1.80 | 0.04 | 1.40 | ns |
| -1 | 0.56 | 1.53 | 0.04 | 1.19 | ns |
| -2 | 0.49 | 1.34 | 0.03 | 1.05 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

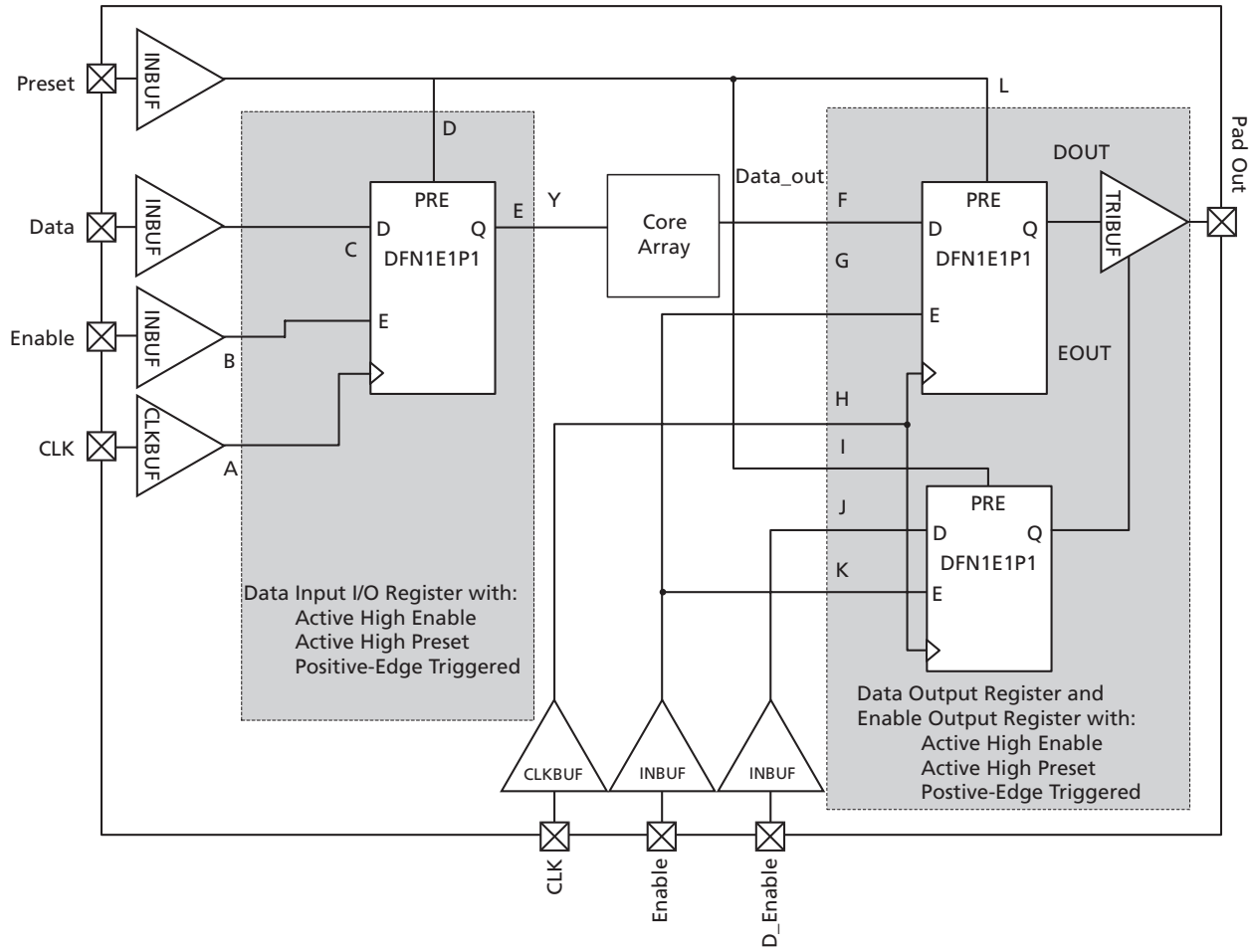


Figure 2-14 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-87 • Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------------|--|-----------------------------|
| t _{OCLKQ} | Clock-to-Q of the Output Data Register | H, DOUT |
| t _{OSUD} | Data Setup Time for the Output Data Register | F, H |
| t _{OHD} | Data Hold Time for the Output Data Register | F, H |
| t _{OSUE} | Enable Setup Time for the Output Data Register | G, H |
| t _{OHE} | Enable Hold Time for the Output Data Register | G, H |
| t _{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| t _{OEMPRE} | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| t _{ORECPRE} | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| t _{OCLKQ} | Clock-to-Q of the Output Enable Register | H, EOUT |
| t _{OESUD} | Data Setup Time for the Output Enable Register | J, H |
| t _{OEH} | Data Hold Time for the Output Enable Register | J, H |
| t _{OESUE} | Enable Setup Time for the Output Enable Register | K, H |
| t _{OEH} | Enable Hold Time for the Output Enable Register | K, H |
| t _{OEPRE2Q} | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| t _{OEMPRE} | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| t _{OERCPRE} | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| t _{ICKQ} | Clock-to-Q of the Input Data Register | A, E |
| t _{ISUD} | Data Setup Time for the Input Data Register | C, A |
| t _{IHD} | Data Hold Time for the Input Data Register | C, A |
| t _{ISUE} | Enable Setup Time for the Input Data Register | B, A |
| t _{IHE} | Enable Hold Time for the Input Data Register | B, A |
| t _{IPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| t _{IEMPRE} | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| t _{IRECPRE} | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

* See Figure 2-14 on page 2-62 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

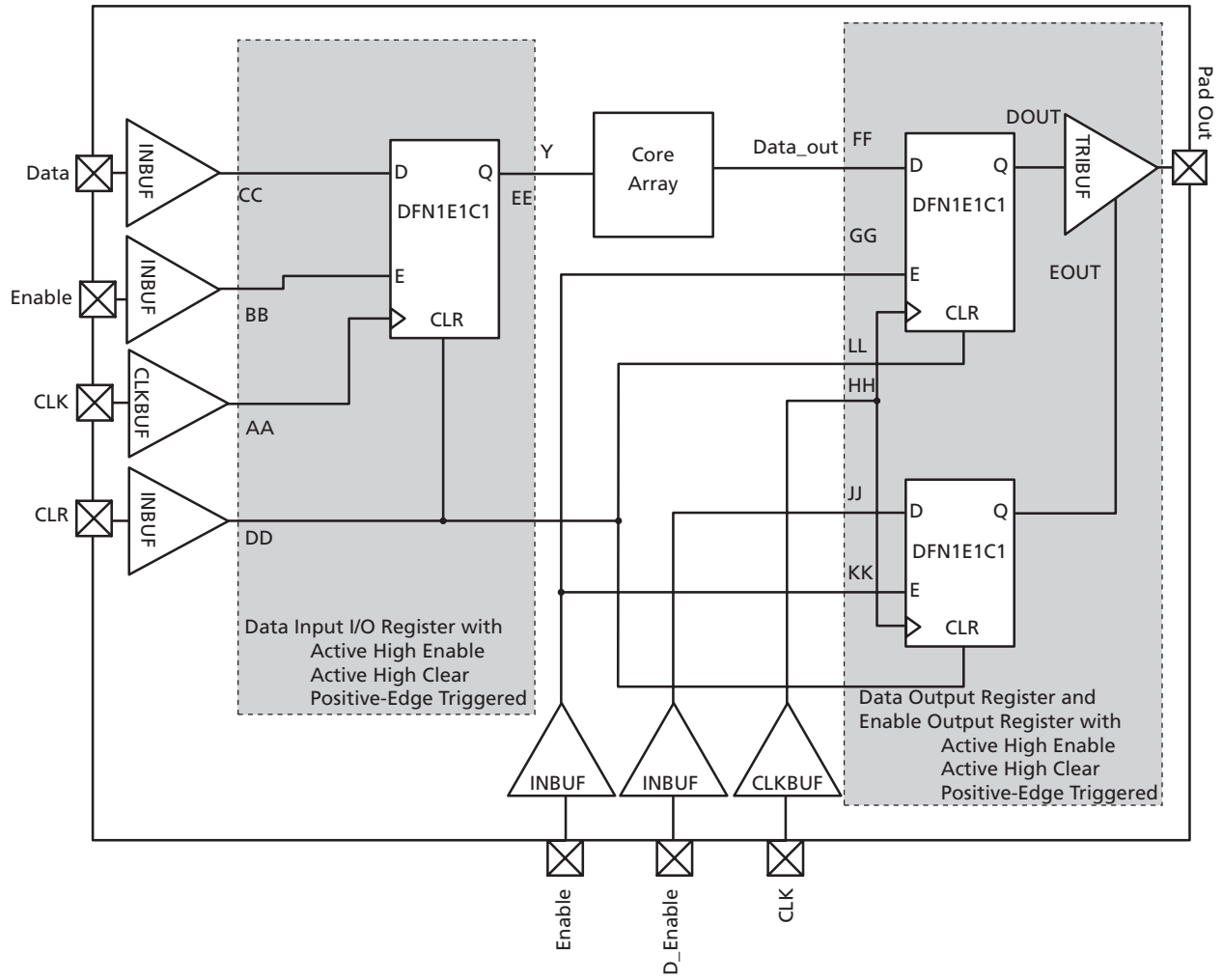


Figure 2-15 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-88 • Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|-----------------------|---|-----------------------------|
| t _{OCLKQ} | Clock-to-Q of the Output Data Register | HH, DOUT |
| t _{OSUD} | Data Setup Time for the Output Data Register | FF, HH |
| t _{OHD} | Data Hold Time for the Output Data Register | FF, HH |
| t _{OSUE} | Enable Setup Time for the Output Data Register | GG, HH |
| t _{OHE} | Enable Hold Time for the Output Data Register | GG, HH |
| t _{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| t _{OREMCLR} | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| t _{ORECCLR} | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| t _{OECLKQ} | Clock-to-Q of the Output Enable Register | HH, EOUT |
| t _{OESUD} | Data Setup Time for the Output Enable Register | JJ, HH |
| t _{OEH} | Data Hold Time for the Output Enable Register | JJ, HH |
| t _{OESUE} | Enable Setup Time for the Output Enable Register | KK, HH |
| t _{OEH} | Enable Hold Time for the Output Enable Register | KK, HH |
| t _{OECLR2Q} | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| t _{OEREMCLR} | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| t _{OERECCLR} | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| t _{ICLKQ} | Clock-to-Q of the Input Data Register | AA, EE |
| t _{ISUD} | Data Setup Time for the Input Data Register | CC, AA |
| t _{IHD} | Data Hold Time for the Input Data Register | CC, AA |
| t _{ISUE} | Enable Setup Time for the Input Data Register | BB, AA |
| t _{IHE} | Enable Hold Time for the Input Data Register | BB, AA |
| t _{ICLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| t _{IREMCLR} | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| t _{IRECCLR} | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

* See Figure 2-15 on page 2-64 for more information.

Input Register

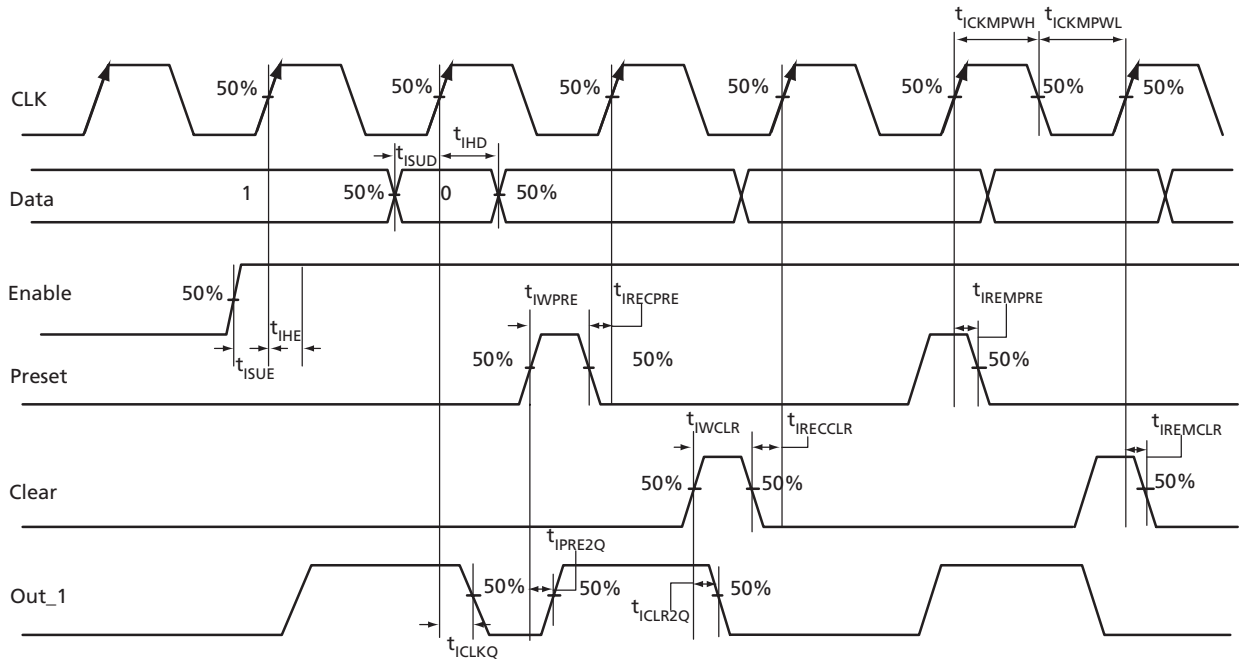


Figure 2-16 • Input Register Timing Diagram

Timing Characteristics

Table 2-89 • Input Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ICLKQ} | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | 0.38 | ns |
| t_{ISUD} | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | 0.42 | ns |
| t_{IHD} | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{ISUE} | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | 0.60 | ns |
| t_{IHE} | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{ICLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | 0.73 | ns |
| t_{IPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | 0.73 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{IWCLR} | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{IWPRE} | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.36 | 0.41 | 0.48 | 0.57 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width LOW for the Input Data Register | 0.32 | 0.37 | 0.43 | 0.52 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Register

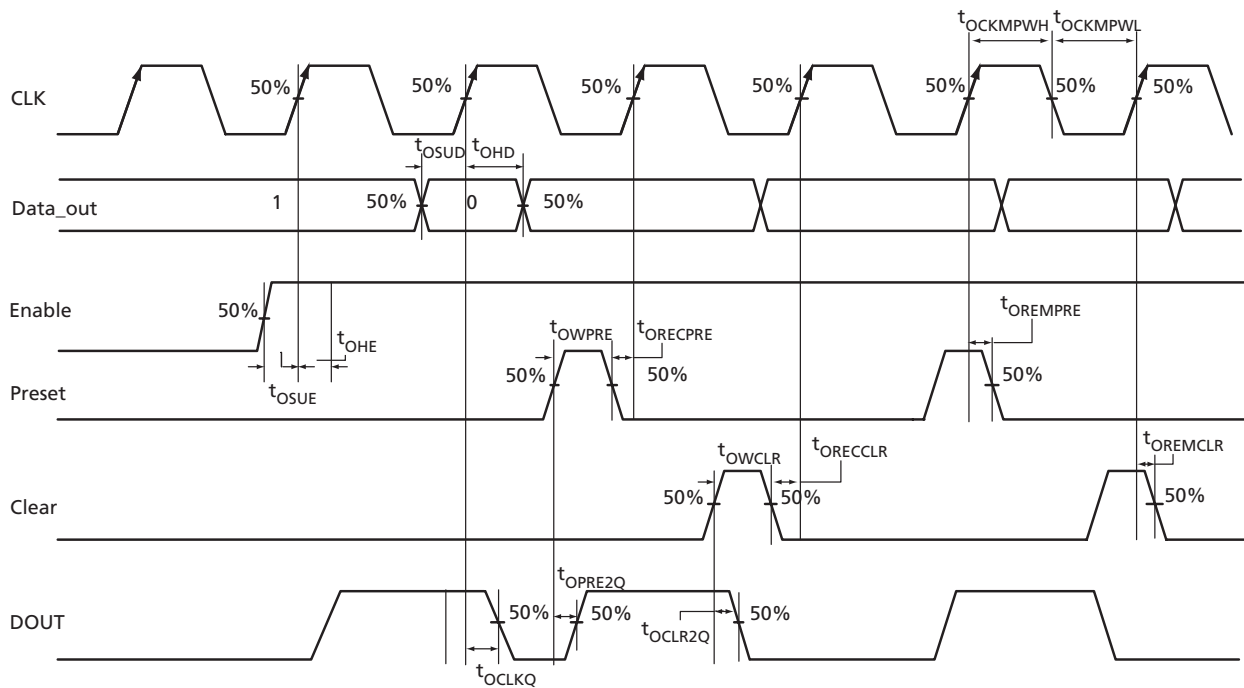


Figure 2-17 • Output Register Timing Diagram

Timing Characteristics

Table 2-90 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|--|------|------|------|------|-------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | 0.59 | 0.67 | 0.79 | 0.95 | ns |
| t_{OSUD} | Data Setup Time for the Output Data Register | 0.31 | 0.36 | 0.42 | 0.50 | ns |
| t_{OHD} | Data Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{OSUE} | Enable Setup Time for the Output Data Register | 0.44 | 0.50 | 0.59 | 0.70 | ns |
| t_{OHE} | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | 1.29 | ns |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | 1.29 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{OWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{OWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.36 | 0.41 | 0.48 | 0.57 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Data Register | 0.32 | 0.37 | 0.43 | 0.52 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Enable Register

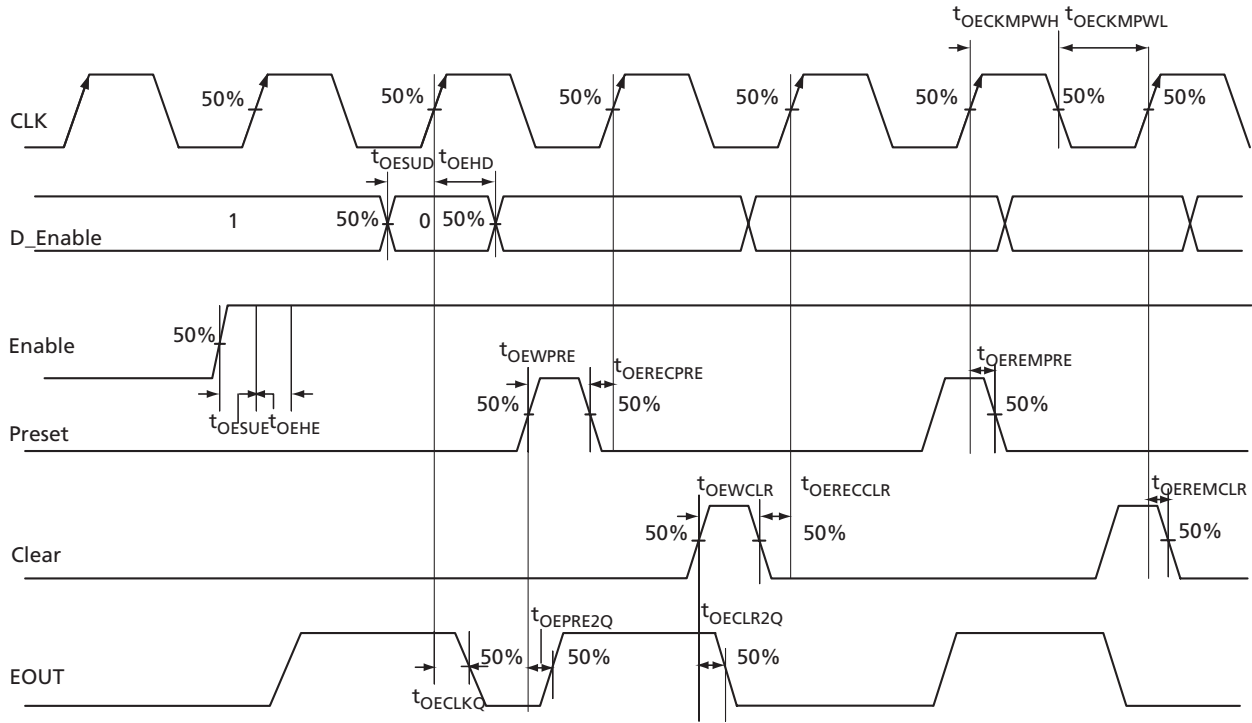


Figure 2-18 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-91 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|----------------|--|------|------|------|------|-------|
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | 0.59 | 0.67 | 0.79 | 0.95 | ns |
| t_{OESUD} | Data Setup Time for the Output Enable Register | 0.31 | 0.36 | 0.42 | 0.50 | ns |
| t_{OEHD} | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | 0.44 | 0.50 | 0.58 | 0.70 | ns |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | 1.07 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | 1.07 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{OEWCCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{OEWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.36 | 0.41 | 0.48 | 0.57 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.32 | 0.37 | 0.43 | 0.52 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

DDR Module Specifications

Input DDR Module

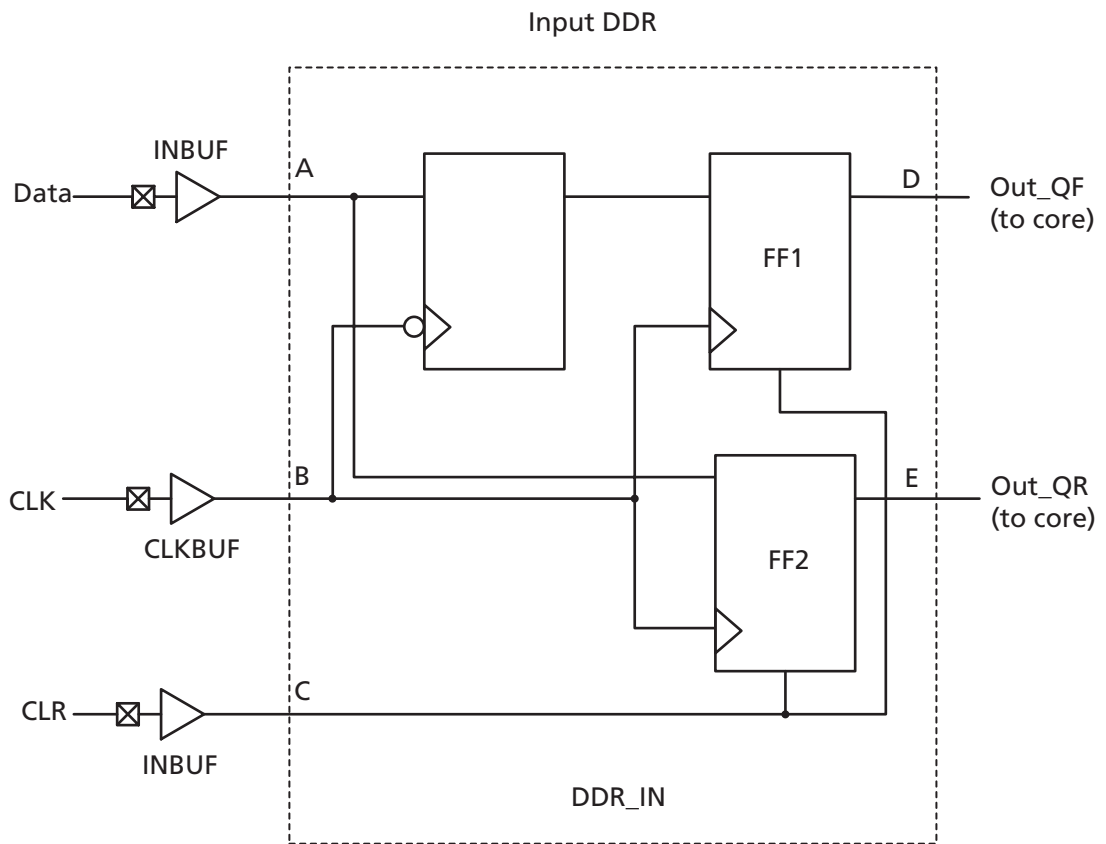
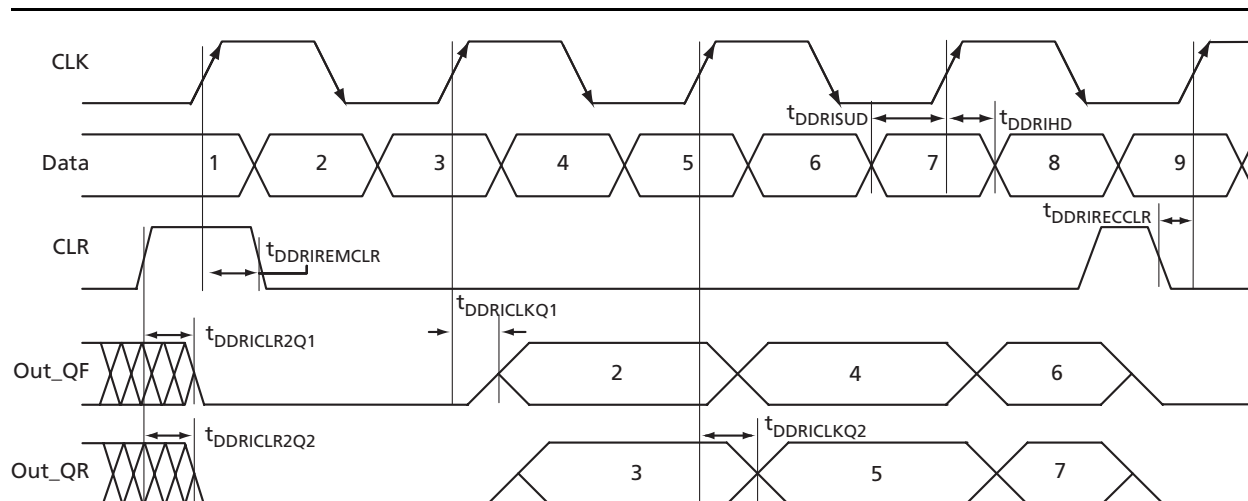


Figure 2-19 • Input DDR Timing Model

Table 2-92 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|------------------------------|----------------------------|
| $t_{DDRICKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| t_{DDRIHD} | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |


Figure 2-20 • Input DDR Timing Diagram

Timing Characteristics

Table 2-93 • Input DDR Propagation Delays

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|-------------------------|--|------|------|------|------|-------|
| t_{DDRICKQ1} | Clock-to-Out Out_QR for Input DDR | 0.27 | 0.31 | 0.37 | 0.44 | ns |
| t_{DDRICKQ2} | Clock-to-Out Out_QF for Input DDR | 0.39 | 0.44 | 0.52 | 0.62 | ns |
| t_{DDRISUD} | Data Setup for Input DDR (Fall) | 0.25 | 0.28 | 0.33 | 0.40 | ns |
| | Data Setup for Input DDR (Rise) | 0.25 | 0.28 | 0.33 | 0.40 | ns |
| t_{DDRIHD} | Data Hold for Input DDR (Fall) | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| | Data Hold for Input DDR (Rise) | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRICLR2Q1}}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 0.46 | 0.53 | 0.62 | 0.74 | ns |
| $t_{\text{DDRICLR2Q2}}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.57 | 0.65 | 0.76 | 0.92 | ns |
| $t_{\text{DDRIREMCLR}}$ | Asynchronous Clear Removal time for Input DDR | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRIRECCLR}}$ | Asynchronous Clear Recovery time for Input DDR | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{DDRIWCLR} | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{\text{DDRICKMPWH}}$ | Clock Minimum Pulse Width High for Input DDR | 0.36 | 0.41 | 0.48 | 0.57 | ns |
| $t_{\text{DDRICKMPWL}}$ | Clock Minimum Pulse Width Low for Input DDR | 0.32 | 0.37 | 0.43 | 0.52 | ns |
| F_{DDRIMAX} | Maximum Frequency for Input DDR | | | | | MHz |

Note: For specific junction temperature and voltage-supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Output DDR Module

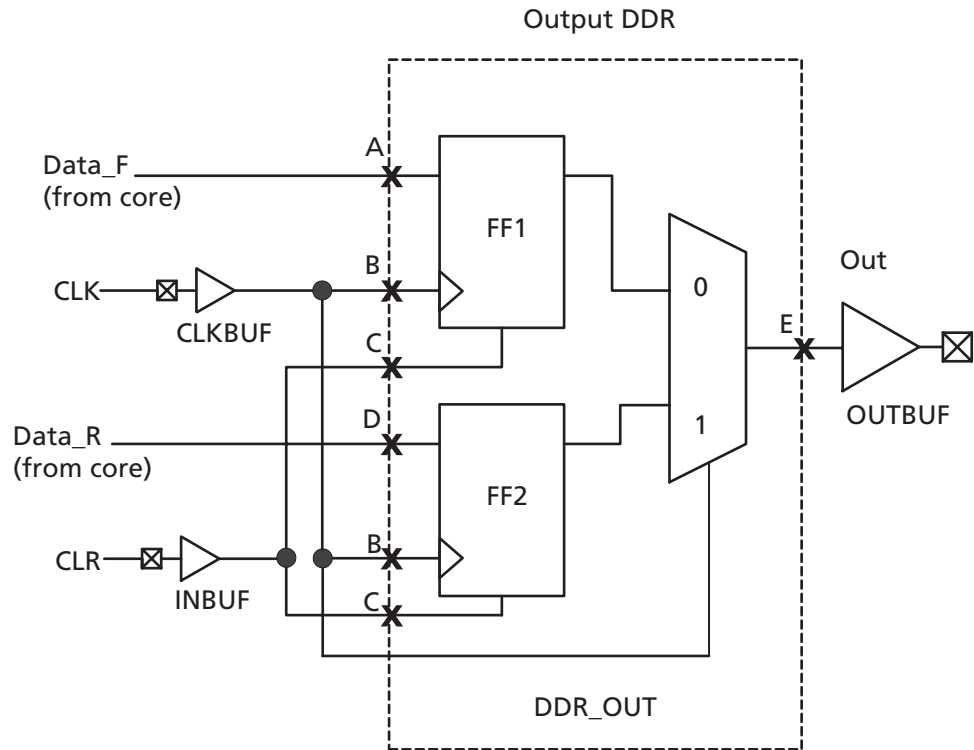
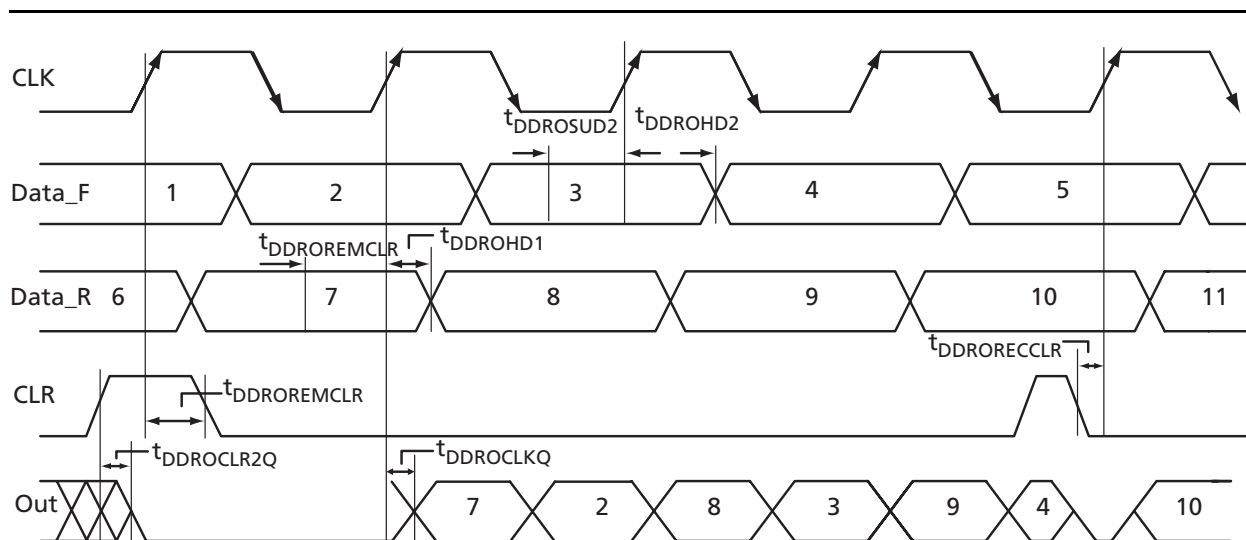


Figure 2-21 • Output DDR Timing Model

Table 2-94 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|---------------------------|----------------------------|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |


Figure 2-22 • Output DDR Timing Diagram

Timing Characteristics

Table 2-95 • Output DDR Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|-------------------------|---|------|------|------|------|-------|
| t_{DDROCLKQ} | Clock-to-Out of DDR for Output DDR | 0.70 | 0.80 | 0.94 | 1.13 | ns |
| t_{DDROSUD1} | Data_F Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | 0.61 | ns |
| t_{DDROSUD2} | Data_R Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | 0.61 | ns |
| t_{DDROHD1} | Data_F Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DDROHD2} | Data_R Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDROCLR2Q}}$ | Asynchronous Clear-to-Out for Output DDR | 0.80 | 0.91 | 1.07 | 1.29 | ns |
| $t_{\text{DDROEMCLR}}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDROECCLR}}$ | Asynchronous Clear Recovery Time for Output DDR | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{\text{DDROWCLR1}}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| $t_{\text{DDROCKMPWH}}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.36 | 0.41 | 0.48 | 0.57 | ns |
| $t_{\text{DDROCKMPWL}}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.32 | 0.37 | 0.43 | 0.52 | ns |
| F_{DDOMAX} | Maximum Frequency for the Output DDR | TBD | TBD | TBD | TBD | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO[®]le, and ProASIC3/E Macro Library Guide*.

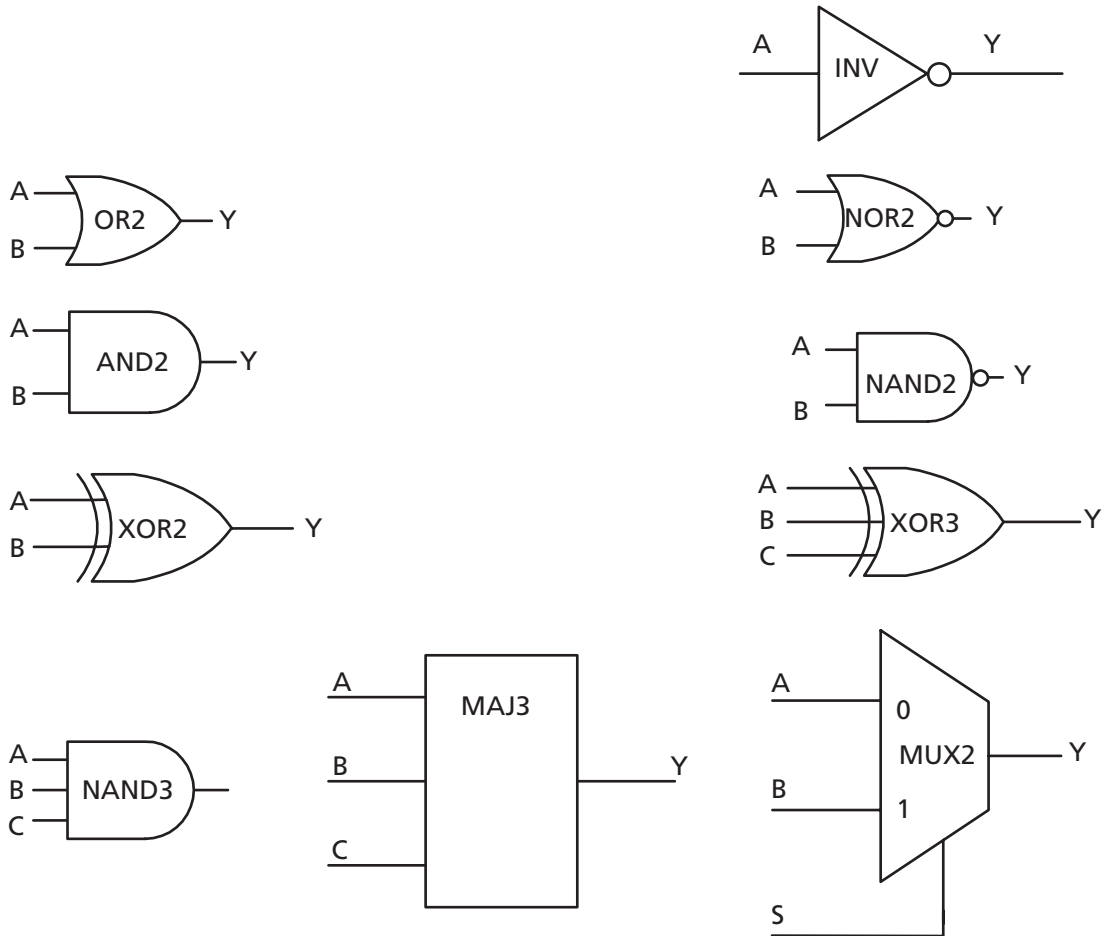


Figure 2-23 • Sample of Combinatorial Cells

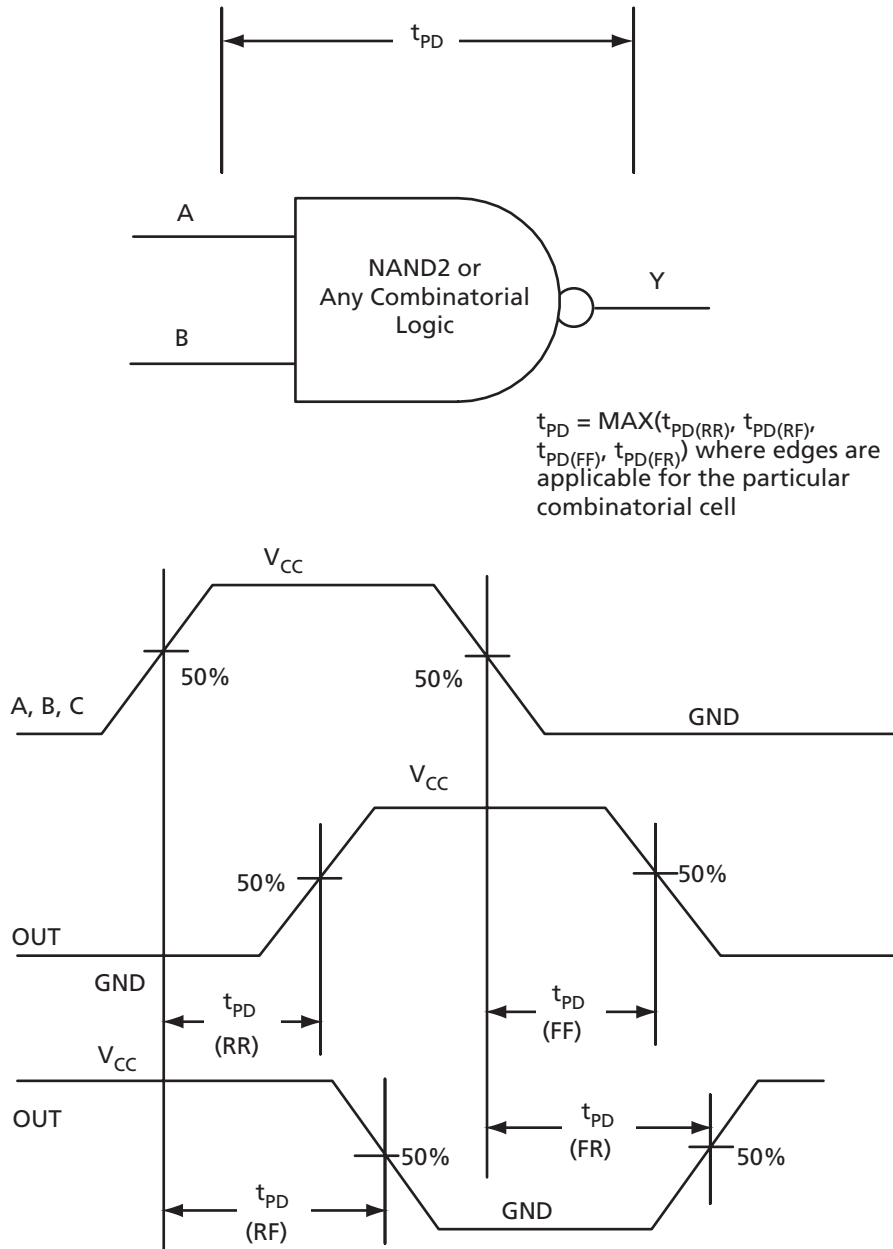


Figure 2-24 • Timing Model and Waveforms

Timing Characteristics

Table 2-96 • Combinatorial Cell Propagation Delays
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Combinatorial Cell | Equation | Parameter | -2 | -1 | Std. | -F | Units |
|--------------------|---------------------------|-----------|------|------|------|------|-------|
| INV | $Y = !A$ | t_{PD} | 0.40 | 0.46 | 0.54 | 0.65 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 0.47 | 0.54 | 0.63 | 0.76 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 0.47 | 0.54 | 0.63 | 0.76 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 0.49 | 0.55 | 0.65 | 0.78 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 0.49 | 0.55 | 0.65 | 0.78 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 0.74 | 0.84 | 0.99 | 1.19 | ns |
| MAJ3 | $Y = \text{MAJ}(A, B, C)$ | t_{PD} | 0.70 | 0.79 | 0.93 | 1.12 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 0.87 | 1.00 | 1.17 | 1.41 | ns |
| MUX2 | $Y = A !S + B S$ | t_{PD} | 0.51 | 0.58 | 0.68 | 0.81 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 0.56 | 0.64 | 0.75 | 0.90 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion, IGLOOe, and ProASIC3IE Macro Library Guide](#).

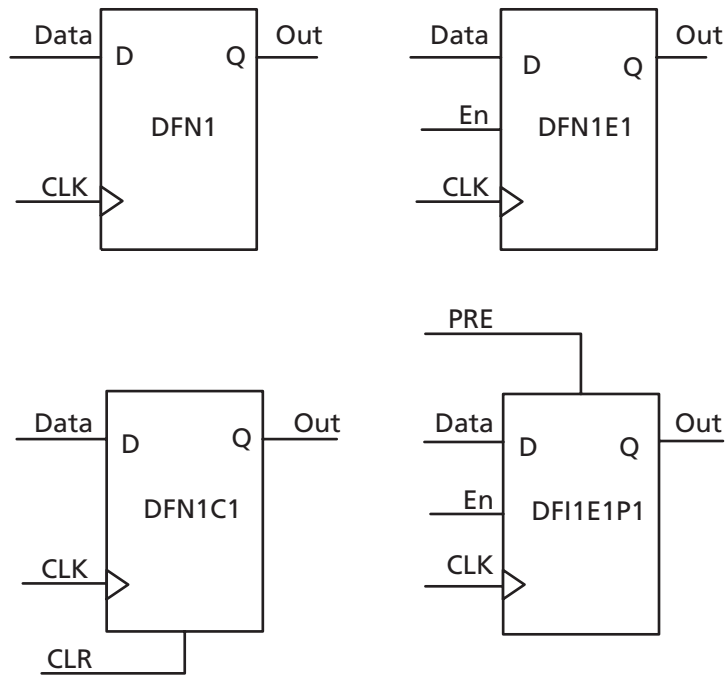
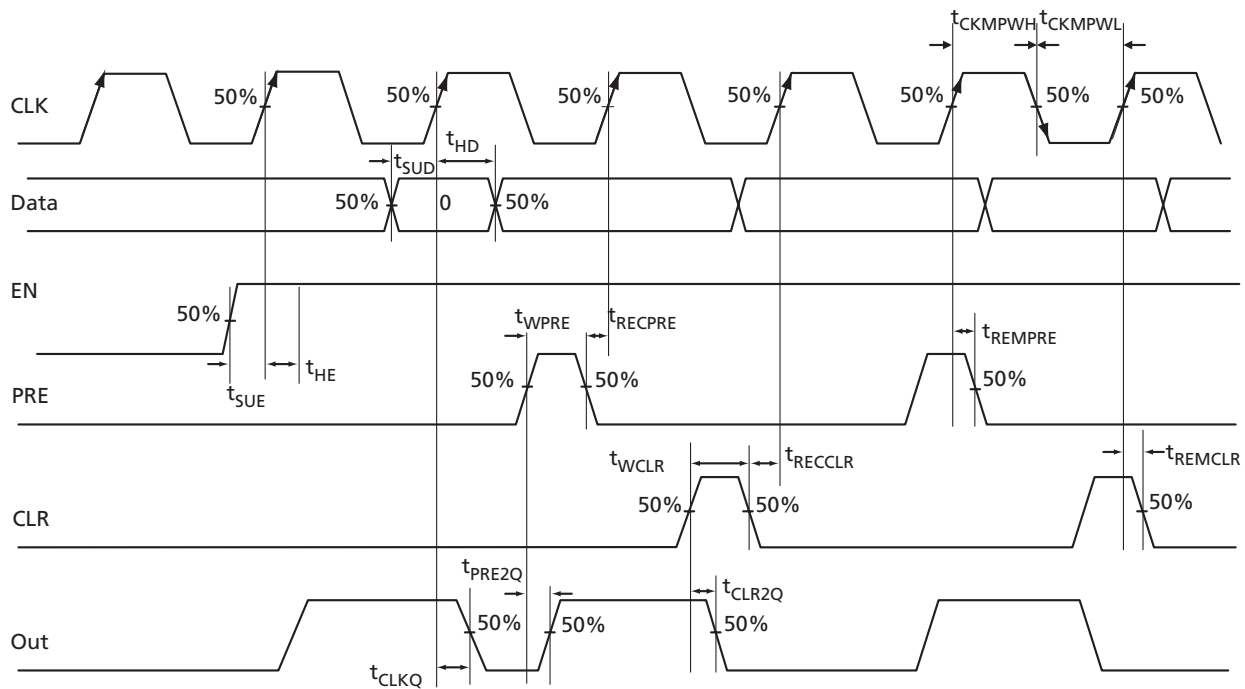


Figure 2-25 • Sample of Sequential Cells


Figure 2-26 • Timing Model and Waveforms

Timing Characteristics

Table 2-97 • Register Delays

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|--------------|---|------|------|------|------|-------|
| t_{CLKQ} | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | 0.89 | ns |
| t_{SUD} | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | 0.69 | ns |
| t_{HD} | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | 0.73 | ns |
| t_{HE} | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | 0.64 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | 0.64 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{RECLL} | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | 0.36 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width HIGH for the Core Register | 0.32 | 0.37 | 0.43 | 0.52 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width LOW for the Core Register | 0.36 | 0.41 | 0.48 | 0.57 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-27 is an example of a global tree used for clock routing. The global tree presented in Figure 2-27 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

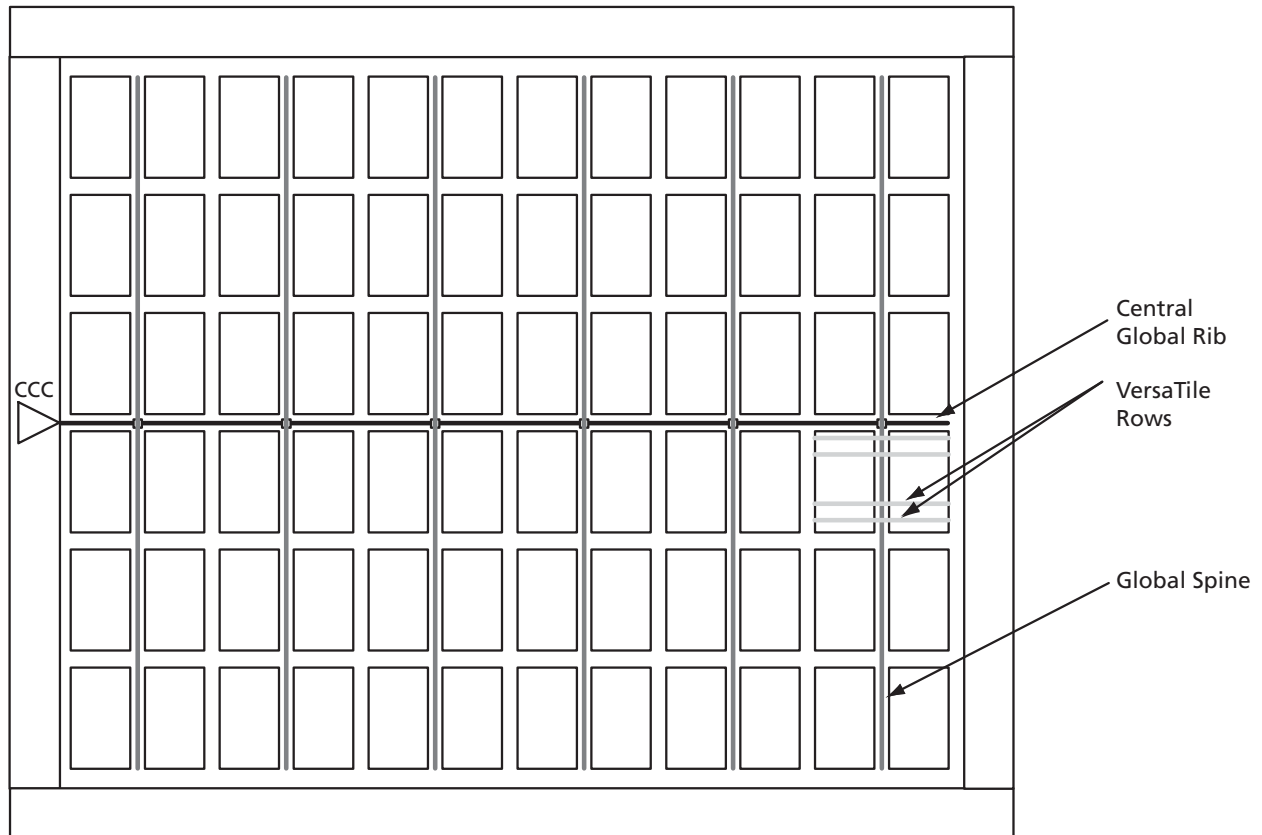


Figure 2-27 • Example of Global Tree Use in an A3P250 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-83. Table 2-99 to Table 2-105 on page 2-82 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-98 • A3P015 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t _{RCKL} | Input LOW Delay for Global Clock | 0.66 | 0.81 | 0.75 | 0.92 | 0.88 | 1.08 | 1.06 | 1.30 | ns |
| t _{RCKH} | Input HIGH Delay for Global Clock | 0.67 | 0.84 | 0.76 | 0.96 | 0.89 | 1.13 | 1.07 | 1.36 | ns |
| t _{RCKMPWH} | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| t _{RCKMPWL} | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t _{RCKSW} | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.25 | | 0.30 | ns |
| F _{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-99 • A3P030 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t _{RCKL} | Input LOW Delay for Global Clock | 0.67 | 0.81 | 0.76 | 0.92 | 0.89 | 1.09 | 1.07 | 1.31 | ns |
| t _{RCKH} | Input HIGH Delay for Global Clock | 0.68 | 0.85 | 0.77 | 0.97 | 0.91 | 1.14 | 1.09 | 1.37 | ns |
| t _{RCKMPWH} | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| t _{RCKMPWL} | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t _{RCKSW} | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.24 | | 0.29 | ns |
| F _{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-100 • A3P060 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input LOW Delay for Global Clock | 0.71 | 0.93 | 0.81 | 1.05 | 0.95 | 1.24 | 1.14 | 1.49 | ns |
| t_{RCKH} | Input HIGH Delay for Global Clock | 0.70 | 0.96 | 0.80 | 1.09 | 0.94 | 1.28 | 1.13 | 1.54 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | | 0.41 | ns |
| F_{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-101 • A3P125 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input LOW Delay for Global Clock | 0.77 | 0.99 | 0.87 | 1.12 | 1.03 | 1.32 | 1.24 | 1.58 | ns |
| t_{RCKH} | Input HIGH Delay for Global Clock | 0.76 | 1.02 | 0.87 | 1.16 | 1.02 | 1.37 | 1.23 | 1.64 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | | 0.41 | ns |
| F_{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-102 • A3P250 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input LOW Delay for Global Clock | 0.80 | 1.01 | 0.91 | 1.15 | 1.07 | 1.36 | 1.28 | 1.63 | ns |
| t_{RCKH} | Input HIGH Delay for Global Clock | 0.78 | 1.04 | 0.89 | 1.18 | 1.04 | 1.39 | 1.25 | 1.66 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | | 0.41 | ns |
| F_{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-103 • A3P400 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input LOW Delay for Global Clock | 0.87 | 1.09 | 0.99 | 1.24 | 1.17 | 1.46 | 1.40 | 1.75 | ns |
| t_{RCKH} | Input HIGH Delay for Global Clock | 0.86 | 1.11 | 0.98 | 1.27 | 1.15 | 1.49 | 1.38 | 1.79 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | | 0.41 | ns |
| F_{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | Mhz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-104 • A3P600 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input LOW Delay for Global Clock | 0.87 | 1.09 | 0.99 | 1.24 | 1.17 | 1.46 | 1.40 | 1.75 | ns |
| t_{RCKH} | Input HIGH Delay for Global Clock | 0.86 | 1.11 | 0.98 | 1.27 | 1.15 | 1.49 | 1.38 | 1.79 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | | 0.41 | ns |
| F_{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-105 • A3P1000 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | -F | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input LOW Delay for Global Clock | 0.94 | 1.16 | 1.07 | 1.32 | 1.26 | 1.55 | 1.51 | 1.86 | ns |
| t_{RCKH} | Input HIGH Delay for Global Clock | 0.93 | 1.19 | 1.06 | 1.35 | 1.24 | 1.59 | 1.49 | 1.91 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.35 | | 0.41 | ns |
| F_{RMAX} | Maximum Frequency for Global Clock | | | | | | | | | MHz |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

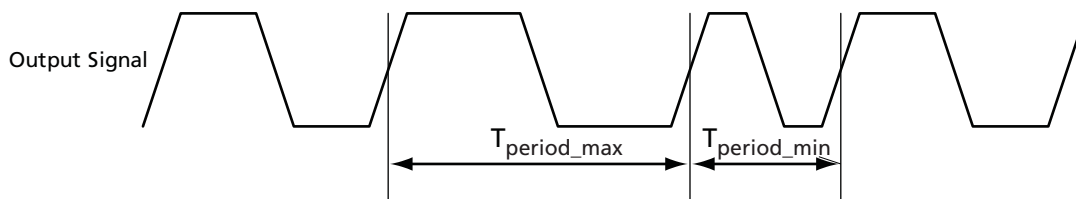
Timing Characteristics

Table 2-106 • ProASIC3 CCC/PLL Specification

| Parameter | Minimum | Typical | Maximum | Units |
|--|--------------------------------|---------|------------------------|-------|
| Clock Conditioning Circuitry Input Frequency f_{IN_CCC} | 1.5 | | 350 | MHz |
| Clock Conditioning Circuitry Output Frequency f_{OUT_CCC} | 0.75 | | 350 | MHz |
| Serial Clock (SCLK) for Dynamic PLL ¹ | | | 125 | MHz |
| Delay Increments in Programmable Delay Blocks ^{2, 3} | | 200 | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Input Period Jitter | | | 1.5 | ns |
| CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | | 0.70% | |
| 24 MHz to 100 MHz | 1.00% | | 1.20% | |
| 100 MHz to 250 MHz | 1.75% | | 2.00% | |
| 250 MHz to 350 MHz | 2.50% | | 5.60% | |
| Acquisition Time | | | | |
| (A3P250 and A3P1000 only) LockControl = 0 | | | 300 | μs |
| LockControl = 1 | | | 300 | μs |
| (all other dies) LockControl = 0 | | | 300 | μs |
| LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter ⁵ | | | | |
| (A3P250 and A3P1000 only) LockControl = 0 | | | 1.6 | ns |
| LockControl = 1 | | | 1.6 | ns |
| (all other dies) LockControl = 0 | | | 1.6 | ns |
| LockControl = 1 | | | 0.8 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay ^{1, 2, 3} | 0.6 | | 5.56 | ns |
| Delay Range in Block: Programmable Delay ^{2, 3} | 0.025 | | 5.56 | ns |
| Delay Range in Block: Fixed Delay ^{2, 3} | | 2.2 | | ns |

Notes:

1. Maximum value obtained for a -2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
2. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) for deratings.
3. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
4. The A3P030 device does not contain a PLL.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-28 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

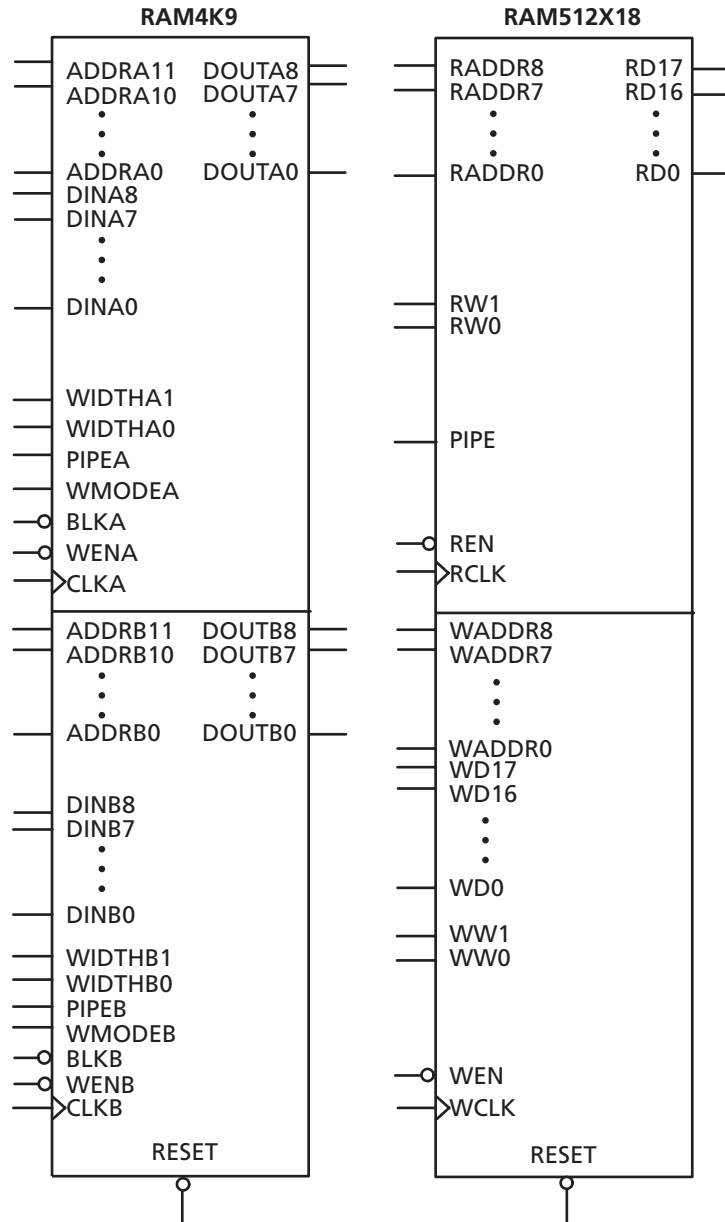


Figure 2-29 • RAM Models

Timing Waveforms

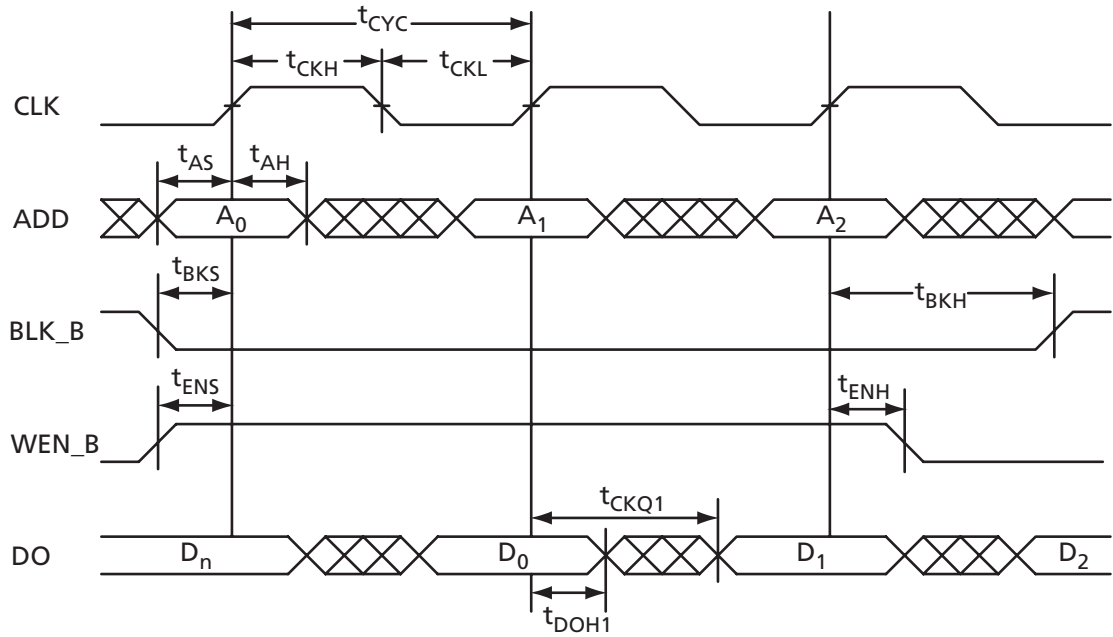


Figure 2-30 • RAM Read for Pass-Through Output

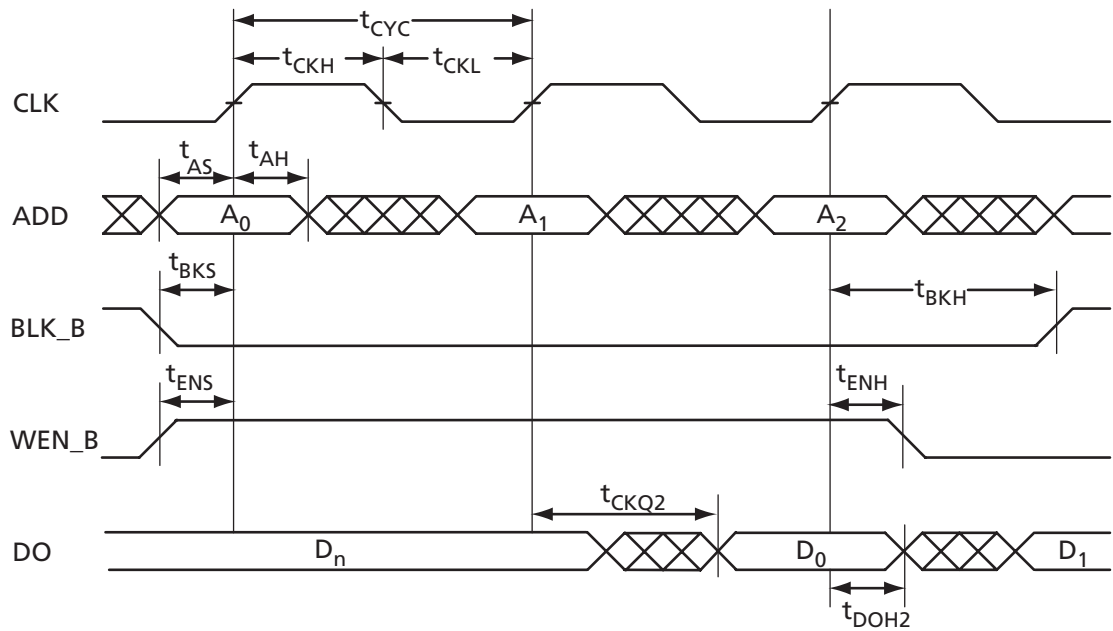
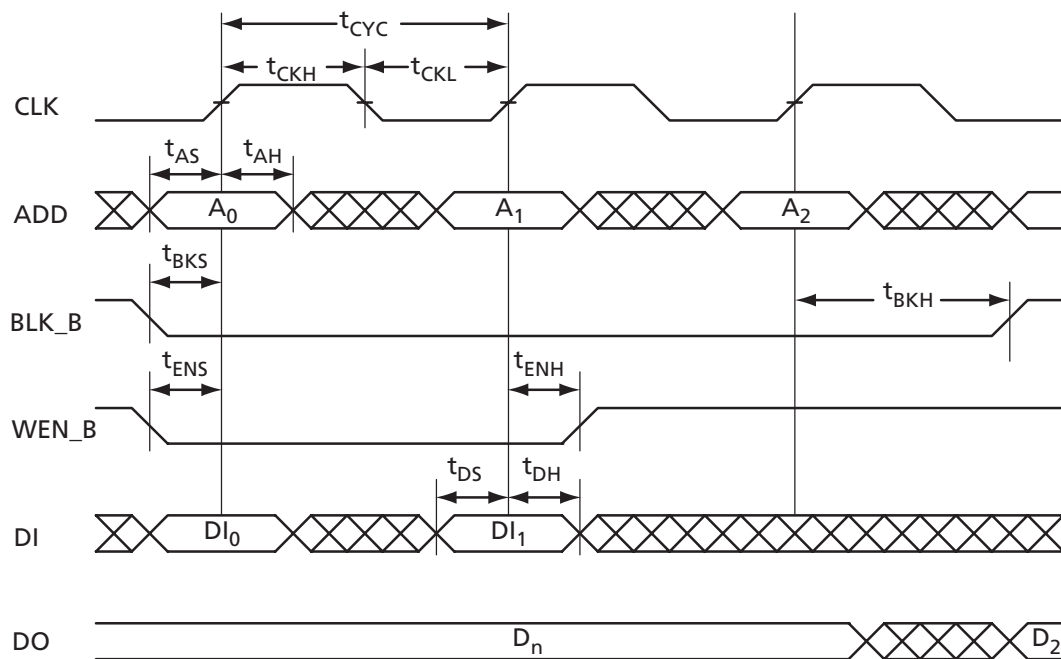
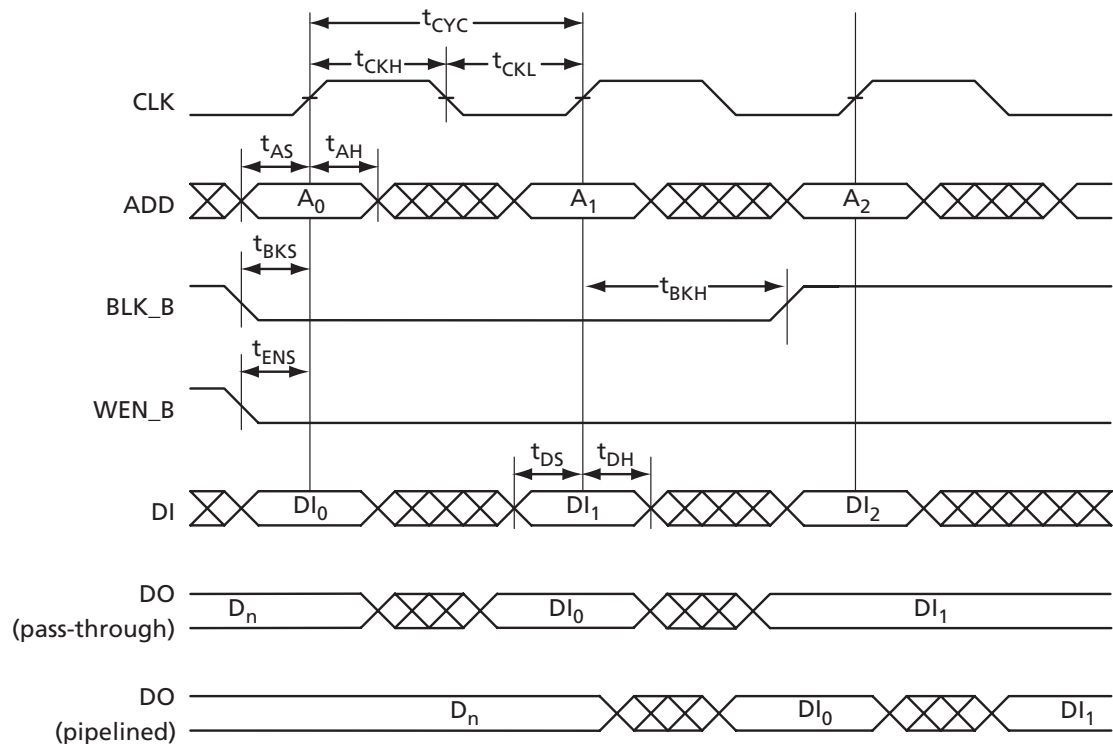


Figure 2-31 • RAM Read for Pipelined Output


Figure 2-32 • RAM Write, Output Retained (WMODE = 0)

Figure 2-33 • RAM Write, Output as Write Data (WMODE = 1)

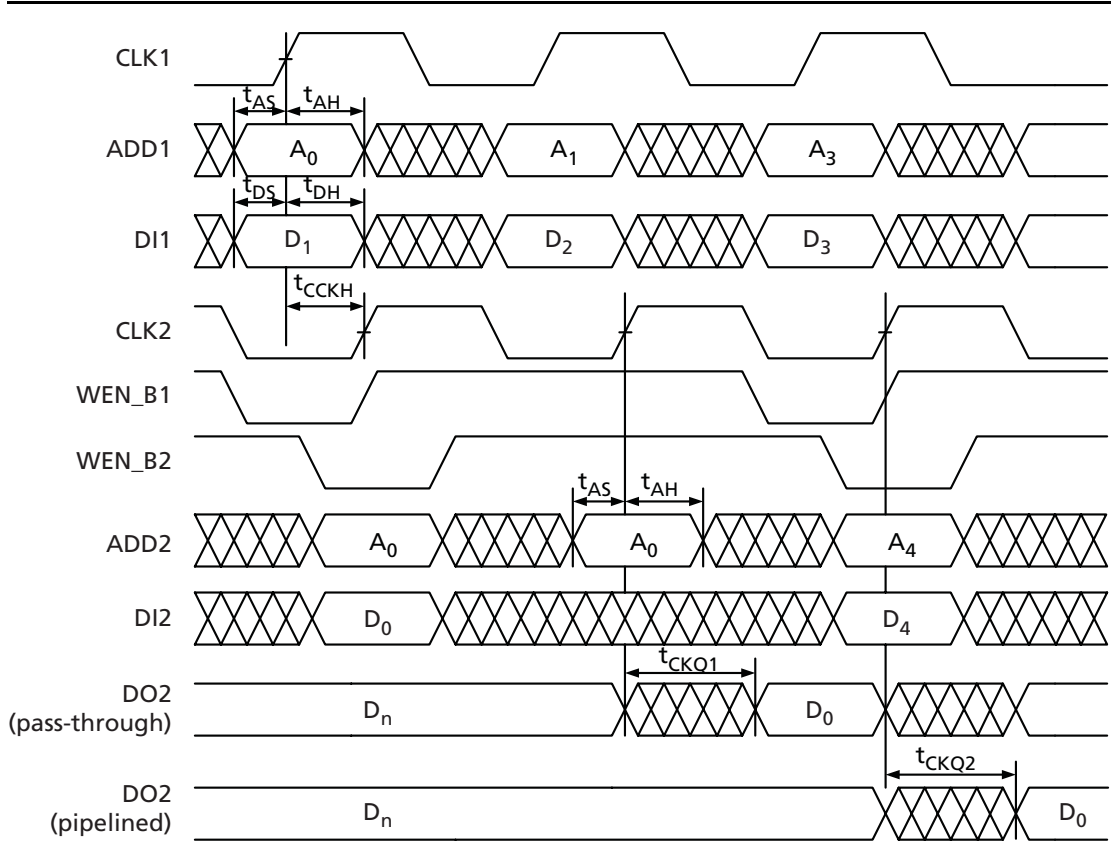


Figure 2-34 • Write Access after Write onto Same Address

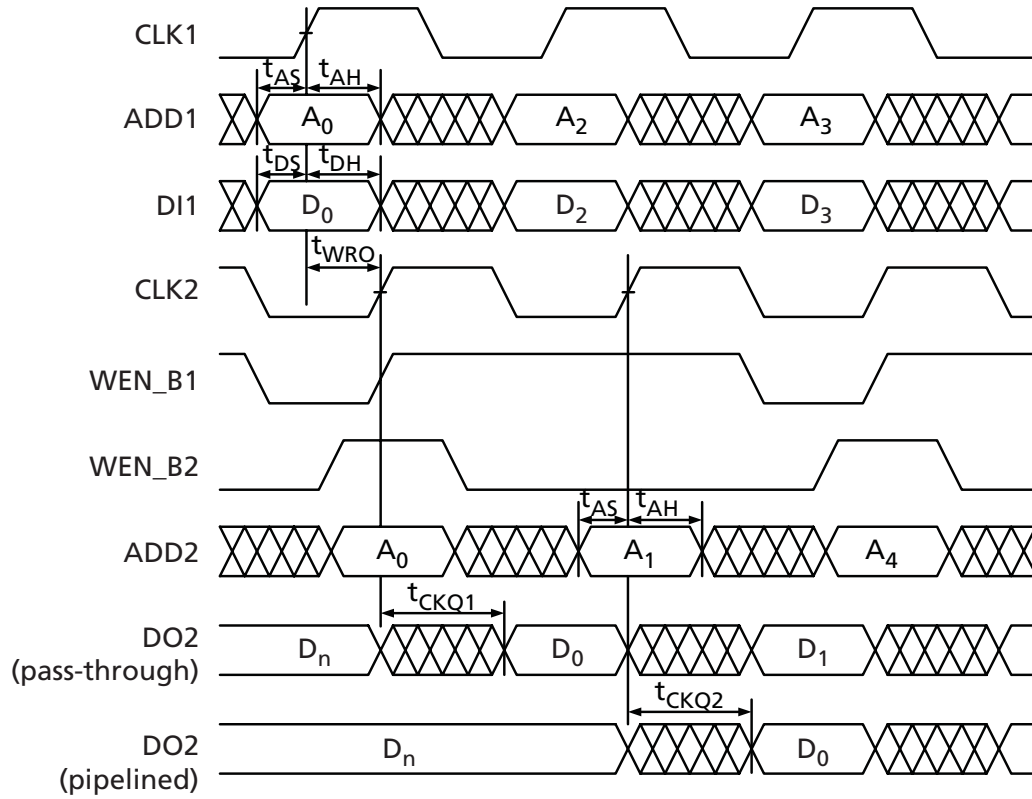


Figure 2-35 • Read Access after Write onto Same Address

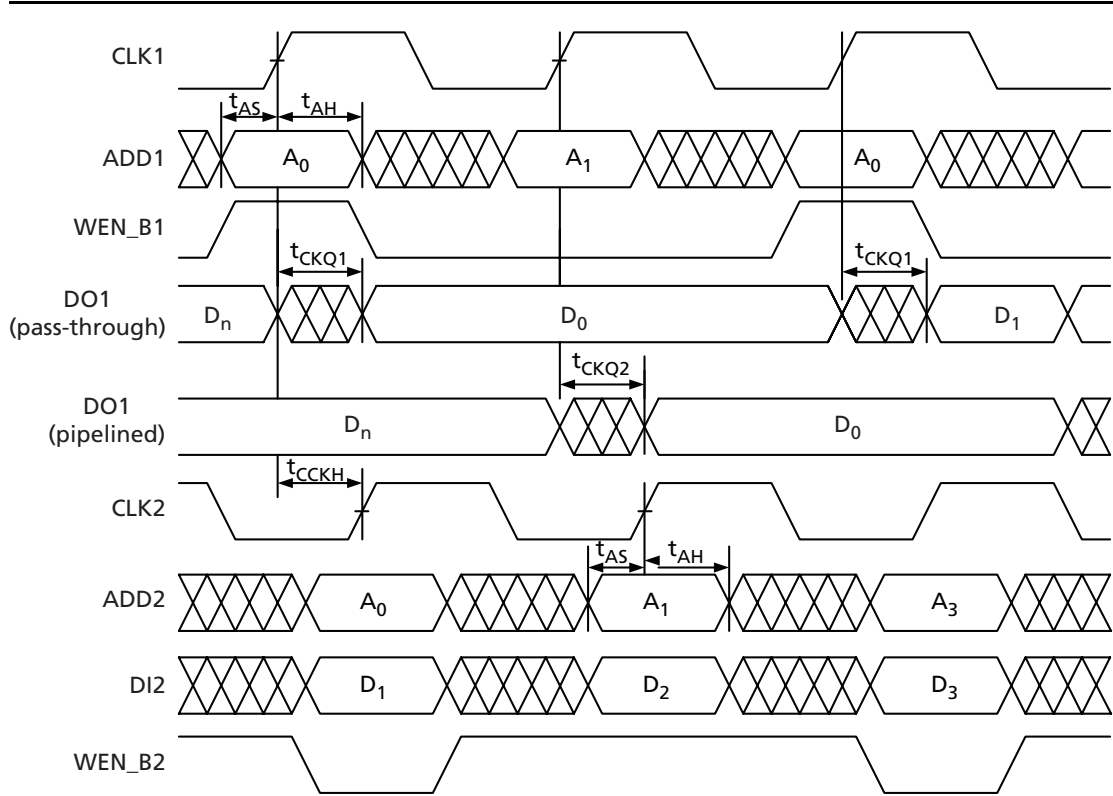


Figure 2-36 • Write Access after Read onto Same Address

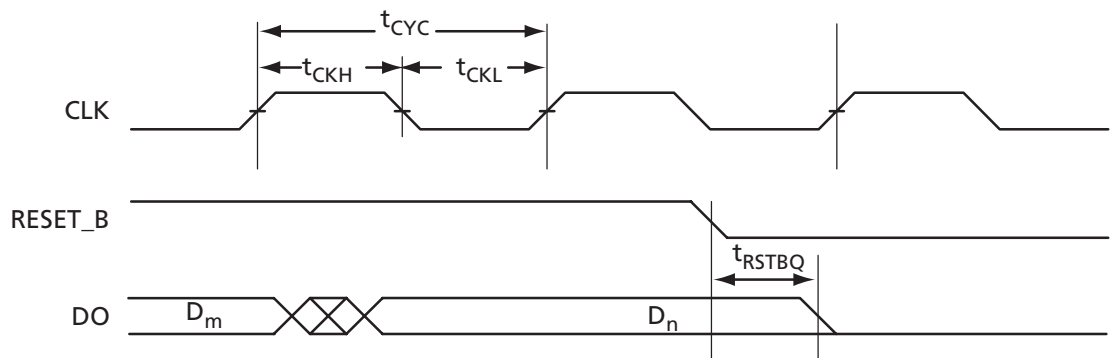


Figure 2-37 • RAM Reset

Timing Characteristics

Table 2-107 • RAM4K9

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | 0.40 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN_B, WEN_B setup time | 0.14 | 0.16 | 0.19 | 0.23 | ns |
| t_{ENH} | REN_B, WEN_B hold time | 0.10 | 0.11 | 0.13 | 0.16 | ns |
| t_{BKS} | BLK_B setup time | 0.23 | 0.27 | 0.31 | 0.37 | ns |
| t_{BKH} | BLK_B hold time | 0.02 | 0.02 | 0.02 | 0.03 | ns |
| t_{DS} | Input data (DI) setup time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input data (DI) hold time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to new data valid on DO (output retained, WMODE = 0) | 2.36 | 2.68 | 3.15 | 3.79 | ns |
| | Clock HIGH to new data valid on DO (flow-through, WMODE = 1) | 1.79 | 2.03 | 2.39 | 2.87 | ns |
| t_{CKQ2} | Clock HIGH to new data valid on DO (pipelined) | 0.89 | 1.02 | 1.20 | 1.44 | ns |
| t_{WRO} | Address collision clk-to-clk delay for reliable read access after write on same address | TBD | TBD | TBD | TBD | ns |
| t_{CCKH} | Address collision clk-to-clk delay for reliable write access after write/read on same address | TBD | TBD | TBD | TBD | ns |
| t_{RSTBQ} | RESET_B LOW to data out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B minimum pulse width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | 193 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-108 • RAM512X18
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | 0.40 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN_B, WEN_B setup time | 0.13 | 0.15 | 0.17 | 0.21 | ns |
| t_{ENH} | REN_B, WEN_B hold time | 0.10 | 0.11 | 0.13 | 0.16 | ns |
| t_{DS} | Input data (DI) setup time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input data (DI) hold time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to new data valid on DO (output retained, WMODE = 0) | 2.16 | 2.46 | 2.89 | 3.47 | ns |
| t_{CKQ2} | Clock HIGH to new data valid on DO (pipelined) | 0.90 | 1.02 | 1.20 | 1.44 | ns |
| t_{WRO} | Address collision clk-to-clk delay for reliable read access after write on same address | TBD | TBD | TBD | TBD | ns |
| t_{CCKH} | Address collision clk-to-clk delay for reliable write access after write/read on same address | TBD | TBD | TBD | TBD | ns |
| t_{RSTBQ} | RESET_B LOW to data out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to data out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B minimum pulse width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | 193 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

FIFO

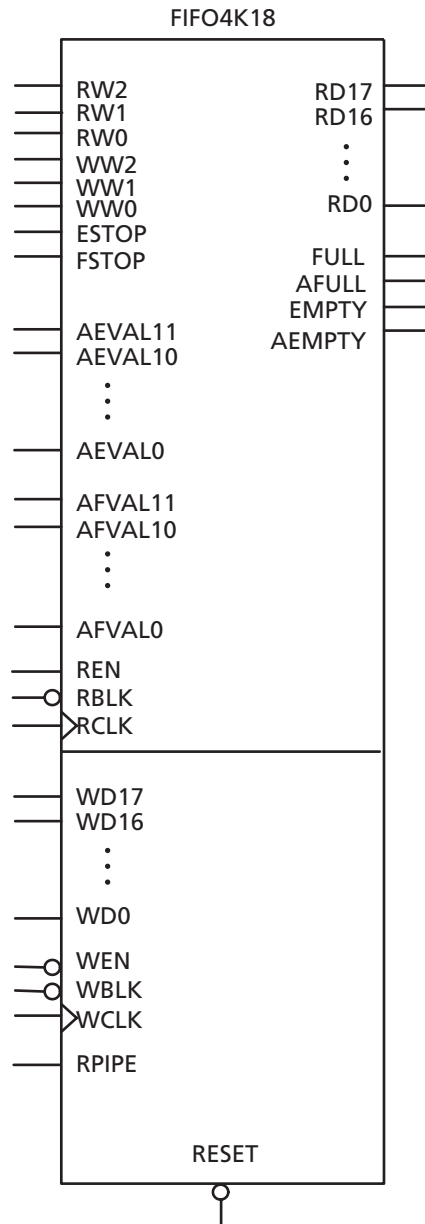


Figure 2-38 • FIFO Model

Timing Waveforms

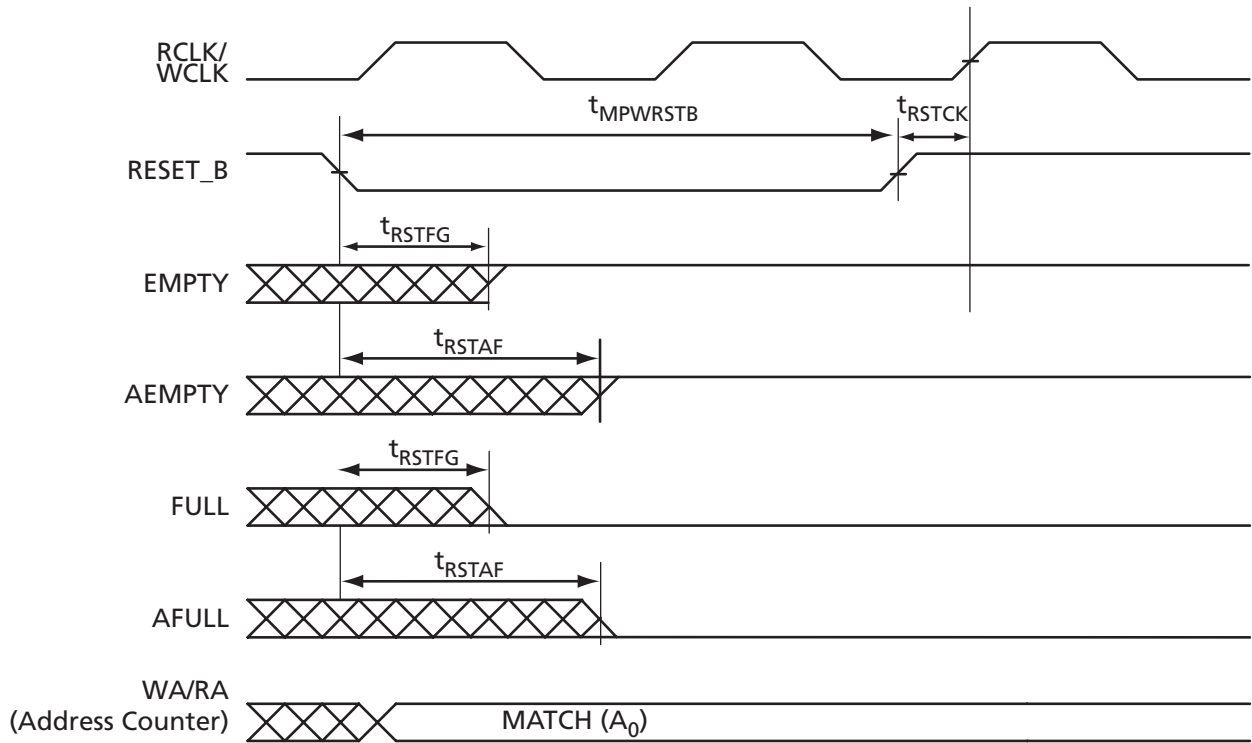


Figure 2-39 • FIFO Reset

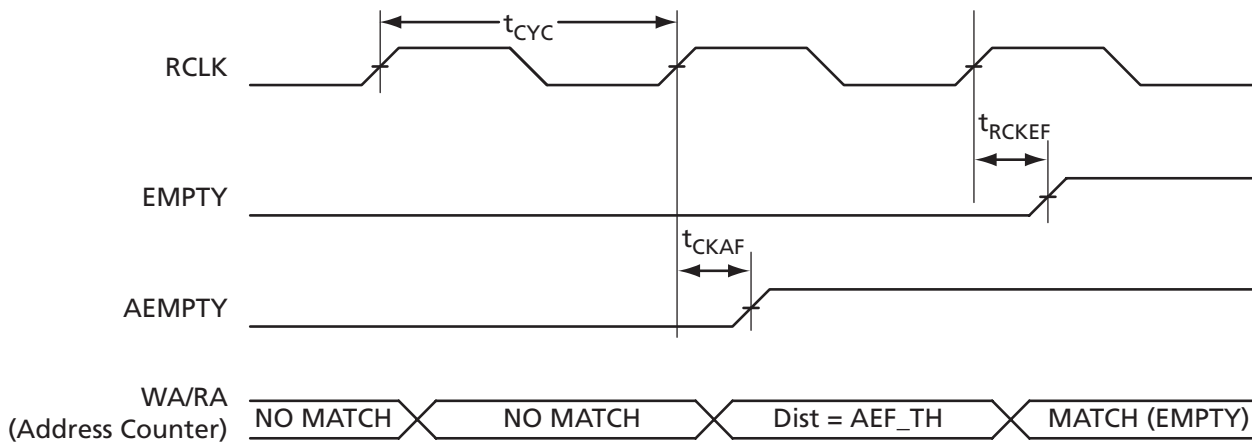
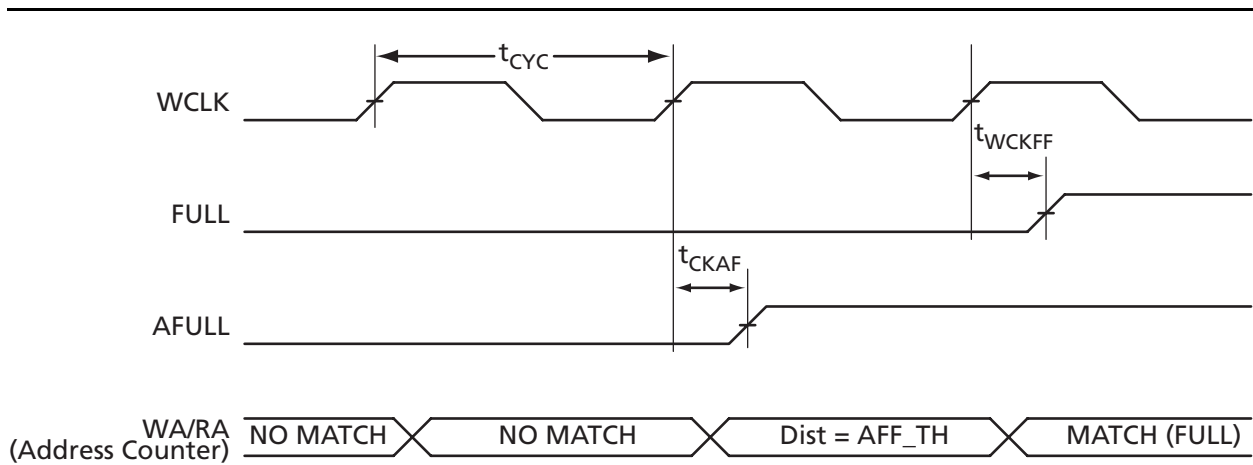
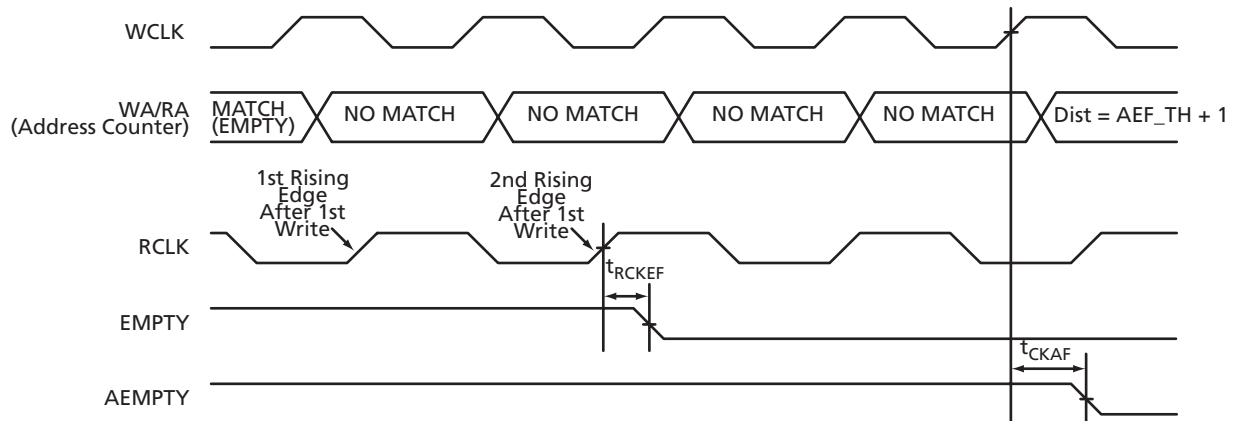
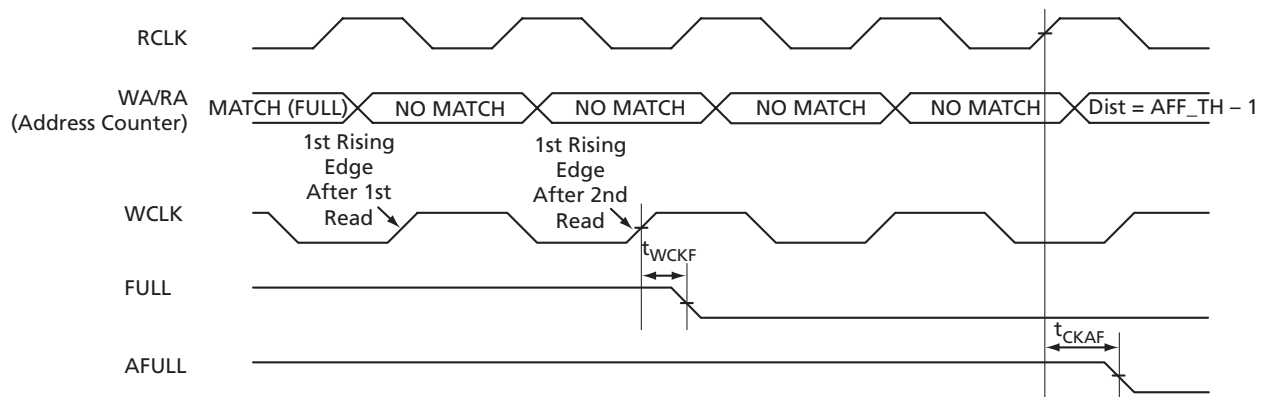


Figure 2-40 • FIFO EMPTY Flag and AEMPTY Flag Assertion


Figure 2-41 • FIFO FULL Flag and AFULL Flag Assertion

Figure 2-42 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

Figure 2-43 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 2-109 • FIFO (for all dies except A3P250)
Worst Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ENS} | REN_B, WEN_B Setup Time | 1.34 | 1.52 | 1.79 | 2.15 | ns |
| t_{ENH} | REN_B, WEN_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK_B Setup Time | 0.19 | 0.22 | 0.26 | 0.31 | ns |
| t_{BKH} | BLK_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (DI) Setup Time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input Data (DI) Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DO (flow-through) | 2.17 | 2.47 | 2.90 | 3.48 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DO (pipelined) | 0.94 | 1.07 | 1.26 | 1.52 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 1.72 | 1.96 | 2.30 | 2.76 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 1.63 | 1.86 | 2.18 | 2.62 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | 9.96 | ns |
| t_{RSTFG} | RESET_B LOW to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | 2.72 | ns |
| t_{RSTAF} | RESET_B LOW to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | 9.85 | ns |
| t_{RSTBQ} | RESET_B LOW to Data Out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | 193 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-110 • FIFO (for A3P250 only, aspect-ratio-dependent)
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ENS} | REN_B, WEN_B Setup Time | 3.26 | 3.71 | 4.36 | 5.24 | ns |
| t_{ENH} | REN_B, WEN_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK_B Setup Time | 0.19 | 0.22 | 0.26 | 0.31 | ns |
| t_{BKH} | BLK_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (DI) Setup Time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input Data (DI) Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DO (flow-through) | 2.17 | 2.47 | 2.90 | 3.48 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DO (pipelined) | 0.94 | 1.07 | 1.26 | 1.52 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 1.72 | 1.96 | 2.30 | 2.76 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 1.63 | 1.86 | 2.18 | 2.62 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | 9.96 | ns |
| t_{RSTFG} | RESET_B LOW to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | 2.72 | ns |
| t_{RSTAF} | RESET_B LOW to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | 9.85 | ns |
| t_{RSTBQ} | RESET_B LOW to Data Out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | 193 | MHz |

Table 2-111 • A3P250 FIFO 512x8
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ENS} | REN_B, WEN_B Setup Time | 3.75 | 4.27 | 5.02 | 6.04 | ns |
| t_{ENH} | REN_B, WEN_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK_B Setup Time | 0.19 | 0.22 | 0.26 | 0.31 | ns |
| t_{BKH} | BLK_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (DI) Setup Time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input Data (DI) Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DO (flow-through) | 2.17 | 2.47 | 2.90 | 3.48 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DO (pipelined) | 0.94 | 1.07 | 1.26 | 1.52 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 1.72 | 1.96 | 2.30 | 2.76 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 1.63 | 1.86 | 2.18 | 2.62 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | 9.96 | ns |
| t_{RSTFG} | RESET_B LOW to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | 2.72 | ns |
| t_{RSTAF} | RESET_B LOW to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | 9.85 | ns |
| t_{RSTBQ} | RESET_B LOW to Data Out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | 193 | MHz |

Table 2-112 • A3P250 FIFO 1kx4
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ENS} | REN_B, WEN_B Setup Time | 4.05 | 4.61 | 5.42 | 6.52 | ns |
| t_{ENH} | REN_B, WEN_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK_B Setup Time | 0.19 | 0.22 | 0.26 | 0.31 | ns |
| t_{BKH} | BLK_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (DI) Setup Time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input Data (DI) Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DO (flow-through) | 2.36 | 2.68 | 3.15 | 3.79 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DO (pipelined) | 0.89 | 1.02 | 1.20 | 1.44 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 1.72 | 1.96 | 2.30 | 2.76 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 1.63 | 1.86 | 2.18 | 2.62 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | 9.96 | ns |
| t_{RSTFG} | RESET_B LOW to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | 2.72 | ns |
| t_{RSTAF} | RESET_B LOW to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | 9.85 | ns |
| t_{RSTBQ} | RESET_B LOW to Data Out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | 193 | MHz |

Table 2-113 • A3P250 FIFO 2kx2
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ENS} | REN_B, WEN_B Setup Time | 4.39 | 5.00 | 5.88 | 7.06 | ns |
| t_{ENH} | REN_B, WEN_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK_B Setup Time | 0.19 | 0.22 | 0.26 | 0.31 | ns |
| t_{BKH} | BLK_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (DI) Setup Time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input Data (DI) Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DO (flow-through) | 2.36 | 2.68 | 3.15 | 3.79 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DO (pipelined) | 0.89 | 1.02 | 1.20 | 1.44 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 1.72 | 1.96 | 2.30 | 2.76 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 1.63 | 1.86 | 2.18 | 2.62 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | 9.96 | ns |
| t_{RSTFG} | RESET_B LOW to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | 2.72 | ns |
| t_{RSTAF} | RESET_B LOW to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | 9.85 | ns |
| t_{RSTBQ} | RESET_B LOW to Data Out LOW on DO (flow-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | 193 | MHz |

Table 2-114 • A3P250 FIFO 4kx1

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | -F | Units |
|---------------|---|------|------|------|------|-------|
| t_{ENS} | REN_B, WEN_B Setup Time | 4.86 | 5.53 | 6.50 | 7.81 | ns |
| t_{ENH} | REN_B, WEN_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK_B Setup Time | 0.19 | 0.22 | 0.26 | 0.31 | ns |
| t_{BKH} | BLK_B Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (DI) Setup Time | 0.18 | 0.21 | 0.25 | 0.29 | ns |
| t_{DH} | Input Data (DI) Hold Time | 0.00 | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DO (flow-through) | 2.36 | 2.68 | 3.15 | 3.79 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DO (pipelined) | 0.89 | 1.02 | 1.20 | 1.44 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 1.72 | 1.96 | 2.30 | 2.76 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 1.63 | 1.86 | 2.18 | 2.62 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | 9.96 | ns |
| t_{RSTFG} | RESET_B LOW to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | 2.72 | ns |
| t_{RSTAF} | RESET_B LOW to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | 9.85 | ns |
| t_{RSTBQ} | RESET_B LOW to Data Out LOW on DO (pass-through) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| | RESET_B LOW to Data Out LOW on DO (pipelined) | 0.92 | 1.05 | 1.23 | 1.48 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.29 | 0.33 | 0.38 | 0.46 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 1.50 | 1.71 | 2.01 | 2.41 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.21 | 0.24 | 0.29 | 0.34 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | 5.19 | ns |
| F_{MAX} | Maximum Frequency | 310 | 272 | 231 | 193 | MHz |

Embedded FlashROM Characteristics

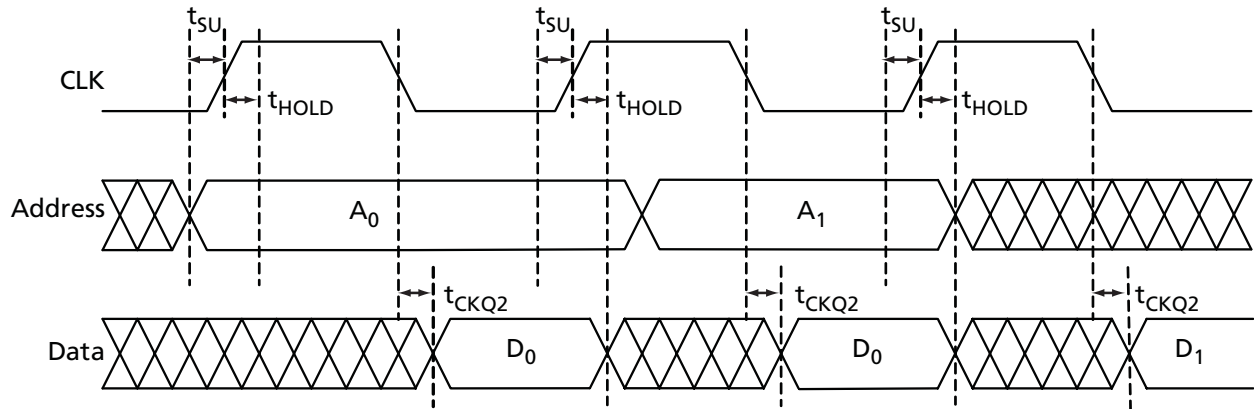


Figure 2-44 • Timing Diagram

Timing Characteristics

Table 2-115 • Embedded FlashROM Access Time

| Parameter | Description | -2 | -1 | Std. | Units |
|------------|-------------------------|-------|-------|-------|-------|
| t_{SU} | Address Setup Time | 0.53 | 0.61 | 0.71 | ns |
| t_{HOLD} | Address Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ2} | Clock to Out | 21.42 | 24.40 | 28.68 | ns |
| F_{MAX} | Maximum Clock Frequency | 15 | 15 | 15 | MHz |

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

Table 2-116 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|-----------------------------|-------|-------|-------|-------|
| t_{DISU} | Test Data Input Setup Time | 0.50 | 0.57 | 0.67 | ns |
| t_{DIHD} | Test Data Input Hold Time | 1.00 | 1.13 | 1.33 | ns |
| t_{TMSSU} | Test Mode Select Setup Time | 0.50 | 0.57 | 0.67 | ns |
| t_{TMDHD} | Test Mode Select Hold Time | 1.00 | 1.13 | 1.33 | ns |
| t_{TCK2Q} | Clock to Q (data out) | 6.00 | 6.80 | 8.00 | ns |
| t_{RSTB2Q} | Reset to Q (data out) | 20.00 | 22.67 | 26.67 | ns |
| F_{TCKMAX} | TCK Maximum Frequency | 25.00 | 22.00 | 19.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.20 | 0.23 | 0.27 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | TBD | TBD | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Part Number and Revision Date

Part Number 51700097-002-3
Revised August 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

| Previous Version | Changes in Current Version (v1.3) | Page |
|------------------------|---|---------------|
| v1.2 (June 2008) | T _J , Maximum Junction Temperature, was changed to 100° from 110° in the "Thermal Characteristics" section and EQ 2-2. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W. | 2-5 |
| | Values for the A3P015 device were added to Table 2-7 · Quiescent Supply Current Characteristics. | 2-6 |
| | Values for the A3P015 device were added to Table 2-14 · Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. P _{AC14} was removed. Table 2-15 · Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new. | 2-10, 2-11 |
| | The "PLL Contribution—PPLL" section was updated to change the P _{PLL} formula from P _{AC13} + P _{AC14} * F _{CLKOUT} to P _{DC4} + P _{AC13} * F _{CLKOUT} . | 2-13 |
| | Both fall and rise values were included for t _{DDRISUD} and t _{DDRIHD} in Table 2-93 · Input DDR Propagation Delays. | 2-71 |
| | Table 2-98 · A3P015 Global Resource is new. | 2-79 |
| | The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-106 · ProASIC3 CCC/PLL Specification. | 2-83 |
| v1.1 (January 2008) | Table note references were added to Table 2-2 · Recommended Operating Conditions ¹ , and the order of the table notes was changed. | 2-2 |
| | The title for Table 2-4 · Overshoot and Undershoot Limits ¹ was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os." | 2-3 |
| | The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power. | 2-6 |
| | Table 2-29 · I/O Output Buffer Maximum Resistances ¹ was revised to include values for 3.3 V PCI/PCI-X. | 2-24 |
| | Table 2-81 · LVDS Minimum and Maximum DC Input and Output Levels was updated. | 2-59 |
| v1.0 (January 2008) | In Table 2-2 · Recommended Operating Conditions ¹ , T _J was listed in the symbol column and was incorrect. It was corrected and changed to T _A . | 2-2 |
| | In Table 2-3 · Flash Programming Limits – Retention, Storage and Operating Temperature ¹ , Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2-2 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-3 |
| | In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency. | 2-13 |
| | In Table 2-21 · Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said T _J and it was corrected and changed to T _A . | 2-20 |

| Previous Version | Changes in Current Version (v1.3) | Page |
|---|--|-------|
| v1.0 (continued) | In Table 2-106 · ProASIC3 CCC/PLL Specification , the SCLK parameter and note 1 are new. | 2-83 |
| | Table 2-116 · JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-103 |
| v2.2 (July 2007) | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel restarted the version numbers so the new version number is v1.0. | N/A |
| v2.1 (May 2007) | The T_J parameter in Table 3-2 · Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added. | 3-2 |
| v2.0 (April 2007) | Table 3-5 · Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new. | 3-5 |
| Advance v0.7 (January 2007) | The timing characteristics tables were updated. | N/A |
| | The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up. | 2-15 |
| | The "PLL Macro" section was updated to include power-up information. | 2-15 |
| | Table 2-11 · ProASIC3 CCC/PLL Specification was updated. | 2-29 |
| | Figure 2-19 · Peak-to-Peak Jitter Definition is new. | 2-18 |
| | The "SRAM and FIFO" section was updated with operation and timing requirement information. | 2-21 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled. | 2-28 |
| | PCI-X 3.3 V was added to Table 2-11 · VCCI Voltages and Compatible Standards . | 2-29 |
| | In the Table 2-15 · Levels of Hot-Swap Support , the ProASIC3 compliance descriptions were updated for levels 3 and 4. | 2-34 |
| | Table 2-43 · I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated. | 2-64 |
| | Notes 3, 4, and 5 were added to Table 2-17 · Comparison Table for 5 V–Compliant Receiver Scheme . 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7. | 2-40 |
| | The "VCCPLF PLL Supply Voltage" section was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" section was updated. | 2-50 |
| | The "GL Globals" section was updated to include information about direct input into quadrant clocks. | 2-51 |
| | V_{JTAG} was deleted from the "TCK Test Clock" section. | 2-51 |
| | In Table 2-22 · Recommended Tie-Off Values for the TCK and TRST Pins , TSK was changed to TCK in note 2. Note 3 was also updated. | 2-51 |
| Ambient was deleted from Table 3-2 · Recommended Operating Conditions . VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45". | 3-2 | |
| Note 3 is new in Table 3-4 · Overshoot and Undershoot Limits (as measured on quiet I/Os) ¹ . | 3-2 | |

| Previous Version | Changes in Current Version (v1.3) | Page |
|--|---|--------------|
| Advance v0.7 (continued) | In EQ 3-2, 150 was changed to 110 and the result changed from 3.9 to 1.951. | 3-5 |
| | Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated. | 3-6 |
| | Table 3-5 • Package Thermal Resistivities was updated. | 3-5 |
| | Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings (Advanced) and Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions (Standard Plus) were updated. | 3-17 to 3-17 |
| | Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated. | 3-20 to 3-20 |
| | Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated. | 3-9 |
| | Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated. | 3-22 to 3-22 |
| | Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated. | 3-18 |
| | Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated. | 3-24 to 3-26 |
| | The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated. | 3-27 |
| | Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new. | 3-82 to 3-84 |
| Figure 3-43 • Timing Diagram was updated. | 3-96 | |
| Advance v0.5 (January 2006) | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-7 • Efficient Long-Line Resources was updated. | 2-7 |
| | The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated. | 2-16 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| The "Introduction" of the "Advanced I/Os" section was updated. | 2-28 | |



| Previous Version | Changes in Current Version (v1.3) | Page |
|--|--|------|
| Advance v0.5 (continued) | The "I/O Banks" section is new. This section explains the following types of I/Os: Advanced Standard+ Standard Table 2-12 • Automotive ProASIC3 Bank Types Definition and Differences is new. This table describes the standards listed above. | 2-29 |
| | PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards | 2-29 |
| | Table 2-13 • ProASIC3 I/O Features was updated. | 2-30 |
| | The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature. | 2-32 |
| | The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information. | 2-35 |
| | Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices. | 2-64 |
| | The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices were updated. | 2-64 |
| | The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new. | 2-41 |
| | A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC3 Devices (maximum drive strength and high slew selected). | 2-30 |
| | Table 2-18 • Automotive ProASIC3 I/O Attributes vs. I/O Standard Applications | 2-45 |
| | Table 2-50 • ProASIC3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device) | 2-83 |
| | Table 2-51 • ProASIC3 Output Drive for Standard+ I/O Bank Type was updated. | 2-84 |
| | Table 2-54 • ProASIC3 Output Drive for Advanced I/O Bank Type was updated. | 2-84 |
| | The "x" was updated in the "User I/O Naming Convention" section. | 2-48 |
| | The "V _{CC} Core Supply Voltage" pin description was updated. | 2-50 |
| | The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected. | 2-50 |
| | The "V _{JTAG} JTAG Supply Voltage" pin description was updated. | 2-50 |
| | The "V _{PUMP} Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground. | 2-50 |
| | The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused. | 2-50 |
| | The "JTAG Pins" section was updated to include information on what happens when the pin is unused. | 2-51 |
| The "Programming" section was updated to include information concerning serialization. | 2-53 | |
| The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information. | 2-54 | |
| "DC and Switching Characteristics" chapter was updated with new information. | 3-1 | |

| Previous Version | Changes in Current Version (v1.3) | Page |
|---|---|--------|
| Advance v0.3 | M7 device information is new. | N/A |
| | Table 2-4 • ProASIC3 Globals/Spines/Rows by Device was updated to include the number or rows in each top or bottom spine. | 2-16 |
| | EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "PLL Macro" section was updated. EXTFB information was removed from this section. | 2-15 |
| | The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-11 • ProASIC3 CCC/PLL Specification | 2-29 |
| | EXTFB was removed from Figure 2-27 • CCC/PLL Macro. | 2-28 |
| | Table 2-13 • ProASIC3 I/O Features was updated. | 2-30 |
| | The "Hot-Swap Support" section was updated. | 2-33 |
| | The "Cold-Sparing Support" section was updated. | 2-34 |
| | "Electrostatic Discharge (ESD) Protection" section was updated. | 2-35 |
| | The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated. | 2-64 |
| | In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and V_{CC1B2} was changed to V_{CC1B1} . | 2-97 |
| | The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section. | 2-50 |
| | The "JTAG Pins" section was updated. | 2-51 |
| | "128-Bit AES Decryption" section was updated to include M7 device information. | 2-53 |
| | Table 3-6 was updated. | 3-6 |
| | Table 3-7 was updated. | 3-6 |
| | In Table 3-11, PAC4 was updated. | 3-93-8 |
| | Table 3-20 was updated. | 3-20 |
| | The note in Table 3-32 was updated. | 3-27 |
| All Timing Characteristics tables were updated from LVTTTL to Register Delays | 3-31 to 3-73 | |
| The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated. | 3-85 to 3-90 | |
| F_{TCKMAX} was updated in Table 3-110. | 3-97 | |
| Advance v0.2 | Figure 2-11 was updated. | 2-9 |
| | The "Clock Resources (VersaNets)" section was updated. | 2-9 |
| | The "VersaNet Global Networks and Spine Access" section was updated. | 2-9 |
| | The "PLL Macro" section was updated. | 2-15 |
| | Figure 2-27 was updated. | 2-28 |
| | Figure 2-20 was updated. | 2-19 |
| | Table 2-5 was updated. | 2-25 |
| | Table 2-6 was updated. | 2-25 |

| Previous Version | Changes in Current Version (v1.3) | Page |
|-----------------------------|---|---------------|
| Advance v0.2 (continued) | The "FIFO Flag Usage Considerations" section was updated. | 2-27 |
| | Table 2-13 was updated. | 2-30 |
| | Figure 2-24 was updated. | 2-31 |
| | The "Cold-Sparing Support" section is new. | 2-34 |
| | Table 2-43 was updated. | 2-64 |
| | Table 2-18 was updated. | 2-45 |
| | Pin descriptions in the "JTAG Pins" section were updated. | 2-51 |
| | The "User I/O Naming Convention" section was updated. | 2-48 |
| | Table 3-7 was updated. | 3-6 |
| | The "Methodology" section was updated. | 3-10 |
| | Table 3-40 and Table 3-39 were updated. | 3-33, 3-32 |

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

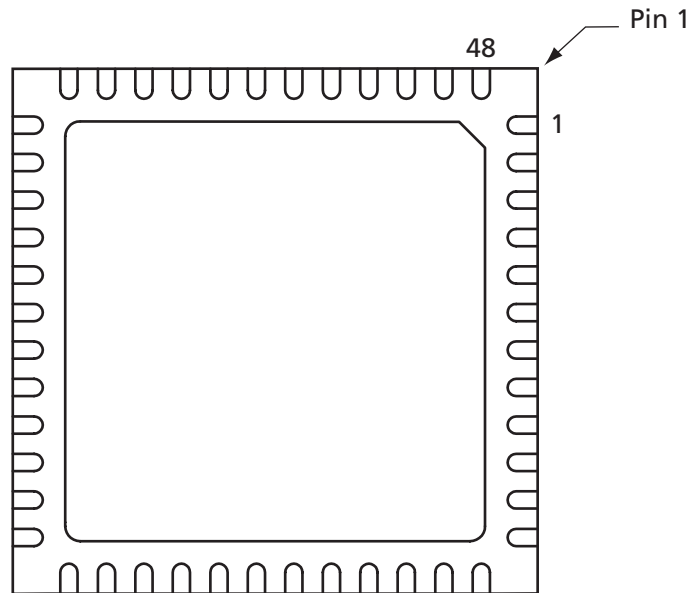
The Actel products described in this advance status datasheet may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.





3 – Package Pin Assignments

48-Pin QFN



Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

Figure 3-1 •

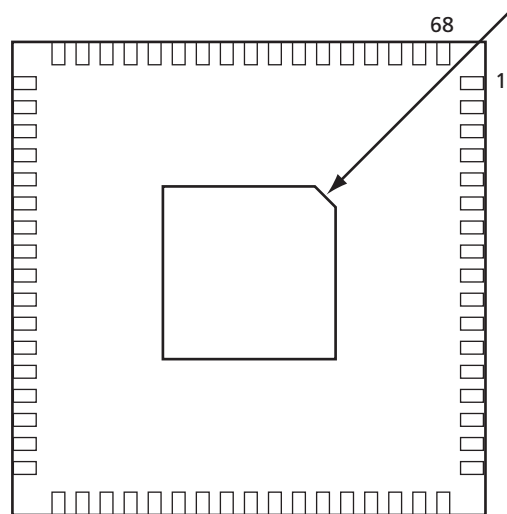
Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 48-Pin QFP | |
|------------|--------------------|
| Pin Number | A3P030 Function |
| 1 | IO82RSB1 |
| 2 | GEC0/IO73RSB1 |
| 3 | GEA0/IO72RSB1 |
| 4 | GEB0/IO71RSB1 |
| 5 | GND |
| 6 | V _{CC} B1 |
| 7 | IO68RSB1 |
| 8 | IO67RSB1 |
| 9 | IO66RSB1 |
| 10 | IO65RSB1 |
| 11 | IO64RSB1 |
| 12 | IO62RSB1 |
| 13 | IO61RSB1 |
| 14 | IO60RSB1 |
| 15 | IO57RSB1 |
| 16 | IO55RSB1 |
| 17 | IO53RSB1 |
| 18 | V _{CC} |
| 19 | V _{CC} B1 |
| 20 | IO46RSB1 |
| 21 | IO42RSB1 |
| 22 | TCK |
| 23 | TDI |
| 24 | TMS |
| 25 | V _{PUMP} |
| 26 | TDO |
| 27 | TRST |
| 28 | V _{JTAG} |
| 29 | IO38RSB0 |
| 30 | GDB0/IO34RSB0 |
| 31 | GDA0/IO33RSB0 |
| 32 | GDC0/IO32RSB0 |
| 33 | V _{CC} B0 |
| 34 | GND |
| 35 | V _{CC} |
| 36 | IO25RSB0 |

| 48-Pin QFP | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| 37 | IO24RSB0 |
| 38 | IO22RSB0 |
| 39 | IO20RSB0 |
| 40 | IO18RSB0 |
| 41 | IO16RSB0 |
| 42 | IO14RSB0 |
| 43 | IO10RSB0 |
| 44 | IO08RSB0 |
| 45 | IO06RSB0 |
| 46 | IO04RSB0 |
| 47 | IO02RSB0 |
| 48 | IO00RSB0 |

68-Pin QFN



Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

Figure 3-2 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 68-Pin QFN | |
|------------|--------------------|
| Pin Number | A3P015 Function |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | V _{CC} |
| 9 | GND |
| 10 | V _{CC} B1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | V _{CC} |
| 25 | GND |
| 26 | V _{CC} B1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | V _{PUMP} |
| 36 | TDO |

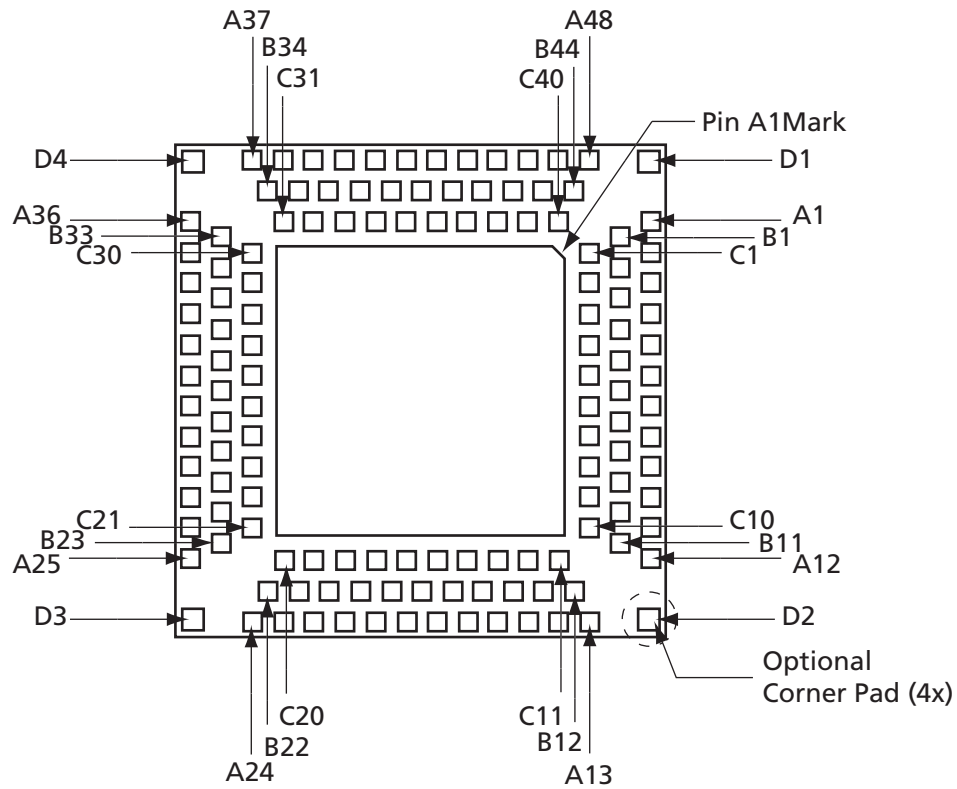
| 68-Pin QFN | |
|------------|--------------------|
| Pin Number | A3P015 Function |
| 37 | TRST |
| 38 | V _{JTAG} |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | V _{CC} B0 |
| 45 | GND |
| 46 | V _{CC} |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | V _{CC} B0 |
| 60 | GND |
| 61 | V _{CC} |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |



| 68-Pin QFN | |
|------------|----------------------|
| Pin Number | A3P030 Function |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | V _{CC} |
| 9 | GND |
| 10 | V _{CC} B1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | V _{CC} |
| 25 | GND |
| 26 | V _{CC} I B1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | V _{PUMP} |
| 36 | TDO |

| 68-Pin QFN | |
|------------|----------------------|
| Pin Number | A3P030 Function |
| 37 | TRST |
| 38 | V _{JTAG} |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | V _{CC} I B0 |
| 45 | GND |
| 46 | V _{CC} |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | V _{CC} I B0 |
| 60 | GND |
| 61 | V _{CC} |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |

132-Pin QFN



Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

Figure 3-3 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 132-Pin QFN | | 132-Pin QFN | | 132-Pin QFN | |
|-------------|-----------------|-------------|-----------------|-------------|--------------------|
| Pin Number | A3P030 Function | Pin Number | A3P030 Function | Pin Number | A3P030 Function |
| A1 | IO1RSB1 | A37 | IO26RSB0 | B25 | GND |
| A2 | IO81RSB1 | A38 | IO23RSB0 | B26 | NC |
| A3 | NC | A39 | NC | B27 | IO41RSB0 |
| A4 | IO80RSB1 | A40 | IO22RSB0 | B28 | GND |
| A5 | GEC0/IO77RSB1 | A41 | IO20RSB0 | B29 | GDA0/IO37RSB0 |
| A6 | NC | A42 | IO18RSB0 | B30 | NC |
| A7 | GEB0/IO75RSB1 | A43 | V _{CC} | B31 | GND |
| A8 | IO73RSB1 | A44 | IO15RSB0 | B32 | IO33RSB0 |
| A9 | NC | A45 | IO12RSB0 | B33 | IO30RSB0 |
| A10 | V _{CC} | A46 | IO10RSB0 | B34 | IO27RSB0 |
| A11 | IO71RSB1 | A47 | IO09RSB0 | B35 | IO24RSB0 |
| A12 | IO68RSB1 | A48 | IO06RSB0 | B36 | GND |
| A13 | IO63RSB1 | B1 | IO02RSB1 | B37 | IO21RSB0 |
| A14 | IO60RSB1 | B2 | IO82RSB1 | B38 | IO19RSB0 |
| A15 | NC | B3 | GND | B39 | GND |
| A16 | IO59RSB1 | B4 | IO79RSB1 | B40 | IO16RSB0 |
| A17 | IO57RSB1 | B5 | NC | B41 | IO13RSB0 |
| A18 | V _{CC} | B6 | GND | B42 | GND |
| A19 | IO54RSB1 | B7 | IO74RSB1 | B43 | IO08RSB0 |
| A20 | IO52RSB1 | B8 | NC | B44 | IO05RSB0 |
| A21 | IO49RSB1 | B9 | GND | C1 | IO03RSB1 |
| A22 | IO48RSB1 | B10 | IO70RSB1 | C2 | IO00RSB1 |
| A23 | IO47RSB1 | B11 | IO67RSB1 | C3 | NC |
| A24 | TDI | B12 | IO64RSB1 | C4 | IO78RSB1 |
| A25 | TRST | B13 | IO61RSB1 | C5 | GEA0/IO76RSB1 |
| A26 | IO44RSB0 | B14 | GND | C6 | NC |
| A27 | NC | B15 | IO58RSB1 | C7 | NC |
| A28 | IO43RSB0 | B16 | IO56RSB1 | C8 | V _{CC} B1 |
| A29 | IO42RSB0 | B17 | GND | C9 | IO69RSB1 |
| A30 | IO40RSB0 | B18 | IO53RSB1 | C10 | IO66RSB1 |
| A31 | IO39RSB0 | B19 | IO50RSB1 | C11 | IO65RSB1 |
| A32 | GDC0/IO36RSB0 | B20 | GND | C12 | IO62RSB1 |
| A33 | NC | B21 | IO46RSB1 | C13 | NC |
| A34 | V _{CC} | B22 | TMS | C14 | NC |
| A35 | IO34RSB0 | B23 | TDO | C15 | IO55RSB1 |
| A36 | IO31RSB0 | B24 | IO45RSB0 | C16 | V _{CC} B1 |

| 132-Pin QFN | |
|-------------|--------------------|
| Pin Number | A3P030 Function |
| C17 | IO51RSB1 |
| C18 | NC |
| C19 | TCK |
| C20 | NC |
| C21 | V _{PUMP} |
| C22 | V _{JTAG} |
| C23 | NC |
| C24 | NC |
| C25 | NC |
| C26 | GDB0/IO38RSB0 |
| C27 | NC |
| C28 | V _{CCIB0} |
| C29 | IO32RSB0 |
| C30 | IO29RSB0 |
| C31 | IO28RSB0 |
| C32 | IO25RSB0 |
| C33 | NC |
| C34 | NC |
| C35 | V _{CCIB0} |
| C36 | IO17RSB0 |
| C37 | IO14RSB0 |
| C38 | IO11RSB0 |
| C39 | IO07RSB0 |
| C40 | IO04RSB0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |



| 132-Pin QFN | |
|-------------|---------------------|
| Pin Number | A3P060 Function |
| A1 | GAB2/IO00RSB1 |
| A2 | IO93RSB1 |
| A3 | V _{CC} B1 |
| A4 | GFC1/IO89RSB1 |
| A5 | GFB0/IO86RSB1 |
| A6 | V _{CC} PLF |
| A7 | GFA1/IO84RSB1 |
| A8 | GFC2/IO81RSB1 |
| A9 | IO78RSB1 |
| A10 | V _{CC} |
| A11 | GEB1/IO75RSB1 |
| A12 | GEA0/IO72RSB1 |
| A13 | GEC2/IO69RSB1 |
| A14 | IO65RSB1 |
| A15 | V _{CC} |
| A16 | IO64RSB1 |
| A17 | IO63RSB1 |
| A18 | IO62RSB1 |
| A19 | IO61RSB1 |
| A20 | IO58RSB1 |
| A21 | GDB2/IO55RSB1 |
| A22 | NC |
| A23 | GDA2/IO54RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO48RSB0 |
| A27 | V _{CC} |
| A28 | IO47RSB0 |
| A29 | GCC2/IO46RSB0 |
| A30 | GCA2/IO44RSB0 |
| A31 | GCA0/IO43RSB0 |
| A32 | GCB1/IO40RSB0 |
| A33 | IO36RSB0 |
| A34 | V _{CC} |
| A35 | IO31RSB0 |
| A36 | GBA2/IO28RSB0 |

| 132-Pin QFN | |
|-------------|---------------------|
| Pin Number | A3P060 Function |
| A37 | GBB1/IO25RSB0 |
| A38 | GBC0/IO22RSB0 |
| A39 | V _{CC} B0 |
| A40 | IO21RSB0 |
| A41 | IO18RSB0 |
| A42 | IO15RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | GAB1/IO08RSB0 |
| A46 | NC |
| A47 | GAB0/IO07RSB0 |
| A48 | IO04RSB0 |
| B1 | IO01RSB1 |
| B2 | GAC2/IO94RSB1 |
| B3 | GND |
| B4 | GFC0/IO88RSB1 |
| B5 | V _{COMPLF} |
| B6 | GND |
| B7 | GFB2/IO82RSB1 |
| B8 | IO79RSB1 |
| B9 | GND |
| B10 | GEB0/IO74RSB1 |
| B11 | VMV1 |
| B12 | GEB2/IO70RSB1 |
| B13 | IO67RSB1 |
| B14 | GND |
| B15 | NC |
| B16 | NC |
| B17 | GND |
| B18 | IO59RSB1 |
| B19 | GDC2/IO56RSB1 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO49RSB0 |

| 132-Pin QFN | |
|-------------|--------------------|
| Pin Number | A3P060 Function |
| B25 | GND |
| B26 | NC |
| B27 | GCB2/IO45RSB0 |
| B28 | GND |
| B29 | GCB0/IO41RSB0 |
| B30 | GCC1/IO38RSB0 |
| B31 | GND |
| B32 | GBB2/IO30RSB0 |
| B33 | VMV0 |
| B34 | GBA0/IO26RSB0 |
| B35 | GBC1/IO23RSB0 |
| B36 | GND |
| B37 | IO20RSB0 |
| B38 | IO17RSB0 |
| B39 | GND |
| B40 | IO12RSB0 |
| B41 | GAC0/IO09RSB0 |
| B42 | GND |
| B43 | GAA1/IO06RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO02RSB1 |
| C2 | IO95RSB1 |
| C3 | V _{CC} |
| C4 | GFB1/IO87RSB1 |
| C5 | GFA0/IO85RSB1 |
| C6 | GFA2/IO83RSB1 |
| C7 | IO80RSB1 |
| C8 | V _{CC} B1 |
| C9 | GEA1/IO73RSB1 |
| C10 | GNDQ |
| C11 | GEA2/IO71RSB1 |
| C12 | IO68RSB1 |
| C13 | V _{CC} B1 |
| C14 | NC |
| C15 | NC |
| C16 | IO60RSB1 |

| 132-Pin QFN | |
|-------------|---------------------|
| Pin Number | A3P060 Function |
| C17 | IO57RSB1 |
| C18 | NC |
| C19 | TCK |
| C20 | VMV1 |
| C21 | V _{PUMP} |
| C22 | V _{JTAG} |
| C23 | V _{CC1} B0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO42RSB0 |
| C27 | GCC0/IO39RSB0 |
| C28 | V _{CC1} B0 |
| C29 | IO29RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO27RSB0 |
| C32 | GBB0/IO24RSB0 |
| C33 | V _{CC} |
| C34 | IO19RSB0 |
| C35 | IO16RSB0 |
| C36 | IO13RSB0 |
| C37 | GAC1/IO10RSB0 |
| C38 | NC |
| C39 | GAA0/IO05RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| 132-Pin QFN | |
|-------------|---------------------|
| Pin Number | A3P125 Function |
| A1 | GAB2/IO69RSB1 |
| A2 | IO130RSB1 |
| A3 | V _{CC} B1 |
| A4 | GFC1/IO126RSB1 |
| A5 | GFB0/IO123RSB1 |
| A6 | V _{CC} PLF |
| A7 | GFA1/IO121RSB1 |
| A8 | GFC2/IO118RSB1 |
| A9 | IO115RSB1 |
| A10 | V _{CC} |
| A11 | GEB1/IO110RSB1 |
| A12 | GEA0/IO107RSB1 |
| A13 | GEC2/IO104RSB1 |
| A14 | IO100RSB1 |
| A15 | V _{CC} |
| A16 | IO99RSB1 |
| A17 | IO96RSB1 |
| A18 | IO94RSB1 |
| A19 | IO91RSB1 |
| A20 | IO85RSB1 |
| A21 | IO79RSB1 |
| A22 | V _{CC} |
| A23 | GDB2/IO71RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO61RSB0 |
| A27 | V _{CC} |
| A28 | IO60RSB0 |
| A29 | GCC2/IO59RSB0 |
| A30 | GCA2/IO57RSB0 |
| A31 | GCA0/IO56RSB0 |
| A32 | GCB1/IO53RSB0 |
| A33 | IO49RSB0 |
| A34 | V _{CC} |
| A35 | IO44RSB0 |
| A36 | GBA2/IO41RSB0 |

| 132-Pin QFN | |
|-------------|---------------------|
| Pin Number | A3P125 Function |
| A37 | GBB1/IO38RSB0 |
| A38 | GBC0/IO35RSB0 |
| A39 | V _{CC} B0 |
| A40 | IO28RSB0 |
| A41 | IO22RSB0 |
| A42 | IO18RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | IO07RSB0 |
| A46 | V _{CC} |
| A47 | GAC1/IO05RSB0 |
| A48 | GAB0/IO02RSB0 |
| B1 | IO68RSB1 |
| B2 | GAC2/IO131RSB1 |
| B3 | GND |
| B4 | GFC0/IO125RSB1 |
| B5 | V _{COMPLF} |
| B6 | GND |
| B7 | GFB2/IO119RSB1 |
| B8 | IO116RSB1 |
| B9 | GND |
| B10 | GEB0/IO109RSB1 |
| B11 | VMV1 |
| B12 | GEB2/IO105RSB1 |
| B13 | IO101RSB1 |
| B14 | GND |
| B15 | IO98RSB1 |
| B16 | IO95RSB1 |
| B17 | GND |
| B18 | IO87RSB1 |
| B19 | IO81RSB1 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO62RSB0 |

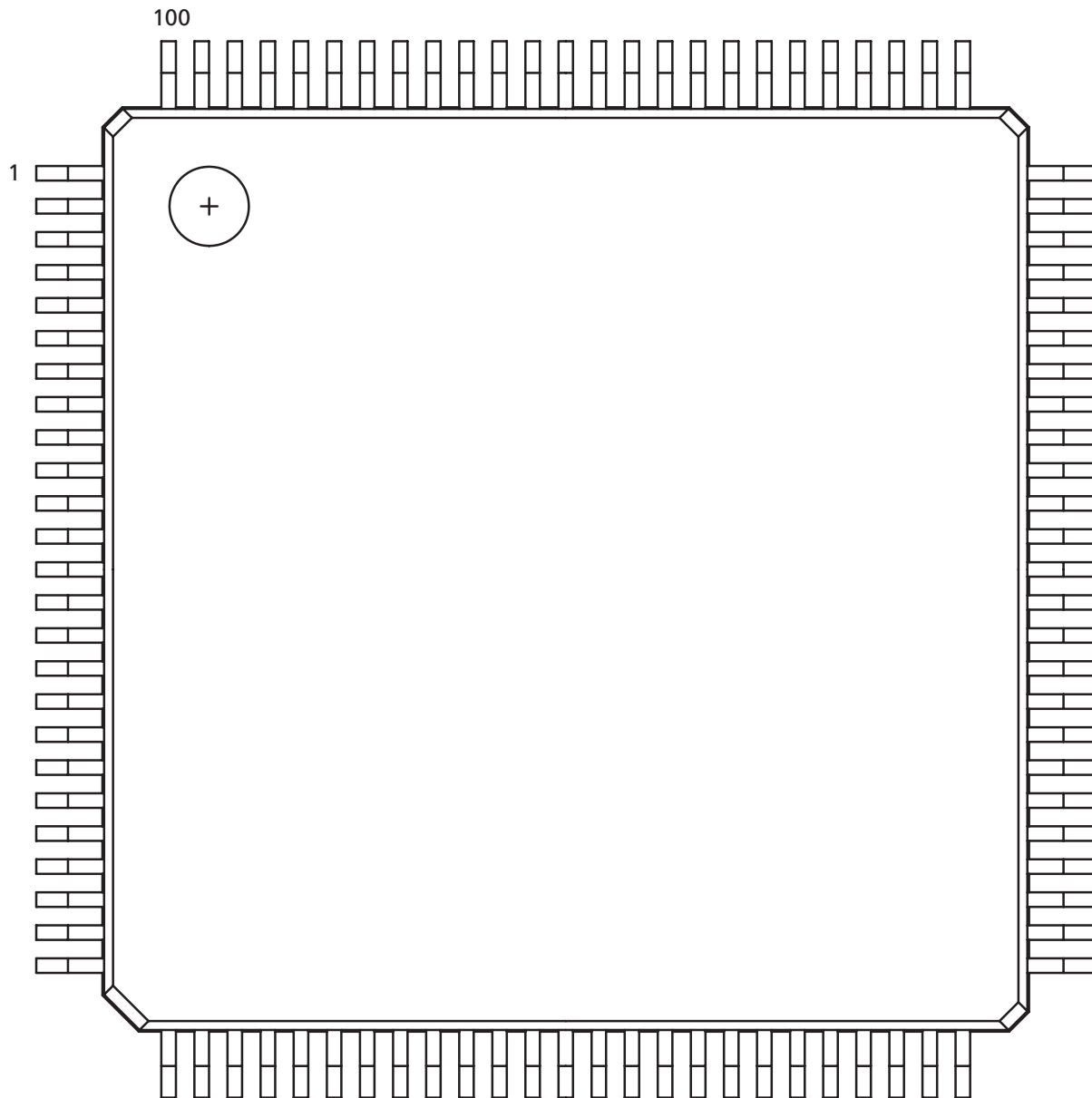
| 132-Pin QFN | |
|-------------|--------------------|
| Pin Number | A3P125 Function |
| B25 | GND |
| B26 | NC |
| B27 | GCB2/IO58RSB0 |
| B28 | GND |
| B29 | GCB0/IO54RSB0 |
| B30 | GCC1/IO51RSB0 |
| B31 | GND |
| B32 | GBB2/IO43RSB0 |
| B33 | VMV0 |
| B34 | GBA0/IO39RSB0 |
| B35 | GBC1/IO36RSB0 |
| B36 | GND |
| B37 | IO26RSB0 |
| B38 | IO21RSB0 |
| B39 | GND |
| B40 | IO13RSB0 |
| B41 | IO08RSB0 |
| B42 | GND |
| B43 | GAC0/IO04RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO67RSB1 |
| C2 | IO132RSB1 |
| C3 | V _{CC} |
| C4 | GFB1/IO124RSB1 |
| C5 | GFA0/IO122RSB1 |
| C6 | GFA2/IO120RSB1 |
| C7 | IO117RSB1 |
| C8 | V _{CC} B1 |
| C9 | GEA1/IO108RSB1 |
| C10 | GNDQ |
| C11 | GEA2/IO106RSB1 |
| C12 | IO103RSB1 |
| C13 | V _{CC} B1 |
| C14 | IO97RSB1 |
| C15 | IO93RSB1 |
| C16 | IO89RSB1 |

| 132-Pin QFN | |
|-------------|--------------------|
| Pin Number | A3P125 Function |
| C17 | IO83RSB1 |
| C18 | V _{CC} B1 |
| C19 | TCK |
| C20 | VMV1 |
| C21 | V _{PUMP} |
| C22 | V _{JTAG} |
| C23 | V _{CC} B0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO55RSB0 |
| C27 | GCC0/IO52RSB0 |
| C28 | V _{CC} B0 |
| C29 | IO42RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | V _{CC} |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | V _{CC} B0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| 132-Pin QFN | | 132-Pin QFN | | 132-Pin QFN | |
|-------------|---------------------|-------------|---------------------|-------------|--------------------|
| Pin Number | A3P250 Function | Pin Number | A3P250 Function | Pin Number | A3P250 Function |
| A1 | GAB2/IO117UPB3 | A37 | GBB1/IO38RSB0 | B25 | GND |
| A2 | IO117VPB3 | A38 | GBC0/IO35RSB0 | B26 | IO54PDB1 |
| A3 | V _{CC} B3 | A39 | V _{CC} B0 | B27 | GCB2/IO52PDB1 |
| A4 | GFC1/IO110PDB3 | A40 | IO28RSB0 | B28 | GND |
| A5 | GFB0/IO109NPB3 | A41 | IO22RSB0 | B29 | GCB0/IO49NDB1 |
| A6 | V _{CC} PLF | A42 | IO18RSB0 | B30 | GCC1/IO48PDB1 |
| A7 | GFA1/IO108PPB3 | A43 | IO14RSB0 | B31 | GND |
| A8 | GFC2/IO105PPB3 | A44 | IO11RSB0 | B32 | GBB2/IO42PDB1 |
| A9 | IO103NDB3 | A45 | IO07RSB0 | B33 | VMV1 |
| A10 | V _{CC} | A46 | V _{CC} | B34 | GBA0/IO39RSB0 |
| A11 | GEA1/IO98PPB3 | A47 | GAC1/IO05RSB0 | B35 | GBC1/IO36RSB0 |
| A12 | GEA0/IO98NPB3 | A48 | GAB0/IO02RSB0 | B36 | GND |
| A13 | GEC2/IO95RSB2 | B1 | IO118VDB3 | B37 | IO26RSB0 |
| A14 | IO91RSB2 | B2 | GAC2/IO116UDB3 | B38 | IO21RSB0 |
| A15 | V _{CC} | B3 | GND | B39 | GND |
| A16 | IO90RSB2 | B4 | GFC0/IO110NDB3 | B40 | IO13RSB0 |
| A17 | IO87RSB2 | B5 | V _{COMPLF} | B41 | IO08RSB0 |
| A18 | IO85RSB2 | B6 | GND | B42 | GND |
| A19 | IO82RSB2 | B7 | GFB2/IO106PSB3 | B43 | GAC0/IO04RSB0 |
| A20 | IO76RSB2 | B8 | IO103PDB3 | B44 | GNDQ |
| A21 | IO70RSB2 | B9 | GND | C1 | GAA2/IO118UDB3 |
| A22 | V _{CC} | B10 | GEB0/IO99NDB3 | C2 | IO116VDB3 |
| A23 | GDB2/IO62RSB2 | B11 | VMV3 | C3 | V _{CC} |
| A24 | TDI | B12 | GEB2/IO96RSB2 | C4 | GFB1/IO109PPB3 |
| A25 | TRST | B13 | IO92RSB2 | C5 | GFA0/IO108NPB3 |
| A26 | GDC1/IO58UDB1 | B14 | GND | C6 | GFA2/IO107PSB3 |
| A27 | V _{CC} | B15 | IO89RSB2 | C7 | IO105NPB3 |
| A28 | IO54NDB1 | B16 | IO86RSB2 | C8 | V _{CC} B3 |
| A29 | IO52NDB1 | B17 | GND | C9 | GEB1/IO99PDB3 |
| A30 | GCA2/IO51PPB1 | B18 | IO78RSB2 | C10 | GNDQ |
| A31 | GCA0/IO50NPB1 | B19 | IO72RSB2 | C11 | GEA2/IO97RSB2 |
| A32 | GCB1/IO49PDB1 | B20 | GND | C12 | IO94RSB2 |
| A33 | IO47NSB1 | B21 | GNDQ | C13 | V _{CC} B2 |
| A34 | V _{CC} | B22 | TMS | C14 | IO88RSB2 |
| A35 | IO41NPB1 | B23 | TDO | C15 | IO84RSB2 |
| A36 | GBA2/IO41PPB1 | B24 | GDC0/IO58VDB1 | C16 | IO80RSB2 |

| 132-Pin QFN | |
|-------------|--------------------|
| Pin Number | A3P250 Function |
| C17 | IO74RSB2 |
| C18 | V _{CC} B2 |
| C19 | TCK |
| C20 | VMV2 |
| C21 | V _{PUMP} |
| C22 | V _{JTAG} |
| C23 | V _{CC} B1 |
| C24 | IO53NSB1 |
| C25 | IO51NPB1 |
| C26 | GCA1/IO50PPB1 |
| C27 | GCC0/IO48NDB1 |
| C28 | V _{CC} B1 |
| C29 | IO42NDB1 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | V _{CC} |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | V _{CC} B0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

100-Pin VQFP



Note: This is the top view of the package.

Figure 3-4 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P030 Function |
| 1 | GND |
| 2 | IO82RSB1 |
| 3 | IO81RSB1 |
| 4 | IO80RSB1 |
| 5 | IO79RSB1 |
| 6 | IO78RSB1 |
| 7 | IO77RSB1 |
| 8 | IO76RSB1 |
| 9 | GND |
| 10 | IO75RSB1 |
| 11 | IO74RSB1 |
| 12 | GEC0/IO73RSB1 |
| 13 | GEA0/IO72RSB1 |
| 14 | GEBO/IO71RSB1 |
| 15 | IO70RSB1 |
| 16 | IO69RSB1 |
| 17 | V _{CC} |
| 18 | V _{CC} B1 |
| 19 | IO68RSB1 |
| 20 | IO67RSB1 |
| 21 | IO66RSB1 |
| 22 | IO65RSB1 |
| 23 | IO64RSB1 |
| 24 | IO63RSB1 |
| 25 | IO62RSB1 |
| 26 | IO61RSB1 |
| 27 | IO60RSB1 |
| 28 | IO59RSB1 |
| 29 | IO58RSB1 |
| 30 | IO57RSB1 |
| 31 | IO56RSB1 |
| 32 | IO55RSB1 |
| 33 | IO54RSB1 |
| 34 | IO53RSB1 |
| 35 | IO52RSB1 |
| 36 | IO51RSB1 |

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P030 Function |
| 37 | V _{CC} |
| 38 | GND |
| 39 | V _{CC} B1 |
| 40 | IO49RSB1 |
| 41 | IO47RSB1 |
| 42 | IO46RSB1 |
| 43 | IO45RSB1 |
| 44 | IO44RSB1 |
| 45 | IO43RSB1 |
| 46 | IO42RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | NC |
| 51 | GND |
| 52 | V _{PUMP} |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | V _{JTAG} |
| 57 | IO41RSB0 |
| 58 | IO40RSB0 |
| 59 | IO39RSB0 |
| 60 | IO38RSB0 |
| 61 | IO37RSB0 |
| 62 | IO36RSB0 |
| 63 | GDB0/IO34RSB0 |
| 64 | GDA0/IO33RSB0 |
| 65 | GDC0/IO32RSB0 |
| 66 | V _{CC} B0 |
| 67 | GND |
| 68 | V _{CC} |
| 69 | IO31RSB0 |
| 70 | IO30RSB0 |
| 71 | IO29RSB0 |
| 72 | IO28RSB0 |

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P030 Function |
| 73 | IO27RSB0 |
| 74 | IO26RSB0 |
| 75 | IO25RSB0 |
| 76 | IO24RSB0 |
| 77 | IO23RSB0 |
| 78 | IO22RSB0 |
| 79 | IO21RSB0 |
| 80 | IO20RSB0 |
| 81 | IO19RSB0 |
| 82 | IO18RSB0 |
| 83 | IO17RSB0 |
| 84 | IO16RSB0 |
| 85 | IO15RSB0 |
| 86 | IO14RSB0 |
| 87 | V _{CC} B0 |
| 88 | GND |
| 89 | V _{CC} |
| 90 | IO12RSB0 |
| 91 | IO10RSB0 |
| 92 | IO08RSB0 |
| 93 | IO07RSB0 |
| 94 | IO06RSB0 |
| 95 | IO05RSB0 |
| 96 | IO04RSB0 |
| 97 | IO03RSB0 |
| 98 | IO02RSB0 |
| 99 | IO01RSB0 |
| 100 | IO00RSB0 |



| 100-Pin VQFP | |
|--------------|---------------------|
| Pin Number | A3P060 Function |
| 1 | GND |
| 2 | GAA2/IO51RSB1 |
| 3 | IO52RSB1 |
| 4 | GAB2/IO53RSB1 |
| 5 | IO95RSB1 |
| 6 | GAC2/IO94RSB1 |
| 7 | IO93RSB1 |
| 8 | IO92RSB1 |
| 9 | GND |
| 10 | GFB1/IO87RSB1 |
| 11 | GFB0/IO86RSB1 |
| 12 | V _{COMPLF} |
| 13 | GFA0/IO85RSB1 |
| 14 | V _{CCPLF} |
| 15 | GFA1/IO84RSB1 |
| 16 | GFA2/IO83RSB1 |
| 17 | V _{CC} |
| 18 | V _{CC1B1} |
| 19 | GEC1/IO77RSB1 |
| 20 | GEB1/IO75RSB1 |
| 21 | GEB0/IO74RSB1 |
| 22 | GEA1/IO73RSB1 |
| 23 | GEA0/IO72RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO71RSB1 |
| 27 | GEB2/IO70RSB1 |
| 28 | GEC2/IO69RSB1 |
| 29 | IO68RSB1 |
| 30 | IO67RSB1 |
| 31 | IO66RSB1 |
| 32 | IO65RSB1 |
| 33 | IO64RSB1 |
| 34 | IO63RSB1 |
| 35 | IO62RSB1 |
| 36 | IO61RSB1 |

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P060 Function |
| 37 | V _{CC} |
| 38 | GND |
| 39 | V _{CC1B1} |
| 40 | IO60RSB1 |
| 41 | IO59RSB1 |
| 42 | IO58RSB1 |
| 43 | IO57RSB1 |
| 44 | GDC2/IO56RSB1 |
| 45 | GDB2/IO55RSB1 |
| 46 | GDA2/IO54RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | V _{PUMP} |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | V _{JTAG} |
| 57 | GDA1/IO49RSB0 |
| 58 | GDC0/IO46RSB0 |
| 59 | GDC1/IO45RSB0 |
| 60 | GCC2/IO43RSB0 |
| 61 | GCB2/IO42RSB0 |
| 62 | GCA0/IO40RSB0 |
| 63 | GCA1/IO39RSB0 |
| 64 | GCC0/IO36RSB0 |
| 65 | GCC1/IO35RSB0 |
| 66 | V _{CC1B0} |
| 67 | GND |
| 68 | V _{CC} |
| 69 | IO31RSB0 |
| 70 | GBC2/IO29RSB0 |
| 71 | GBB2/IO27RSB0 |
| 72 | IO26RSB0 |

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P060 Function |
| 73 | GBA2/IO25RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO24RSB0 |
| 77 | GBA0/IO23RSB0 |
| 78 | GBB1/IO22RSB0 |
| 79 | GBB0/IO21RSB0 |
| 80 | GBC1/IO20RSB0 |
| 81 | GBC0/IO19RSB0 |
| 82 | IO18RSB0 |
| 83 | IO17RSB0 |
| 84 | IO15RSB0 |
| 85 | IO13RSB0 |
| 86 | IO11RSB0 |
| 87 | V _{CC1B0} |
| 88 | GND |
| 89 | V _{CC} |
| 90 | IO10RSB0 |
| 91 | IO09RSB0 |
| 92 | IO08RSB0 |
| 93 | GAC1/IO07RSB0 |
| 94 | GAC0/IO06RSB0 |
| 95 | GAB1/IO05RSB0 |
| 96 | GAB0/IO04RSB0 |
| 97 | GAA1/IO03RSB0 |
| 98 | GAA0/IO02RSB0 |
| 99 | IO01RSB0 |
| 100 | IO00RSB0 |

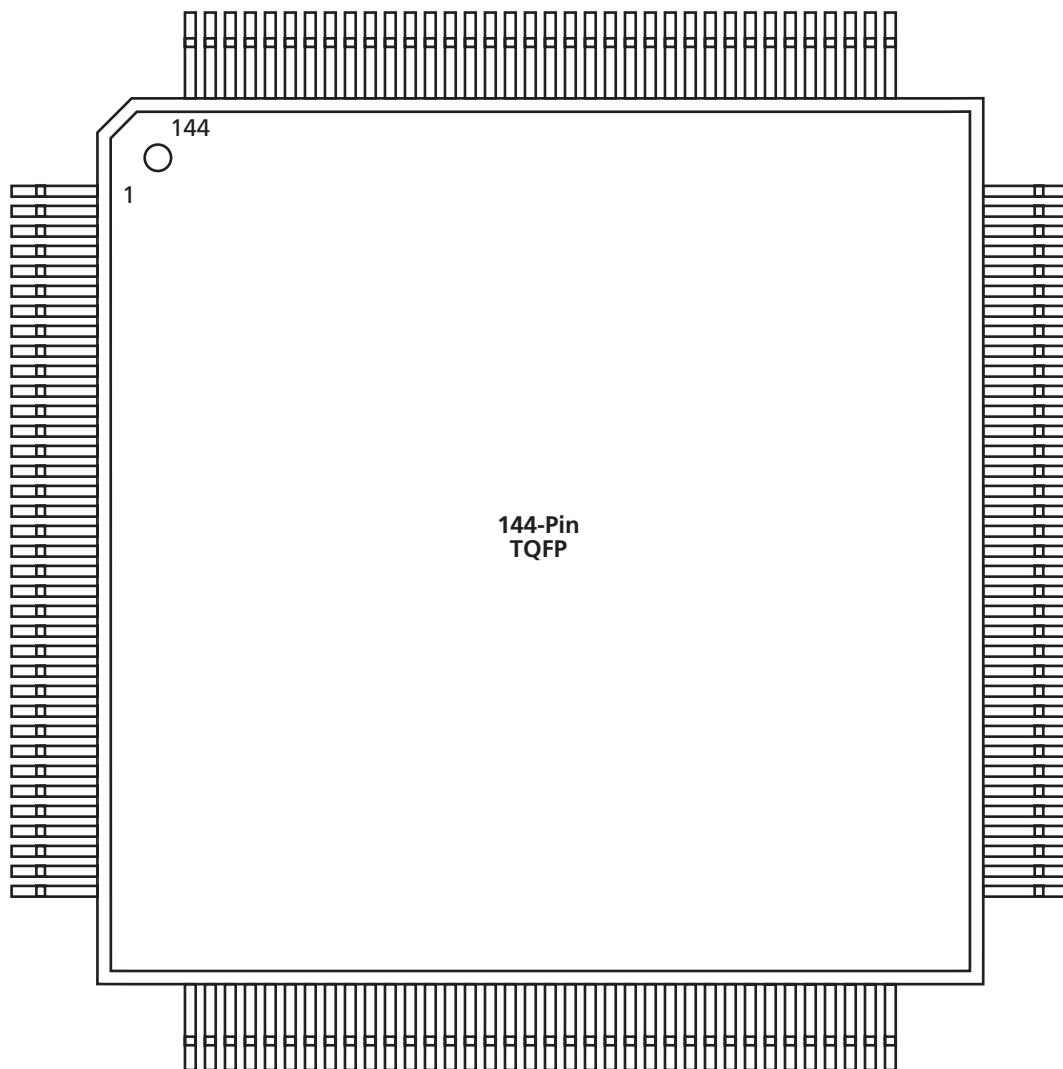
| 100-Pin VQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 1 | GND |
| 2 | GAA2/IO67RSB1 |
| 3 | IO68RSB1 |
| 4 | GAB2/IO69RSB1 |
| 5 | IO132RSB1 |
| 6 | GAC2/IO131RSB1 |
| 7 | IO130RSB1 |
| 8 | IO129RSB1 |
| 9 | GND |
| 10 | GFB1/IO124RSB1 |
| 11 | GFB0/IO123RSB1 |
| 12 | V _{COMPLF} |
| 13 | GFA0/IO122RSB1 |
| 14 | V _{CCPLF} |
| 15 | GFA1/IO121RSB1 |
| 16 | GFA2/IO120RSB1 |
| 17 | V _{CC} |
| 18 | V _{CCIB1} |
| 19 | GEC0/IO111RSB1 |
| 20 | GEB1/IO110RSB1 |
| 21 | GEB0/IO109RSB1 |
| 22 | GEA1/IO108RSB1 |
| 23 | GEA0/IO107RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO106RSB1 |
| 27 | GEB2/IO105RSB1 |
| 28 | GEC2/IO104RSB1 |
| 29 | IO102RSB1 |
| 30 | IO100RSB1 |
| 31 | IO99RSB1 |
| 32 | IO97RSB1 |
| 33 | IO96RSB1 |
| 34 | IO95RSB1 |
| 35 | IO94RSB1 |
| 36 | IO93RSB1 |

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P125 Function |
| 37 | V _{CC} |
| 38 | GND |
| 39 | V _{CCIB1} |
| 40 | IO87RSB1 |
| 41 | IO84RSB1 |
| 42 | IO81RSB1 |
| 43 | IO75RSB1 |
| 44 | GDC2/IO72RSB1 |
| 45 | GDB2/IO71RSB1 |
| 46 | GDA2/IO70RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | V _{PUMP} |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | V _{JTAG} |
| 57 | GDA1/IO65RSB0 |
| 58 | GDC0/IO62RSB0 |
| 59 | GDC1/IO61RSB0 |
| 60 | GCC2/IO59RSB0 |
| 61 | GCB2/IO58RSB0 |
| 62 | GCA0/IO56RSB0 |
| 63 | GCA1/IO55RSB0 |
| 64 | GCC0/IO52RSB0 |
| 65 | GCC1/IO51RSB0 |
| 66 | V _{CCIB0} |
| 67 | GND |
| 68 | V _{CC} |
| 69 | IO47RSB0 |
| 70 | GBC2/IO45RSB0 |
| 71 | GBB2/IO43RSB0 |
| 72 | IO42RSB0 |

| 100-Pin VQFP | |
|--------------|--------------------|
| Pin Number | A3P125 Function |
| 73 | GBA2/IO41RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO32RSB0 |
| 83 | IO28RSB0 |
| 84 | IO25RSB0 |
| 85 | IO22RSB0 |
| 86 | IO19RSB0 |
| 87 | V _{CCIB0} |
| 88 | GND |
| 89 | V _{CC} |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | IO09RSB0 |
| 94 | IO07RSB0 |
| 95 | GAC1/IO05RSB0 |
| 96 | GAC0/IO04RSB0 |
| 97 | GAB1/IO03RSB0 |
| 98 | GAB0/IO02RSB0 |
| 99 | GAA1/IO01RSB0 |
| 100 | GAA0/IO00RSB0 |

| 100-Pin VQFP | | 100-Pin VQFP | | 100-Pin VQFP | |
|--------------|---------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P250 Function | Pin Number | A3P250 Function | Pin Number | A3P250 Function |
| 1 | GND | 37 | V _{CC} | 73 | GBA2/IO41PDB1 |
| 2 | GAA2/IO118UDB3 | 38 | GND | 74 | VMV1 |
| 3 | IO118VDB3 | 39 | V _{CC} B2 | 75 | GNDQ |
| 4 | GAB2/IO117UDB3 | 40 | IO77RSB2 | 76 | GBA1/IO40RSB0 |
| 5 | IO117VDB3 | 41 | IO74RSB2 | 77 | GBA0/IO39RSB0 |
| 6 | GAC2/IO116UDB3 | 42 | IO71RSB2 | 78 | GBB1/IO38RSB0 |
| 7 | IO116VDB3 | 43 | GDC2/IO63RSB2 | 79 | GBB0/IO37RSB0 |
| 8 | IO112PSB3 | 44 | GDB2/IO62RSB2 | 80 | GBC1/IO36RSB0 |
| 9 | GND | 45 | GDA2/IO61RSB2 | 81 | GBC0/IO35RSB0 |
| 10 | GFB1/IO109PDB3 | 46 | GNDQ | 82 | IO29RSB0 |
| 11 | GFB0/IO109NDB3 | 47 | TCK | 83 | IO27RSB0 |
| 12 | V _{COMPLF} | 48 | TDI | 84 | IO25RSB0 |
| 13 | GFA0/IO108NPB3 | 49 | TMS | 85 | IO23RSB0 |
| 14 | V _{CCPLF} | 50 | VMV2 | 86 | IO21RSB0 |
| 15 | GFA1/IO108PPB3 | 51 | GND | 87 | V _{CC} B0 |
| 16 | GFA2/IO107PSB3 | 52 | V _{PUMP} | 88 | GND |
| 17 | V _{CC} | 53 | NC | 89 | V _{CC} |
| 18 | V _{CC} B3 | 54 | TDO | 90 | IO15RSB0 |
| 19 | GFC2/IO105PSB3 | 55 | TRST | 91 | IO13RSB0 |
| 20 | GEC1/IO100PDB3 | 56 | V _{JTAG} | 92 | IO11RSB0 |
| 21 | GEC0/IO100NDB3 | 57 | GDA1/IO60USB1 | 93 | GAC1/IO05RSB0 |
| 22 | GEA1/IO98PDB3 | 58 | GDC0/IO58VDB1 | 94 | GAC0/IO04RSB0 |
| 23 | GEA0/IO98NDB3 | 59 | GDC1/IO58UDB1 | 95 | GAB1/IO03RSB0 |
| 24 | VMV3 | 60 | IO52NDB1 | 96 | GAB0/IO02RSB0 |
| 25 | GNDQ | 61 | GCB2/IO52PDB1 | 97 | GAA1/IO01RSB0 |
| 26 | GEA2/IO97RSB2 | 62 | GCA1/IO50PDB1 | 98 | GAA0/IO00RSB0 |
| 27 | GEB2/IO96RSB2 | 63 | GCA0/IO50NDB1 | 99 | GNDQ |
| 28 | GEC2/IO95RSB2 | 64 | GCC0/IO48NDB1 | 100 | VMV0 |
| 29 | IO93RSB2 | 65 | GCC1/IO48PDB1 | | |
| 30 | IO92RSB2 | 66 | V _{CC} B1 | | |
| 31 | IO91RSB2 | 67 | GND | | |
| 32 | IO90RSB2 | 68 | V _{CC} | | |
| 33 | IO88RSB2 | 69 | IO43NDB1 | | |
| 34 | IO86RSB2 | 70 | GBC2/IO43PDB1 | | |
| 35 | IO85RSB2 | 71 | GBB2/IO42PSB1 | | |
| 36 | IO84RSB2 | 72 | IO41NDB1 | | |

144-Pin TQFP



Note: This is the top view of the package.

Figure 3-5 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 144-Pin TQFP | | 144-Pin TQFP | | 144-Pin TQFP | |
|--------------|---------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P060 Function | Pin Number | A3P060 Function | Pin Number | A3P060 Function |
| 1 | GAA2/IO51RSB1 | 37 | NC | 73 | V _{PUMP} |
| 2 | IO52RSB1 | 38 | GEA2/IO71RSB1 | 74 | NC |
| 3 | GAB2/IO53RSB1 | 39 | GEB2/IO70RSB1 | 75 | TDO |
| 4 | IO95RSB1 | 40 | GEC2/IO69RSB1 | 76 | TRST |
| 5 | GAC2/IO94RSB1 | 41 | IO68RSB1 | 77 | V _{JTAG} |
| 6 | IO93RSB1 | 42 | IO67RSB1 | 78 | GDA0/IO50RSB0 |
| 7 | IO92RSB1 | 43 | IO66RSB1 | 79 | GDB0/IO48RSB0 |
| 8 | IO91RSB1 | 44 | IO65RSB1 | 80 | GDB1/IO47RSB0 |
| 9 | V _{CC} | 45 | V _{CC} | 81 | V _{CC} B0 |
| 10 | GND | 46 | GND | 82 | GND |
| 11 | V _{CC} B1 | 47 | V _{CC} B1 | 83 | IO44RSB0 |
| 12 | IO90RSB1 | 48 | NC | 84 | GCC2/IO43RSB0 |
| 13 | GFC1/IO89RSB1 | 49 | IO64RSB1 | 85 | GCB2/IO42RSB0 |
| 14 | GFC0/IO88RSB1 | 50 | NC | 86 | GCA2/IO41RSB0 |
| 15 | GFB1/IO87RSB1 | 51 | IO63RSB1 | 87 | GCA0/IO40RSB0 |
| 16 | GFB0/IO86RSB1 | 52 | NC | 88 | GCA1/IO39RSB0 |
| 17 | V _{COMPLF} | 53 | IO62RSB1 | 89 | GCB0/IO38RSB0 |
| 18 | GFA0/IO85RSB1 | 54 | NC | 90 | GCB1/IO37RSB0 |
| 19 | V _{CC} PLF | 55 | IO61RSB1 | 91 | GCC0/IO36RSB0 |
| 20 | GFA1/IO84RSB1 | 56 | NC | 92 | GCC1/IO35RSB0 |
| 21 | GFA2/IO83RSB1 | 57 | NC | 93 | IO34RSB0 |
| 22 | GFB2/IO82RSB1 | 58 | IO60RSB1 | 94 | IO33RSB0 |
| 23 | GFC2/IO81RSB1 | 59 | IO59RSB1 | 95 | NC |
| 24 | IO80RSB1 | 60 | IO58RSB1 | 96 | NC |
| 25 | IO79RSB1 | 61 | IO57RSB1 | 97 | NC |
| 26 | IO78RSB1 | 62 | NC | 98 | V _{CC} B0 |
| 27 | GND | 63 | GND | 99 | GND |
| 28 | V _{CC} B1 | 64 | NC | 100 | V _{CC} |
| 29 | GEC1/IO77RSB1 | 65 | GDC2/IO56RSB1 | 101 | IO30RSB0 |
| 30 | GEC0/IO76RSB1 | 66 | GDB2/IO55RSB1 | 102 | GBC2/IO29RSB0 |
| 31 | GEB1/IO75RSB1 | 67 | GDA2/IO54RSB1 | 103 | IO28RSB0 |
| 32 | GEB0/IO74RSB1 | 68 | GNDQ | 104 | GBB2/IO27RSB0 |
| 33 | GEA1/IO73RSB1 | 69 | TCK | 105 | IO26RSB0 |
| 34 | GEA0/IO72RSB1 | 70 | TDI | 106 | GBA2/IO25RSB0 |
| 35 | VMV1 | 71 | TMS | 107 | VMV0 |
| 36 | GNDQ | 72 | VMV1 | 108 | GNDQ |

| 144-Pin TQFP | |
|--------------|---------------------|
| Pin Number | A3P060 Function |
| 109 | NC |
| 110 | NC |
| 111 | GBA1/IO24RSB0 |
| 112 | GBA0/IO23RSB0 |
| 113 | GBB1/IO22RSB0 |
| 114 | GBB0/IO21RSB0 |
| 115 | GBC1/IO20RSB0 |
| 116 | GBC0/IO19RSB0 |
| 117 | V _{CCI} B0 |
| 118 | GND |
| 119 | V _{CC} |
| 120 | IO18RSB0 |
| 121 | IO17RSB0 |
| 122 | IO16RSB0 |
| 123 | IO15RSB0 |
| 124 | IO14RSB0 |
| 125 | IO13RSB0 |
| 126 | IO12RSB0 |
| 127 | IO11RSB0 |
| 128 | NC |
| 129 | IO10RSB0 |
| 130 | IO09RSB0 |
| 131 | IO08RSB0 |
| 132 | GAC1/IO07RSB0 |
| 133 | GAC0/IO06RSB0 |
| 134 | NC |
| 135 | GND |
| 136 | NC |
| 137 | GAB1/IO05RSB0 |
| 138 | GAB0/IO04RSB0 |
| 139 | GAA1/IO03RSB0 |
| 140 | GAA0/IO02RSB0 |
| 141 | IO01RSB0 |
| 142 | IO00RSB0 |
| 143 | GNDQ |
| 144 | VMV0 |

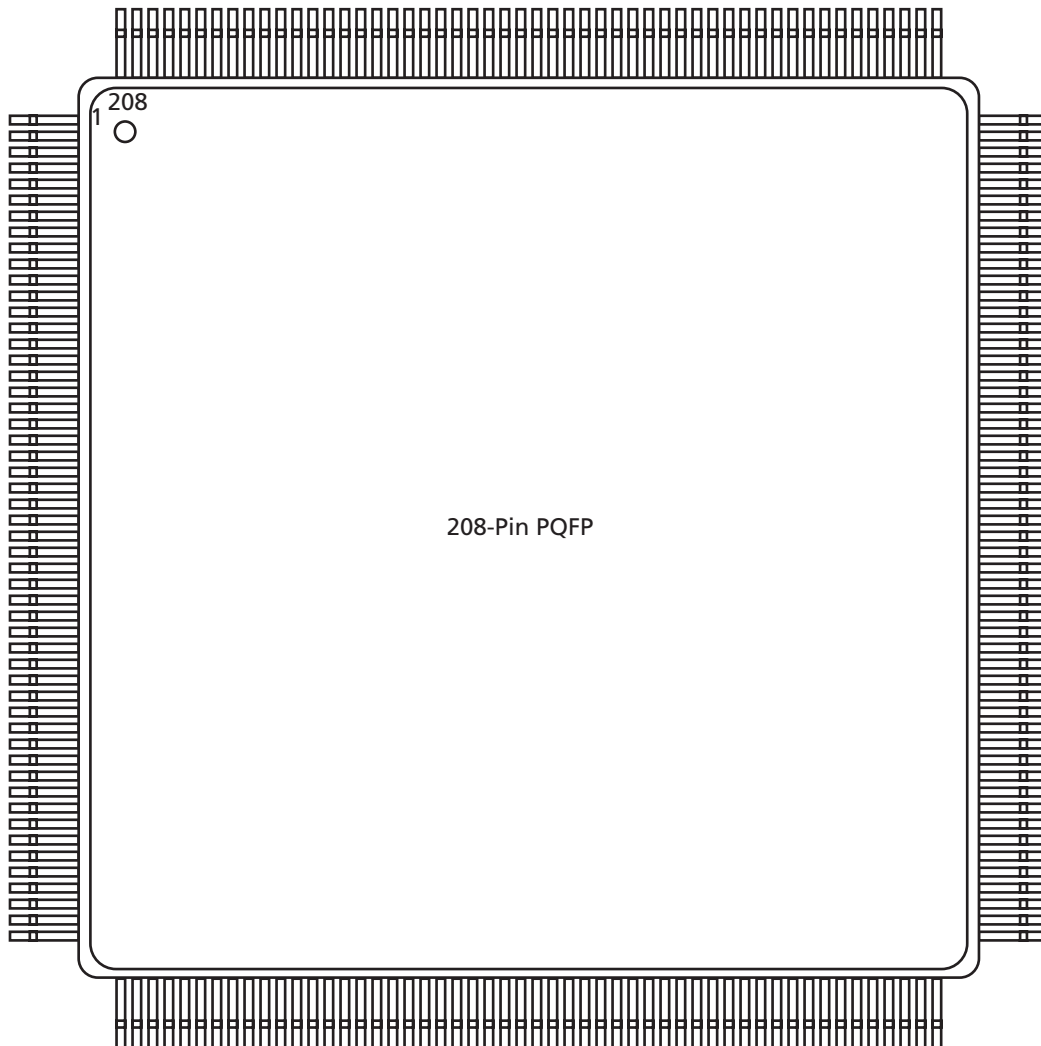
| 144-Pin TQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 1 | GAA2/IO67RSB1 |
| 2 | IO68RSB1 |
| 3 | GAB2/IO69RSB1 |
| 4 | IO132RSB1 |
| 5 | GAC2/IO131RSB1 |
| 6 | IO130RSB1 |
| 7 | IO129RSB1 |
| 8 | IO128RSB1 |
| 9 | V _{CC} |
| 10 | GND |
| 11 | V _{CC1} B1 |
| 12 | IO127RSB1 |
| 13 | GFC1/IO126RSB1 |
| 14 | GFC0/IO125RSB1 |
| 15 | GFB1/IO124RSB1 |
| 16 | GFB0/IO123RSB1 |
| 17 | V _{COMPLF} |
| 18 | GFA0/IO122RSB1 |
| 19 | V _{CCPLF} |
| 20 | GFA1/IO121RSB1 |
| 21 | GFA2/IO120RSB1 |
| 22 | GFB2/IO119RSB1 |
| 23 | GFC2/IO118RSB1 |
| 24 | IO117RSB1 |
| 25 | IO116RSB1 |
| 26 | IO115RSB1 |
| 27 | GND |
| 28 | V _{CC1} B1 |
| 29 | GEC1/IO112RSB1 |
| 30 | GEC0/IO111RSB1 |
| 31 | GEB1/IO110RSB1 |
| 32 | GEB0/IO109RSB1 |
| 33 | GEA1/IO108RSB1 |
| 34 | GEA0/IO107RSB1 |
| 35 | VMV1 |
| 36 | GNDQ |

| 144-Pin TQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 37 | NC |
| 38 | GEA2/IO106RSB1 |
| 39 | GEB2/IO105RSB1 |
| 40 | GEC2/IO104RSB1 |
| 41 | IO103RSB1 |
| 42 | IO102RSB1 |
| 43 | IO101RSB1 |
| 44 | IO100RSB1 |
| 45 | V _{CC} |
| 46 | GND |
| 47 | V _{CC1} B1 |
| 48 | IO99RSB1 |
| 49 | IO97RSB1 |
| 50 | IO95RSB1 |
| 51 | IO93RSB1 |
| 52 | IO92RSB1 |
| 53 | IO90RSB1 |
| 54 | IO88RSB1 |
| 55 | IO86RSB1 |
| 56 | IO84RSB1 |
| 57 | IO83RSB1 |
| 58 | IO82RSB1 |
| 59 | IO81RSB1 |
| 60 | IO80RSB1 |
| 61 | IO79RSB1 |
| 62 | V _{CC} |
| 63 | GND |
| 64 | V _{CC1} B1 |
| 65 | GDC2/IO72RSB1 |
| 66 | GDB2/IO71RSB1 |
| 67 | GDA2/IO70RSB1 |
| 68 | GNDQ |
| 69 | TCK |
| 70 | TDI |
| 71 | TMS |
| 72 | VMV1 |

| 144-Pin TQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 73 | V _{PUMP} |
| 74 | NC |
| 75 | TDO |
| 76 | TRST |
| 77 | V _{JTAG} |
| 78 | GDA0/IO66RSB0 |
| 79 | GDB0/IO64RSB0 |
| 80 | GDB1/IO63RSB0 |
| 81 | V _{CC1} B0 |
| 82 | GND |
| 83 | IO60RSB0 |
| 84 | GCC2/IO59RSB0 |
| 85 | GCB2/IO58RSB0 |
| 86 | GCA2/IO57RSB0 |
| 87 | GCA0/IO56RSB0 |
| 88 | GCA1/IO55RSB0 |
| 89 | GCB0/IO54RSB0 |
| 90 | GCB1/IO53RSB0 |
| 91 | GCC0/IO52RSB0 |
| 92 | GCC1/IO51RSB0 |
| 93 | IO50RSB0 |
| 94 | IO49RSB0 |
| 95 | NC |
| 96 | NC |
| 97 | NC |
| 98 | V _{CC1} B0 |
| 99 | GND |
| 100 | V _{CC} |
| 101 | IO47RSB0 |
| 102 | GBC2/IO45RSB0 |
| 103 | IO44RSB0 |
| 104 | GBB2/IO43RSB0 |
| 105 | IO42RSB0 |
| 106 | GBA2/IO41RSB0 |
| 107 | VMV0 |
| 108 | GNDQ |

| 144-Pin TQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 109 | GBA1/IO40RSB0 |
| 110 | GBA0/IO39RSB0 |
| 111 | GBB1/IO38RSB0 |
| 112 | GBB0/IO37RSB0 |
| 113 | GBC1/IO36RSB0 |
| 114 | GBC0/IO35RSB0 |
| 115 | IO34RSB0 |
| 116 | IO33RSB0 |
| 117 | V _{CCI} B0 |
| 118 | GND |
| 119 | V _{CC} |
| 120 | IO29RSB0 |
| 121 | IO28RSB0 |
| 122 | IO27RSB0 |
| 123 | IO25RSB0 |
| 124 | IO23RSB0 |
| 125 | IO21RSB0 |
| 126 | IO19RSB0 |
| 127 | IO17RSB0 |
| 128 | IO16RSB0 |
| 129 | IO14RSB0 |
| 130 | IO12RSB0 |
| 131 | IO10RSB0 |
| 132 | IO08RSB0 |
| 133 | IO06RSB0 |
| 134 | V _{CCI} B0 |
| 135 | GND |
| 136 | V _{CC} |
| 137 | GAC1/IO05RSB0 |
| 138 | GAC0/IO04RSB0 |
| 139 | GAB1/IO03RSB0 |
| 140 | GAB0/IO02RSB0 |
| 141 | GAA1/IO01RSB0 |
| 142 | GAA0/IO00RSB0 |
| 143 | GNDQ |
| 144 | VMV0 |

208-Pin PQFP



Note: This is the top view of the package.

Figure 3-6 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 208-Pin PQFP | |
|--------------|----------------------|
| Pin Number | A3P125 Function |
| 1 | GND |
| 2 | GAA2/IO67RSB1 |
| 3 | IO68RSB1 |
| 4 | GAB2/IO69RSB1 |
| 5 | IO132RSB1 |
| 6 | GAC2/IO131RSB1 |
| 7 | NC |
| 8 | NC |
| 9 | IO130RSB1 |
| 10 | IO129RSB1 |
| 11 | NC |
| 12 | IO128RSB1 |
| 13 | NC |
| 14 | NC |
| 15 | NC |
| 16 | V _{CC} |
| 17 | GND |
| 18 | V _{CC1} B1 |
| 19 | IO127RSB1 |
| 20 | NC |
| 21 | GFC1/IO126RSB1 |
| 22 | GFC0/IO125RSB1 |
| 23 | GFB1/IO124RSB1 |
| 24 | GFB0/IO123RSB1 |
| 25 | V _{CCOMPLF} |
| 26 | GFA0/IO122RSB1 |
| 27 | V _{CCPLF} |
| 28 | GFA1/IO121RSB1 |
| 29 | GND |
| 30 | GFA2/IO120RSB1 |
| 31 | NC |
| 32 | GFB2/IO119RSB1 |
| 33 | NC |
| 34 | GFC2/IO118RSB1 |
| 35 | IO117RSB1 |
| 36 | NC |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 37 | IO116RSB1 |
| 38 | IO115RSB1 |
| 39 | NC |
| 40 | V _{CC1} B1 |
| 41 | GND |
| 42 | IO114RSB1 |
| 43 | IO113RSB1 |
| 44 | GEC1/IO112RSB1 |
| 45 | GEC0/IO111RSB1 |
| 46 | GEB1/IO110RSB1 |
| 47 | GEB0/IO109RSB1 |
| 48 | GEA1/IO108RSB1 |
| 49 | GEA0/IO107RSB1 |
| 50 | VMV1 |
| 51 | GNDQ |
| 52 | GND |
| 53 | NC |
| 54 | NC |
| 55 | GEA2/IO106RSB1 |
| 56 | GEB2/IO105RSB1 |
| 57 | GEC2/IO104RSB1 |
| 58 | IO103RSB1 |
| 59 | IO102RSB1 |
| 60 | IO101RSB1 |
| 61 | IO100RSB1 |
| 62 | V _{CC1} B1 |
| 63 | IO99RSB1 |
| 64 | IO98RSB1 |
| 65 | GND |
| 66 | IO97RSB1 |
| 67 | IO96RSB1 |
| 68 | IO95RSB1 |
| 69 | IO94RSB1 |
| 70 | IO93RSB1 |
| 71 | V _{CC} |
| 72 | V _{CC1} B1 |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| 73 | IO92RSB1 |
| 74 | IO91RSB1 |
| 75 | IO90RSB1 |
| 76 | IO89RSB1 |
| 77 | IO88RSB1 |
| 78 | IO87RSB1 |
| 79 | IO86RSB1 |
| 80 | IO85RSB1 |
| 81 | GND |
| 82 | IO84RSB1 |
| 83 | IO83RSB1 |
| 84 | IO82RSB1 |
| 85 | IO81RSB1 |
| 86 | IO80RSB1 |
| 87 | IO79RSB1 |
| 88 | V _{CC} |
| 89 | V _{CC1} B1 |
| 90 | IO78RSB1 |
| 91 | IO77RSB1 |
| 92 | IO76RSB1 |
| 93 | IO75RSB1 |
| 94 | IO74RSB1 |
| 95 | IO73RSB1 |
| 96 | GDC2/IO72RSB1 |
| 97 | GND |
| 98 | GDB2/IO71RSB1 |
| 99 | GDA2/IO70RSB1 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV1 |
| 105 | GND |
| 106 | V _{PUMP} |
| 107 | NC |
| 108 | TDO |

| 208-Pin PQFP | | 208-Pin PQFP | | 208-Pin PQFP | |
|--------------|---------------------------------|--------------|---------------------------------|--------------|---------------------------------|
| Pin Number | A3P125 Function | Pin Number | A3P125 Function | Pin Number | A3P125 Function |
| 109 | TRST | 145 | IO46RSB0 | 181 | IO21RSB0 |
| 110 | V _{JTAG} | 146 | NC | 182 | IO20RSB0 |
| 111 | GDA0/IO66RSB0 | 147 | NC | 183 | IO19RSB0 |
| 112 | GDA1/IO65RSB0 | 148 | NC | 184 | IO18RSB0 |
| 113 | GDB0/IO64RSB0 | 149 | GBC2/IO45RSB0 | 185 | IO17RSB0 |
| 114 | GDB1/IO63RSB0 | 150 | IO44RSB0 | 186 | V _{CC} I _{B0} |
| 115 | GDC0/IO62RSB0 | 151 | GBB2/IO43RSB0 | 187 | V _{CC} |
| 116 | GDC1/IO61RSB0 | 152 | IO42RSB0 | 188 | IO16RSB0 |
| 117 | NC | 153 | GBA2/IO41RSB0 | 189 | IO15RSB0 |
| 118 | NC | 154 | VMV0 | 190 | IO14RSB0 |
| 119 | NC | 155 | GNDQ | 191 | IO13RSB0 |
| 120 | NC | 156 | GND | 192 | IO12RSB0 |
| 121 | NC | 157 | NC | 193 | IO11RSB0 |
| 122 | GND | 158 | GBA1/IO40RSB0 | 194 | IO10RSB0 |
| 123 | V _{CC} I _{B0} | 159 | GBA0/IO39RSB0 | 195 | GND |
| 124 | NC | 160 | GBB1/IO38RSB0 | 196 | IO09RSB0 |
| 125 | NC | 161 | GBB0/IO37RSB0 | 197 | IO08RSB0 |
| 126 | V _{CC} | 162 | GND | 198 | IO07RSB0 |
| 127 | IO60RSB0 | 163 | GBC1/IO36RSB0 | 199 | IO06RSB0 |
| 128 | GCC2/IO59RSB0 | 164 | GBC0/IO35RSB0 | 200 | V _{CC} I _{B0} |
| 129 | GCB2/IO58RSB0 | 165 | IO34RSB0 | 201 | GAC1/IO05RSB0 |
| 130 | GND | 166 | IO33RSB0 | 202 | GAC0/IO04RSB0 |
| 131 | GCA2/IO57RSB0 | 167 | IO32RSB0 | 203 | GAB1/IO03RSB0 |
| 132 | GCA0/IO56RSB0 | 168 | IO31RSB0 | 204 | GAB0/IO02RSB0 |
| 133 | GCA1/IO55RSB0 | 169 | IO30RSB0 | 205 | GAA1/IO01RSB0 |
| 134 | GCB0/IO54RSB0 | 170 | V _{CC} I _{B0} | 206 | GAA0/IO00RSB0 |
| 135 | GCB1/IO53RSB0 | 171 | V _{CC} | 207 | GNDQ |
| 136 | GCC0/IO52RSB0 | 172 | IO29RSB0 | 208 | VMV0 |
| 137 | GCC1/IO51RSB0 | 173 | IO28RSB0 | | |
| 138 | IO50RSB0 | 174 | IO27RSB0 | | |
| 139 | IO49RSB0 | 175 | IO26RSB0 | | |
| 140 | V _{CC} I _{B0} | 176 | IO25RSB0 | | |
| 141 | GND | 177 | IO24RSB0 | | |
| 142 | V _{CC} | 178 | GND | | |
| 143 | IO48RSB0 | 179 | IO23RSB0 | | |
| 144 | IO47RSB0 | 180 | IO22RSB0 | | |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P250 Function |
| 1 | GND |
| 2 | GAA2/IO118UDB3 |
| 3 | IO118VDB3 |
| 4 | GAB2/IO117UDB3 |
| 5 | IO117VDB3 |
| 6 | GAC2/IO116UDB3 |
| 7 | IO116VDB3 |
| 8 | IO115UDB3 |
| 9 | IO115VDB3 |
| 10 | IO114UDB3 |
| 11 | IO114VDB3 |
| 12 | IO113PDB3 |
| 13 | IO113NDB3 |
| 14 | IO112PDB3 |
| 15 | IO112NDB3 |
| 16 | V _{CC} |
| 17 | GND |
| 18 | V _{CC} B3 |
| 19 | IO111PDB3 |
| 20 | IO111NDB3 |
| 21 | GFC1/IO110PDB3 |
| 22 | GFC0/IO110NDB3 |
| 23 | GFB1/IO109PDB3 |
| 24 | GFB0/IO109NDB3 |
| 25 | V _{COMPLF} |
| 26 | GFA0/IO108NPB3 |
| 27 | V _{CC} PLF |
| 28 | GFA1/IO108PPB3 |
| 29 | GND |
| 30 | GFA2/IO107PDB3 |
| 31 | IO107NDB3 |
| 32 | GFB2/IO106PDB3 |
| 33 | IO106NDB3 |
| 34 | GFC2/IO105PDB3 |
| 35 | IO105NDB3 |
| 36 | NC |

| 208-Pin PQFP | |
|--------------|--------------------|
| Pin Number | A3P250 Function |
| 37 | IO104PDB3 |
| 38 | IO104NDB3 |
| 39 | IO103PSB3 |
| 40 | V _{CC} B3 |
| 41 | GND |
| 42 | IO101PDB3 |
| 43 | IO101NDB3 |
| 44 | GEC1/IO100PDB3 |
| 45 | GEC0/IO100NDB3 |
| 46 | GEB1/IO99PDB3 |
| 47 | GEB0/IO99NDB3 |
| 48 | GEA1/IO98PDB3 |
| 49 | GEA0/IO98NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | NC |
| 54 | NC |
| 55 | GEA2/IO97RSB2 |
| 56 | GEB2/IO96RSB2 |
| 57 | GEC2/IO95RSB2 |
| 58 | IO94RSB2 |
| 59 | IO93RSB2 |
| 60 | IO92RSB2 |
| 61 | IO91RSB2 |
| 62 | V _{CC} B2 |
| 63 | IO90RSB2 |
| 64 | IO89RSB2 |
| 65 | GND |
| 66 | IO88RSB2 |
| 67 | IO87RSB2 |
| 68 | IO86RSB2 |
| 69 | IO85RSB2 |
| 70 | IO84RSB2 |
| 71 | V _{CC} |
| 72 | V _{CC} B2 |

| 208-Pin PQFP | |
|--------------|--------------------|
| Pin Number | A3P250 Function |
| 73 | IO83RSB2 |
| 74 | IO82RSB2 |
| 75 | IO81RSB2 |
| 76 | IO80RSB2 |
| 77 | IO79RSB2 |
| 78 | IO78RSB2 |
| 79 | IO77RSB2 |
| 80 | IO76RSB2 |
| 81 | GND |
| 82 | IO75RSB2 |
| 83 | IO74RSB2 |
| 84 | IO73RSB2 |
| 85 | IO72RSB2 |
| 86 | IO71RSB2 |
| 87 | IO70RSB2 |
| 88 | V _{CC} |
| 89 | V _{CC} B2 |
| 90 | IO69RSB2 |
| 91 | IO68RSB2 |
| 92 | IO67RSB2 |
| 93 | IO66RSB2 |
| 94 | IO65RSB2 |
| 95 | IO64RSB2 |
| 96 | GDC2/IO63RSB2 |
| 97 | GND |
| 98 | GDB2/IO62RSB2 |
| 99 | GDA2/IO61RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | V _{PUMP} |
| 107 | NC |
| 108 | TDO |

| 208-Pin PQFP | | 208-Pin PQFP | | 208-Pin PQFP | |
|--------------|--------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P250 Function | Pin Number | A3P250 Function | Pin Number | A3P250 Function |
| 109 | TRST | 145 | IO45PDB1 | 181 | IO21RSB0 |
| 110 | V _{JTAG} | 146 | IO44NDB1 | 182 | IO20RSB0 |
| 111 | GDA0/IO60VDB1 | 147 | IO44PDB1 | 183 | IO19RSB0 |
| 112 | GDA1/IO60UDB1 | 148 | IO43NDB1 | 184 | IO18RSB0 |
| 113 | GDB0/IO59VDB1 | 149 | GBC2/IO43PDB1 | 185 | IO17RSB0 |
| 114 | GDB1/IO59UDB1 | 150 | IO42NDB1 | 186 | V _{CC} B0 |
| 115 | GDC0/IO58VDB1 | 151 | GBB2/IO42PDB1 | 187 | V _{CC} |
| 116 | GDC1/IO58UDB1 | 152 | IO41NDB1 | 188 | IO16RSB0 |
| 117 | IO57VDB1 | 153 | GBA2/IO41PDB1 | 189 | IO15RSB0 |
| 118 | IO57UDB1 | 154 | VMV1 | 190 | IO14RSB0 |
| 119 | IO56NDB1 | 155 | GNDQ | 191 | IO13RSB0 |
| 120 | IO56PDB1 | 156 | GND | 192 | IO12RSB0 |
| 121 | IO55RSB1 | 157 | NC | 193 | IO11RSB0 |
| 122 | GND | 158 | GBA1/IO40RSB0 | 194 | IO10RSB0 |
| 123 | V _{CC} B1 | 159 | GBA0/IO39RSB0 | 195 | GND |
| 124 | NC | 160 | GBB1/IO38RSB0 | 196 | IO09RSB0 |
| 125 | NC | 161 | GBB0/IO37RSB0 | 197 | IO08RSB0 |
| 126 | V _{CC} | 162 | GND | 198 | IO07RSB0 |
| 127 | IO53NDB1 | 163 | GBC1/IO36RSB0 | 199 | IO06RSB0 |
| 128 | GCC2/IO53PDB1 | 164 | GBC0/IO35RSB0 | 200 | V _{CC} B0 |
| 129 | GCB2/IO52PSB1 | 165 | IO34RSB0 | 201 | GAC1/IO05RSB0 |
| 130 | GND | 166 | IO33RSB0 | 202 | GAC0/IO04RSB0 |
| 131 | GCA2/IO51PSB1 | 167 | IO32RSB0 | 203 | GAB1/IO03RSB0 |
| 132 | GCA1/IO50PDB1 | 168 | IO31RSB0 | 204 | GAB0/IO02RSB0 |
| 133 | GCA0/IO50NDB1 | 169 | IO30RSB0 | 205 | GAA1/IO01RSB0 |
| 134 | GCB0/IO49NDB1 | 170 | V _{CC} B0 | 206 | GAA0/IO00RSB0 |
| 135 | GCB1/IO49PDB1 | 171 | V _{CC} | 207 | GNDQ |
| 136 | GCC0/IO48NDB1 | 172 | IO29RSB0 | 208 | VMV0 |
| 137 | GCC1/IO48PDB1 | 173 | IO28RSB0 | | |
| 138 | IO47NDB1 | 174 | IO27RSB0 | | |
| 139 | IO47PDB1 | 175 | IO26RSB0 | | |
| 140 | V _{CC} B1 | 176 | IO25RSB0 | | |
| 141 | GND | 177 | IO24RSB0 | | |
| 142 | V _{CC} | 178 | GND | | |
| 143 | IO46RSB1 | 179 | IO23RSB0 | | |
| 144 | IO45NDB1 | 180 | IO22RSB0 | | |

| 208-Pin PQFP | |
|--------------|----------------------|
| Pin Number | A3P400 Function |
| 1 | GND |
| 2 | GAA2/IO155UDB3 |
| 3 | IO155VDB3 |
| 4 | GAB2/IO154UDB3 |
| 5 | IO154VDB3 |
| 6 | GAC2/IO153UDB3 |
| 7 | IO153VDB3 |
| 8 | IO152UDB3 |
| 9 | IO152VDB3 |
| 10 | IO151UDB3 |
| 11 | IO151VDB3 |
| 12 | IO150PDB3 |
| 13 | IO150NDB3 |
| 14 | IO149PDB3 |
| 15 | IO149NDB3 |
| 16 | V _{CC} |
| 17 | GND |
| 18 | V _{CC1} B3 |
| 19 | IO148PDB3 |
| 20 | IO148NDB3 |
| 21 | GFC1/IO147PDB3 |
| 22 | GFC0/IO147NDB3 |
| 23 | GFB1/IO146PDB3 |
| 24 | GFB0/IO146NDB3 |
| 25 | V _{CCOMPLF} |
| 26 | GFA0/IO145NPB3 |
| 27 | V _{CCPLF} |
| 28 | GFA1/IO145PPB3 |
| 29 | GND |
| 30 | GFA2/IO144PDB3 |
| 31 | IO144NDB3 |
| 32 | GFB2/IO143PDB3 |
| 33 | IO143NDB3 |
| 34 | GFC2/IO142PDB3 |
| 35 | IO142NDB3 |
| 36 | NC |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P400 Function |
| 37 | IO141PSB3 |
| 38 | IO140PDB3 |
| 39 | IO140NDB3 |
| 40 | V _{CC1} B3 |
| 41 | GND |
| 42 | IO138PDB3 |
| 43 | IO138NDB3 |
| 44 | GEC1/IO137PDB3 |
| 45 | GEC0/IO137NDB3 |
| 46 | GEB1/IO136PDB3 |
| 47 | GEB0/IO136NDB3 |
| 48 | GEA1/IO135PDB3 |
| 49 | GEA0/IO135NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV2 |
| 54 | NC |
| 55 | GEA2/IO134RSB2 |
| 56 | GEB2/IO133RSB2 |
| 57 | GEC2/IO132RSB2 |
| 58 | IO131RSB2 |
| 59 | IO130RSB2 |
| 60 | IO129RSB2 |
| 61 | IO128RSB2 |
| 62 | V _{CC1} B2 |
| 63 | IO125RSB2 |
| 64 | IO123RSB2 |
| 65 | GND |
| 66 | IO121RSB2 |
| 67 | IO119RSB2 |
| 68 | IO117RSB2 |
| 69 | IO115RSB2 |
| 70 | IO113RSB2 |
| 71 | V _{CC} |
| 72 | V _{CC1} B2 |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P400 Function |
| 73 | IO112RSB2 |
| 74 | IO111RSB2 |
| 75 | IO110RSB2 |
| 76 | IO109RSB2 |
| 77 | IO108RSB2 |
| 78 | IO107RSB2 |
| 79 | IO106RSB2 |
| 80 | IO104RSB2 |
| 81 | GND |
| 82 | IO102RSB2 |
| 83 | IO101RSB2 |
| 84 | IO100RSB2 |
| 85 | IO99RSB2 |
| 86 | IO98RSB2 |
| 87 | IO97RSB2 |
| 88 | V _{CC} |
| 89 | V _{CC1} B2 |
| 90 | IO94RSB2 |
| 91 | IO92RSB2 |
| 92 | IO90RSB2 |
| 93 | IO88RSB2 |
| 94 | IO86RSB2 |
| 95 | IO84RSB2 |
| 96 | GDC2/IO82RSB2 |
| 97 | GND |
| 98 | GDB2/IO81RSB2 |
| 99 | GDA2/IO80RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | V _{PUMP} |
| 107 | NC |
| 108 | TDO |

| 208-Pin PQFP | | 208-Pin PQFP | | 208-Pin PQFP | |
|--------------|--------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P400 Function | Pin Number | A3P400 Function | Pin Number | A3P400 Function |
| 109 | TRST | 145 | IO64PDB1 | 181 | IO27RSB0 |
| 110 | V _{JTAG} | 146 | IO63NDB1 | 182 | IO26RSB0 |
| 111 | GDA0/IO79VDB1 | 147 | IO63PDB1 | 183 | IO25RSB0 |
| 112 | GDA1/IO79UDB1 | 148 | IO62NDB1 | 184 | IO24RSB0 |
| 113 | GDB0/IO78VDB1 | 149 | GBC2/IO62PDB1 | 185 | IO23RSB0 |
| 114 | GDB1/IO78UDB1 | 150 | IO61NDB1 | 186 | V _{CC} B0 |
| 115 | GDC0/IO77VDB1 | 151 | GBB2/IO61PDB1 | 187 | V _{CC} |
| 116 | GDC1/IO77UDB1 | 152 | IO60NDB1 | 188 | IO21RSB0 |
| 117 | IO76VDB1 | 153 | GBA2/IO60PDB1 | 189 | IO20RSB0 |
| 118 | IO76UDB1 | 154 | VMV1 | 190 | IO19RSB0 |
| 119 | IO75NDB1 | 155 | GNDQ | 191 | IO18RSB0 |
| 120 | IO75PDB1 | 156 | GND | 192 | IO17RSB0 |
| 121 | IO74RSB1 | 157 | VMV0 | 193 | IO16RSB0 |
| 122 | GND | 158 | GBA1/IO59RSB0 | 194 | IO15RSB0 |
| 123 | V _{CC} B1 | 159 | GBA0/IO58RSB0 | 195 | GND |
| 124 | NC | 160 | GBB1/IO57RSB0 | 196 | IO13RSB0 |
| 125 | NC | 161 | GBB0/IO56RSB0 | 197 | IO11RSB0 |
| 126 | V _{CC} | 162 | GND | 198 | IO09RSB0 |
| 127 | IO72NDB1 | 163 | GBC1/IO55RSB0 | 199 | IO07RSB0 |
| 128 | GCC2/IO72PDB1 | 164 | GBC0/IO54RSB0 | 200 | V _{CC} B0 |
| 129 | GCB2/IO71PSB1 | 165 | IO52RSB0 | 201 | GAC1/IO05RSB0 |
| 130 | GND | 166 | IO49RSB0 | 202 | GAC0/IO04RSB0 |
| 131 | GCA2/IO70PSB1 | 167 | IO46RSB0 | 203 | GAB1/IO03RSB0 |
| 132 | GCA1/IO69PDB1 | 168 | IO43RSB0 | 204 | GAB0/IO02RSB0 |
| 133 | GCA0/IO69NDB1 | 169 | IO40RSB0 | 205 | GAA1/IO01RSB0 |
| 134 | GCB0/IO68NDB1 | 170 | V _{CC} B0 | 206 | GAA0/IO00RSB0 |
| 135 | GCB1/IO68PDB1 | 171 | V _{CC} | 207 | GNDQ |
| 136 | GCC0/IO67NDB1 | 172 | IO36RSB0 | 208 | VMV0 |
| 137 | GCC1/IO67PDB1 | 173 | IO35RSB0 | | |
| 138 | IO66NDB1 | 174 | IO34RSB0 | | |
| 139 | IO66PDB1 | 175 | IO33RSB0 | | |
| 140 | V _{CC} B1 | 176 | IO32RSB0 | | |
| 141 | GND | 177 | IO31RSB0 | | |
| 142 | V _{CC} | 178 | GND | | |
| 143 | IO65RSB1 | 179 | IO29RSB0 | | |
| 144 | IO64NDB1 | 180 | IO28RSB0 | | |

| 208-Pin PQFP | | 208-Pin PQFP | | 208-Pin PQFP | |
|--------------|---------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P600 Function | Pin Number | A3P600 Function | Pin Number | A3P600 Function |
| 1 | GND | 37 | IO152PDB3 | 73 | IO120RSB2 |
| 2 | GAA2/IO174PDB3 | 38 | IO152NDB3 | 74 | IO119RSB2 |
| 3 | IO174NDB3 | 39 | IO150PSB3 | 75 | IO118RSB2 |
| 4 | GAB2/IO173PDB3 | 40 | V _{CC} B3 | 76 | IO117RSB2 |
| 5 | IO173NDB3 | 41 | GND | 77 | IO116RSB2 |
| 6 | GAC2/IO172PDB3 | 42 | IO147PDB3 | 78 | IO115RSB2 |
| 7 | IO172NDB3 | 43 | IO147NDB3 | 79 | IO114RSB2 |
| 8 | IO171PDB3 | 44 | GEC1/IO146PDB3 | 80 | IO112RSB2 |
| 9 | IO171NDB3 | 45 | GEC0/IO146NDB3 | 81 | GND |
| 10 | IO170PDB3 | 46 | GEB1/IO145PDB3 | 82 | IO111RSB2 |
| 11 | IO170NDB3 | 47 | GEB0/IO145NDB3 | 83 | IO110RSB2 |
| 12 | IO169PDB3 | 48 | GEA1/IO144PDB3 | 84 | IO109RSB2 |
| 13 | IO169NDB3 | 49 | GEA0/IO144NDB3 | 85 | IO108RSB2 |
| 14 | IO168PDB3 | 50 | VMV3 | 86 | IO107RSB2 |
| 15 | IO168NDB3 | 51 | GNDQ | 87 | IO106RSB2 |
| 16 | V _{CC} | 52 | GND | 88 | V _{CC} |
| 17 | GND | 53 | VMV2 | 89 | V _{CC} B2 |
| 18 | V _{CC} B3 | 54 | GEA2/IO143RSB2 | 90 | IO104RSB2 |
| 19 | IO166PDB3 | 55 | GEB2/IO142RSB2 | 91 | IO102RSB2 |
| 20 | IO166NDB3 | 56 | GEC2/IO141RSB2 | 92 | IO100RSB2 |
| 21 | GFC1/IO164PDB3 | 57 | IO140RSB2 | 93 | IO98RSB2 |
| 22 | GFC0/IO164NDB3 | 58 | IO139RSB2 | 94 | IO96RSB2 |
| 23 | GFB1/IO163PDB3 | 59 | IO138RSB2 | 95 | IO92RSB2 |
| 24 | GFB0/IO163NDB3 | 60 | IO137RSB2 | 96 | GDC2/IO91RSB2 |
| 25 | V _{COMPLF} | 61 | IO136RSB2 | 97 | GND |
| 26 | GFA0/IO162NPB3 | 62 | V _{CC} B2 | 98 | GDB2/IO90RSB2 |
| 27 | V _{CC} PLF | 63 | IO135RSB2 | 99 | GDA2/IO89RSB2 |
| 28 | GFA1/IO162PPB3 | 64 | IO133RSB2 | 100 | GNDQ |
| 29 | GND | 65 | GND | 101 | TCK |
| 30 | GFA2/IO161PDB3 | 66 | IO131RSB2 | 102 | TDI |
| 31 | IO161NDB3 | 67 | IO129RSB2 | 103 | TMS |
| 32 | GFB2/IO160PDB3 | 68 | IO127RSB2 | 104 | VMV2 |
| 33 | IO160NDB3 | 69 | IO125RSB2 | 105 | GND |
| 34 | GFC2/IO159PDB3 | 70 | IO123RSB2 | 106 | V _{PUMP} |
| 35 | IO159NDB3 | 71 | V _{CC} | 107 | GNDQ |
| 36 | V _{CC} | 72 | V _{CC} B2 | 108 | TDO |

| 208-Pin PQFP | | 208-Pin PQFP | | 208-Pin PQFP | |
|--------------|---------------------|--------------|---------------------|--------------|---------------------|
| Pin Number | A3P600 Function | Pin Number | A3P600 Function | Pin Number | A3P600 Function |
| 109 | TRST | 145 | IO64PDB1 | 181 | IO27RSB0 |
| 110 | V _{JTAG} | 146 | IO63NDB1 | 182 | IO26RSB0 |
| 111 | GDA0/IO88NDB1 | 147 | IO63PDB1 | 183 | IO25RSB0 |
| 112 | GDA1/IO88PDB1 | 148 | IO62NDB1 | 184 | IO24RSB0 |
| 113 | GDB0/IO87NDB1 | 149 | GBC2/IO62PDB1 | 185 | IO23RSB0 |
| 114 | GDB1/IO87PDB1 | 150 | IO61NDB1 | 186 | V _{CCi} B0 |
| 115 | GDC0/IO86NDB1 | 151 | GBB2/IO61PDB1 | 187 | V _{CC} |
| 116 | GDC1/IO86PDB1 | 152 | IO60NDB1 | 188 | IO20RSB0 |
| 117 | IO84NDB1 | 153 | GBA2/IO60PDB1 | 189 | IO19RSB0 |
| 118 | IO84PDB1 | 154 | VMV1 | 190 | IO18RSB0 |
| 119 | IO82NDB1 | 155 | GNDQ | 191 | IO17RSB0 |
| 120 | IO82PDB1 | 156 | GND | 192 | IO16RSB0 |
| 121 | IO81PSB1 | 157 | VMV0 | 193 | IO14RSB0 |
| 122 | GND | 158 | GBA1/IO59RSB0 | 194 | IO12RSB0 |
| 123 | V _{CCi} B1 | 159 | GBA0/IO58RSB0 | 195 | GND |
| 124 | IO77NDB1 | 160 | GBB1/IO57RSB0 | 196 | IO10RSB0 |
| 125 | IO77PDB1 | 161 | GBB0/IO56RSB0 | 197 | IO09RSB0 |
| 126 | NC | 162 | GND | 198 | IO08RSB0 |
| 127 | IO74NDB1 | 163 | GBC1/IO55RSB0 | 199 | IO07RSB0 |
| 128 | GCC2/IO74PDB1 | 164 | GBC0/IO54RSB0 | 200 | V _{CCi} B0 |
| 129 | GCB2/IO73PSB1 | 165 | IO52RSB0 | 201 | GAC1/IO05RSB0 |
| 130 | GND | 166 | IO50RSB0 | 202 | GAC0/IO04RSB0 |
| 131 | GCA2/IO72PSB1 | 167 | IO48RSB0 | 203 | GAB1/IO03RSB0 |
| 132 | GCA1/IO71PDB1 | 168 | IO46RSB0 | 204 | GAB0/IO02RSB0 |
| 133 | GCA0/IO71NDB1 | 169 | IO44RSB0 | 205 | GAA1/IO01RSB0 |
| 134 | GCB0/IO70NDB1 | 170 | V _{CCi} B0 | 206 | GAA0/IO00RSB0 |
| 135 | GCB1/IO70PDB1 | 171 | V _{CC} | 207 | GNDQ |
| 136 | GCC0/IO69NDB1 | 172 | IO36RSB0 | 208 | VMV0 |
| 137 | GCC1/IO69PDB1 | 173 | IO35RSB0 | | |
| 138 | IO67NDB1 | 174 | IO34RSB0 | | |
| 139 | IO67PDB1 | 175 | IO33RSB0 | | |
| 140 | V _{CCi} B1 | 176 | IO32RSB0 | | |
| 141 | GND | 177 | IO31RSB0 | | |
| 142 | V _{CC} | 178 | GND | | |
| 143 | IO65PSB1 | 179 | IO29RSB0 | | |
| 144 | IO64NDB1 | 180 | IO28RSB0 | | |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| 1 | GND |
| 2 | GAA2/IO225PDB3 |
| 3 | IO225NDB3 |
| 4 | GAB2/IO224PDB3 |
| 5 | IO224NDB3 |
| 6 | GAC2/IO223PDB3 |
| 7 | IO223NDB3 |
| 8 | IO222PDB3 |
| 9 | IO222NDB3 |
| 10 | IO220PDB3 |
| 11 | IO220NDB3 |
| 12 | IO218PDB3 |
| 13 | IO218NDB3 |
| 14 | IO216PDB3 |
| 15 | IO216NDB3 |
| 16 | V _{CC} |
| 17 | GND |
| 18 | V _{CCI} B3 |
| 19 | IO212PDB3 |
| 20 | IO212NDB3 |
| 21 | GFC1/IO209PDB3 |
| 22 | GFC0/IO209NDB3 |
| 23 | GFB1/IO208PDB3 |
| 24 | GFB0/IO208NDB3 |
| 25 | V _{COMPLF} |
| 26 | GFA0/IO207NPB3 |
| 27 | V _{CCPLF} |
| 28 | GFA1/IO207PPB3 |
| 29 | GND |
| 30 | GFA2/IO206PDB3 |
| 31 | IO206NDB3 |
| 32 | GFB2/IO205PDB3 |
| 33 | IO205NDB3 |
| 34 | GFC2/IO204PDB3 |
| 35 | IO204NDB3 |
| 36 | V _{CC} |

| 208-Pin PQFP | |
|--------------|--------------------|
| Pin Number | A3P1000 Function |
| 37 | IO199PDB3 |
| 38 | IO199NDB3 |
| 39 | IO197PSB3 |
| 40 | V _{CC} B3 |
| 41 | GND |
| 42 | IO191PDB3 |
| 43 | IO191NDB3 |
| 44 | GEC1/IO190PDB3 |
| 45 | GEC0/IO190NDB3 |
| 46 | GEB1/IO189PDB3 |
| 47 | GEB0/IO189NDB3 |
| 48 | GEA1/IO188PDB3 |
| 49 | GEA0/IO188NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV2 |
| 54 | GEA2/IO187RSB2 |
| 55 | GEB2/IO186RSB2 |
| 56 | GEC2/IO185RSB2 |
| 57 | IO184RSB2 |
| 58 | IO183RSB2 |
| 59 | IO182RSB2 |
| 60 | IO181RSB2 |
| 61 | IO180RSB2 |
| 62 | V _{CC} B2 |
| 63 | IO178RSB2 |
| 64 | IO176RSB2 |
| 65 | GND |
| 66 | IO174RSB2 |
| 67 | IO172RSB2 |
| 68 | IO170RSB2 |
| 69 | IO168RSB2 |
| 70 | IO166RSB2 |
| 71 | V _{CC} |
| 72 | V _{CC} B2 |

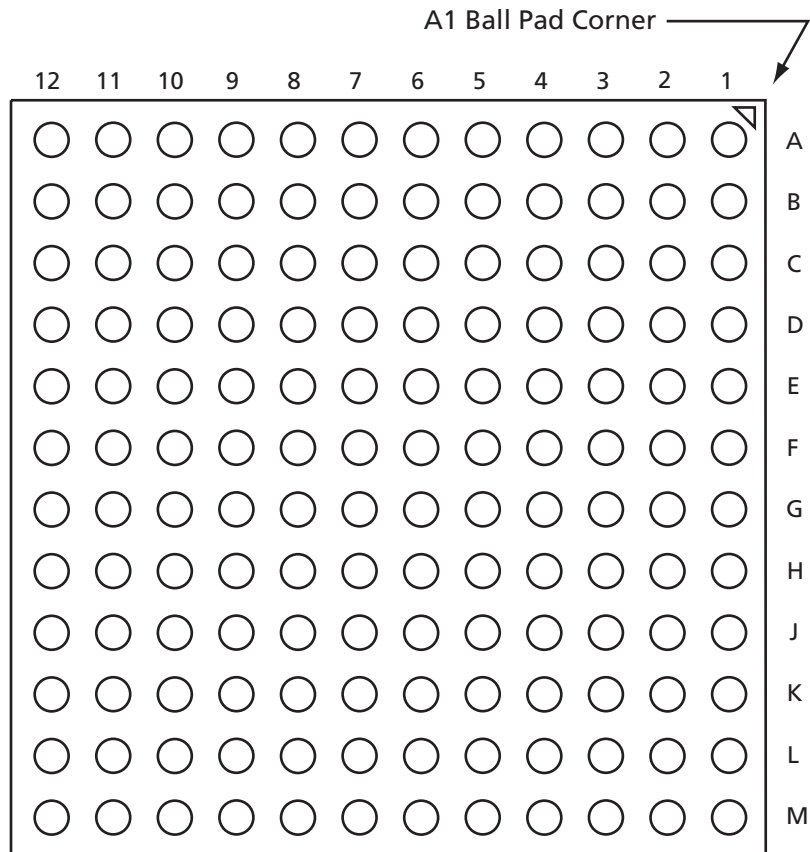
| 208-Pin PQFP | |
|--------------|--------------------|
| Pin Number | A3P1000 Function |
| 73 | IO162RSB2 |
| 74 | IO160RSB2 |
| 75 | IO158RSB2 |
| 76 | IO156RSB2 |
| 77 | IO154RSB2 |
| 78 | IO152RSB2 |
| 79 | IO150RSB2 |
| 80 | IO148RSB2 |
| 81 | GND |
| 82 | IO143RSB2 |
| 83 | IO141RSB2 |
| 84 | IO139RSB2 |
| 85 | IO137RSB2 |
| 86 | IO135RSB2 |
| 87 | IO133RSB2 |
| 88 | V _{CC} |
| 89 | V _{CC} B2 |
| 90 | IO128RSB2 |
| 91 | IO126RSB2 |
| 92 | IO124RSB2 |
| 93 | IO122RSB2 |
| 94 | IO120RSB2 |
| 95 | IO118RSB2 |
| 96 | GDC2/IO116RSB2 |
| 97 | GND |
| 98 | GDB2/IO115RSB2 |
| 99 | GDA2/IO114RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | V _{PUMP} |
| 107 | GNDQ |
| 108 | TDO |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| 109 | TRST |
| 110 | V _{JTAG} |
| 111 | GDA0/IO113NDB1 |
| 112 | GDA1/IO113PDB1 |
| 113 | GDB0/IO112NDB1 |
| 114 | GDB1/IO112PDB1 |
| 115 | GDC0/IO111NDB1 |
| 116 | GDC1/IO111PDB1 |
| 117 | IO109NDB1 |
| 118 | IO109PDB1 |
| 119 | IO106NDB1 |
| 120 | IO106PDB1 |
| 121 | IO104PSB1 |
| 122 | GND |
| 123 | V _{CC1} B1 |
| 124 | IO99NDB1 |
| 125 | IO99PDB1 |
| 126 | NC |
| 127 | IO96NDB1 |
| 128 | GCC2/IO96PDB1 |
| 129 | GCB2/IO95PSB1 |
| 130 | GND |
| 131 | GCA2/IO94PSB1 |
| 132 | GCA1/IO93PDB1 |
| 133 | GCA0/IO93NDB1 |
| 134 | GCB0/IO92NDB1 |
| 135 | GCB1/IO92PDB1 |
| 136 | GCC0/IO91NDB1 |
| 137 | GCC1/IO91PDB1 |
| 138 | IO88NDB1 |
| 139 | IO88PDB1 |
| 140 | V _{CC1} B1 |
| 141 | GND |
| 142 | V _{CC} |
| 143 | IO86PSB1 |
| 144 | IO84NDB1 |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| 145 | IO84PDB1 |
| 146 | IO82NDB1 |
| 147 | IO82PDB1 |
| 148 | IO80NDB1 |
| 149 | GBC2/IO80PDB1 |
| 150 | IO79NDB1 |
| 151 | GBB2/IO79PDB1 |
| 152 | IO78NDB1 |
| 153 | GBA2/IO78PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO77RSB0 |
| 159 | GBA0/IO76RSB0 |
| 160 | GBB1/IO75RSB0 |
| 161 | GBB0/IO74RSB0 |
| 162 | GND |
| 163 | GBC1/IO73RSB0 |
| 164 | GBC0/IO72RSB0 |
| 165 | IO70RSB0 |
| 166 | IO67RSB0 |
| 167 | IO63RSB0 |
| 168 | IO60RSB0 |
| 169 | IO57RSB0 |
| 170 | V _{CC1} B0 |
| 171 | V _{CC} |
| 172 | IO54RSB0 |
| 173 | IO51RSB0 |
| 174 | IO48RSB0 |
| 175 | IO45RSB0 |
| 176 | IO42RSB0 |
| 177 | IO40RSB0 |
| 178 | GND |
| 179 | IO38RSB0 |
| 180 | IO35RSB0 |

| 208-Pin PQFP | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| 181 | IO33RSB0 |
| 182 | IO31RSB0 |
| 183 | IO29RSB0 |
| 184 | IO27RSB0 |
| 185 | IO25RSB0 |
| 186 | V _{CC1} B0 |
| 187 | V _{CC} |
| 188 | IO22RSB0 |
| 189 | IO20RSB0 |
| 190 | IO18RSB0 |
| 191 | IO16RSB0 |
| 192 | IO15RSB0 |
| 193 | IO14RSB0 |
| 194 | IO13RSB0 |
| 195 | GND |
| 196 | IO12RSB0 |
| 197 | IO11RSB0 |
| 198 | IO10RSB0 |
| 199 | IO09RSB0 |
| 200 | V _{CC1} B0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

144-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-7 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 144-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P060 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO04RSB0 |
| A4 | GAB1/IO05RSB0 |
| A5 | IO08RSB0 |
| A6 | GND |
| A7 | IO11RSB0 |
| A8 | V _{CC} |
| A9 | IO16RSB0 |
| A10 | GBA0/IO23RSB0 |
| A11 | GBA1/IO24RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO53RSB1 |
| B2 | GND |
| B3 | GAA0/IO02RSB0 |
| B4 | GAA1/IO03RSB0 |
| B5 | IO00RSB0 |
| B6 | IO10RSB0 |
| B7 | IO12RSB0 |
| B8 | IO14RSB0 |
| B9 | GBB0/IO21RSB0 |
| B10 | GBB1/IO22RSB0 |
| B11 | GND |
| B12 | VMV0 |
| C1 | IO95RSB1 |
| C2 | GFA2/IO83RSB1 |
| C3 | GAC2/IO94RSB1 |
| C4 | V _{CC} |
| C5 | IO01RSB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO17RSB0 |
| C10 | GBA2/IO25RSB0 |
| C11 | IO26RSB0 |
| C12 | GBC2/IO29RSB0 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P060 Function |
| D1 | IO91RSB1 |
| D2 | IO92RSB1 |
| D3 | IO93RSB1 |
| D4 | GAA2/IO51RSB1 |
| D5 | GAC0/IO06RSB0 |
| D6 | GAC1/IO07RSB0 |
| D7 | GBC0/IO19RSB0 |
| D8 | GBC1/IO20RSB0 |
| D9 | GBB2/IO27RSB0 |
| D10 | IO18RSB0 |
| D11 | IO28RSB0 |
| D12 | GCB1/IO37RSB0 |
| E1 | V _{CC} |
| E2 | GFC0/IO88RSB1 |
| E3 | GFC1/IO89RSB1 |
| E4 | V _{CC} B1 |
| E5 | IO52RSB1 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | GCC1/IO35RSB0 |
| E9 | V _{CC} B0 |
| E10 | V _{CC} |
| E11 | GCA0/IO40RSB0 |
| E12 | IO30RSB0 |
| F1 | GFB0/IO86RSB1 |
| F2 | V _{COMPLF} |
| F3 | GFB1/IO87RSB1 |
| F4 | IO90RSB1 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO36RSB0 |
| F9 | GCB0/IO38RSB0 |
| F10 | GND |
| F11 | GCA1/IO39RSB0 |
| F12 | GCA2/IO41RSB0 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P060 Function |
| G1 | GFA1/IO84RSB1 |
| G2 | GND |
| G3 | V _{CC} PLF |
| G4 | GFA0/IO85RSB1 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO45RSB0 |
| G9 | IO32RSB0 |
| G10 | GCC2/IO43RSB0 |
| G11 | IO31RSB0 |
| G12 | GCB2/IO42RSB0 |
| H1 | V _{CC} |
| H2 | GFB2/IO82RSB1 |
| H3 | GFC2/IO81RSB1 |
| H4 | GEC1/IO77RSB1 |
| H5 | V _{CC} |
| H6 | IO34RSB0 |
| H7 | IO44RSB0 |
| H8 | GDB2/IO55RSB1 |
| H9 | GDC0/IO46RSB0 |
| H10 | V _{CC} B0 |
| H11 | IO33RSB0 |
| H12 | V _{CC} |
| J1 | GEB1/IO75RSB1 |
| J2 | IO78RSB1 |
| J3 | V _{CC} B1 |
| J4 | GEC0/IO76RSB1 |
| J5 | IO79RSB1 |
| J6 | IO80RSB1 |
| J7 | V _{CC} |
| J8 | TCK |
| J9 | GDA2/IO54RSB1 |
| J10 | TDO |
| J11 | GDA1/IO49RSB0 |
| J12 | GDB1/IO47RSB0 |

| 144-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P060 Function |
| K1 | GEB0/IO74RSB1 |
| K2 | GEA1/IO73RSB1 |
| K3 | GEA0/IO72RSB1 |
| K4 | GEA2/IO71RSB1 |
| K5 | IO65RSB1 |
| K6 | IO64RSB1 |
| K7 | GND |
| K8 | IO57RSB1 |
| K9 | GDC2/IO56RSB1 |
| K10 | GND |
| K11 | GDA0/IO50RSB0 |
| K12 | GDB0/IO48RSB0 |
| L1 | GND |
| L2 | VMV1 |
| L3 | GEB2/IO70RSB1 |
| L4 | IO67RSB1 |
| L5 | V _{CC} B1 |
| L6 | IO62RSB1 |
| L7 | IO59RSB1 |
| L8 | IO58RSB1 |
| L9 | TMS |
| L10 | V _{JTAG} |
| L11 | VMV1 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO69RSB1 |
| M3 | IO68RSB1 |
| M4 | IO66RSB1 |
| M5 | IO63RSB1 |
| M6 | IO61RSB1 |
| M7 | IO60RSB1 |
| M8 | NC |
| M9 | TDI |
| M10 | V _{CC} B1 |
| M11 | V _{PUMP} |
| M12 | GNDQ |

| 144-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P125 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO11RSB0 |
| A6 | GND |
| A7 | IO18RSB0 |
| A8 | V _{CC} |
| A9 | IO25RSB0 |
| A10 | GBA0/IO39RSB0 |
| A11 | GBA1/IO40RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO69RSB1 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO08RSB0 |
| B6 | IO14RSB0 |
| B7 | IO19RSB0 |
| B8 | IO22RSB0 |
| B9 | GBB0/IO37RSB0 |
| B10 | GBB1/IO38RSB0 |
| B11 | GND |
| B12 | VMV0 |
| C1 | IO132RSB1 |
| C2 | GFA2/IO120RSB1 |
| C3 | GAC2/IO131RSB1 |
| C4 | V _{CC} |
| C5 | IO10RSB0 |
| C6 | IO12RSB0 |
| C7 | IO21RSB0 |
| C8 | IO24RSB0 |
| C9 | IO27RSB0 |
| C10 | GBA2/IO41RSB0 |
| C11 | IO42RSB0 |
| C12 | GBC2/IO45RSB0 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| D1 | IO128RSB1 |
| D2 | IO129RSB1 |
| D3 | IO130RSB1 |
| D4 | GAA2/IO67RSB1 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO35RSB0 |
| D8 | GBC1/IO36RSB0 |
| D9 | GBB2/IO43RSB0 |
| D10 | IO28RSB0 |
| D11 | IO44RSB0 |
| D12 | GCB1/IO53RSB0 |
| E1 | V _{CC} |
| E2 | GFC0/IO125RSB1 |
| E3 | GFC1/IO126RSB1 |
| E4 | V _{CC} B1 |
| E5 | IO68RSB1 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | GCC1/IO51RSB0 |
| E9 | V _{CC} B0 |
| E10 | V _{CC} |
| E11 | GCA0/IO56RSB0 |
| E12 | IO46RSB0 |
| F1 | GFB0/IO123RSB1 |
| F2 | V _{COMPLF} |
| F3 | GFB1/IO124RSB1 |
| F4 | IO127RSB1 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO52RSB0 |
| F9 | GCB0/IO54RSB0 |
| F10 | GND |
| F11 | GCA1/IO55RSB0 |
| F12 | GCA2/IO57RSB0 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| G1 | GFA1/IO121RSB1 |
| G2 | GND |
| G3 | V _{CC} PLF |
| G4 | GFA0/IO122RSB1 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO61RSB0 |
| G9 | IO48RSB0 |
| G10 | GCC2/IO59RSB0 |
| G11 | IO47RSB0 |
| G12 | GCB2/IO58RSB0 |
| H1 | V _{CC} |
| H2 | GFB2/IO119RSB1 |
| H3 | GFC2/IO118RSB1 |
| H4 | GEC1/IO112RSB1 |
| H5 | V _{CC} |
| H6 | IO50RSB0 |
| H7 | IO60RSB0 |
| H8 | GDB2/IO71RSB1 |
| H9 | GDC0/IO62RSB0 |
| H10 | V _{CC} B0 |
| H11 | IO49RSB0 |
| H12 | V _{CC} |
| J1 | GEB1/IO110RSB1 |
| J2 | IO115RSB1 |
| J3 | V _{CC} B1 |
| J4 | GEC0/IO111RSB1 |
| J5 | IO116RSB1 |
| J6 | IO117RSB1 |
| J7 | V _{CC} |
| J8 | TCK |
| J9 | GDA2/IO70RSB1 |
| J10 | TDO |
| J11 | GDA1/IO65RSB0 |
| J12 | GDB1/IO63RSB0 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P125 Function |
| K1 | GEB0/IO109RSB1 |
| K2 | GEA1/IO108RSB1 |
| K3 | GEA0/IO107RSB1 |
| K4 | GEA2/IO106RSB1 |
| K5 | IO100RSB1 |
| K6 | IO98RSB1 |
| K7 | GND |
| K8 | IO73RSB1 |
| K9 | GDC2/IO72RSB1 |
| K10 | GND |
| K11 | GDA0/IO66RSB0 |
| K12 | GDB0/IO64RSB0 |
| L1 | GND |
| L2 | VMV1 |
| L3 | GEB2/IO105RSB1 |
| L4 | IO102RSB1 |
| L5 | V _{CCI} B1 |
| L6 | IO95RSB1 |
| L7 | IO85RSB1 |
| L8 | IO74RSB1 |
| L9 | TMS |
| L10 | V _{JTAG} |
| L11 | VMV1 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO104RSB1 |
| M3 | IO103RSB1 |
| M4 | IO101RSB1 |
| M5 | IO97RSB1 |
| M6 | IO94RSB1 |
| M7 | IO86RSB1 |
| M8 | IO75RSB1 |
| M9 | TDI |
| M10 | V _{CCI} B1 |
| M11 | V _{PUMP} |
| M12 | GNDQ |

| 144-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P250 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO16RSB0 |
| A6 | GND |
| A7 | IO29RSB0 |
| A8 | V _{CC} |
| A9 | IO33RSB0 |
| A10 | GBA0/IO39RSB0 |
| A11 | GBA1/IO40RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO117UDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO14RSB0 |
| B6 | IO19RSB0 |
| B7 | IO22RSB0 |
| B8 | IO30RSB0 |
| B9 | GBB0/IO37RSB0 |
| B10 | GBB1/IO38RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO117VDB3 |
| C2 | GFA2/IO107PPB3 |
| C3 | GAC2/IO116UDB3 |
| C4 | V _{CC} |
| C5 | IO12RSB0 |
| C6 | IO17RSB0 |
| C7 | IO24RSB0 |
| C8 | IO31RSB0 |
| C9 | IO34RSB0 |
| C10 | GBA2/IO41PDB1 |
| C11 | IO41NDB1 |
| C12 | GBC2/IO43PPB1 |

| 144-Pin FBGA | |
|--------------|------------------------|
| Pin Number | A3P250 Function |
| D1 | IO112NDB3 |
| D2 | IO112PDB3 |
| D3 | IO116VDB3 |
| D4 | GAA2/IO118UPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO35RSB0 |
| D8 | GBC1/IO36RSB0 |
| D9 | GBB2/IO42PDB1 |
| D10 | IO42NDB1 |
| D11 | IO43NPB1 |
| D12 | GCB1/IO49PPB1 |
| E1 | V _{CC} |
| E2 | GFC0/IO110NDB3 |
| E3 | GFC1/IO110PDB3 |
| E4 | V _{CC} B3 |
| E5 | IO118VPB3 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | GCC1/IO48PDB1 |
| E9 | V _{CC} B1 |
| E10 | V _{CC} |
| E11 | GCA0/IO50NDB1 |
| E12 | IO51NDB1 |
| F1 | GFB0/IO109NPB3 |
| F2 | V _{CC} COMPLF |
| F3 | GFB1/IO109PPB3 |
| F4 | IO107NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO48NDB1 |
| F9 | GCB0/IO49NPB1 |
| F10 | GND |
| F11 | GCA1/IO50PDB1 |
| F12 | GCA2/IO51PDB1 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P250 Function |
| G1 | GFA1/IO108PPB3 |
| G2 | GND |
| G3 | V _{CC} PLF |
| G4 | GFA0/IO108NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO58UPB1 |
| G9 | IO53NDB1 |
| G10 | GCC2/IO53PDB1 |
| G11 | IO52NDB1 |
| G12 | GCB2/IO52PDB1 |
| H1 | V _{CC} |
| H2 | GFB2/IO106PDB3 |
| H3 | GFC2/IO105PSB3 |
| H4 | GEC1/IO100PDB3 |
| H5 | V _{CC} |
| H6 | IO79RSB2 |
| H7 | IO65RSB2 |
| H8 | GDB2/IO62RSB2 |
| H9 | GDC0/IO58VPB1 |
| H10 | V _{CC} B1 |
| H11 | IO54PSB1 |
| H12 | V _{CC} |
| J1 | GEB1/IO99PDB3 |
| J2 | IO106NDB3 |
| J3 | V _{CC} B3 |
| J4 | GEC0/IO100NDB3 |
| J5 | IO88RSB2 |
| J6 | IO81RSB2 |
| J7 | V _{CC} |
| J8 | TCK |
| J9 | GDA2/IO61RSB2 |
| J10 | TDO |
| J11 | GDA1/IO60UDB1 |
| J12 | GDB1/IO59UDB1 |

| 144-Pin FBGA | |
|--------------|----------------------|
| Pin Number | A3P250 Function |
| K1 | GEB0/IO99NDB3 |
| K2 | GEA1/IO98PDB3 |
| K3 | GEA0/IO98NDB3 |
| K4 | GEA2/IO97RSB2 |
| K5 | IO90RSB2 |
| K6 | IO84RSB2 |
| K7 | GND |
| K8 | IO66RSB2 |
| K9 | GDC2/IO63RSB2 |
| K10 | GND |
| K11 | GDA0/IO60VDB1 |
| K12 | GDB0/IO59VDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO96RSB2 |
| L4 | IO91RSB2 |
| L5 | V _{CC} I B2 |
| L6 | IO82RSB2 |
| L7 | IO80RSB2 |
| L8 | IO72RSB2 |
| L9 | TMS |
| L10 | V _{JTAG} |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO95RSB2 |
| M3 | IO92RSB2 |
| M4 | IO89RSB2 |
| M5 | IO87RSB2 |
| M6 | IO85RSB2 |
| M7 | IO78RSB2 |
| M8 | IO76RSB2 |
| M9 | TDI |
| M10 | V _{CC} I B2 |
| M11 | V _{PUMP} |
| M12 | GNDQ |

| 144-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P400 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO16RSB0 |
| A6 | GND |
| A7 | IO30RSB0 |
| A8 | V _{CC} |
| A9 | IO34RSB0 |
| A10 | GBA0/IO58RSB0 |
| A11 | GBA1/IO59RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO154UDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO14RSB0 |
| B6 | IO19RSB0 |
| B7 | IO23RSB0 |
| B8 | IO31RSB0 |
| B9 | GBB0/IO56RSB0 |
| B10 | GBB1/IO57RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO154VDB3 |
| C2 | GFA2/IO144PPB3 |
| C3 | GAC2/IO153UDB3 |
| C4 | V _{CC} |
| C5 | IO12RSB0 |
| C6 | IO17RSB0 |
| C7 | IO25RSB0 |
| C8 | IO32RSB0 |
| C9 | IO53RSB0 |
| C10 | GBA2/IO60PDB1 |
| C11 | IO60NDB1 |
| C12 | GBC2/IO62PPB1 |

| 144-Pin FBGA | |
|--------------|-----------------------|
| Pin Number | A3P400 Function |
| D1 | IO149NDB3 |
| D2 | IO149PDB3 |
| D3 | IO153VDB3 |
| D4 | GAA2/IO155UPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO54RSB0 |
| D8 | GBC1/IO55RSB0 |
| D9 | GBB2/IO61PDB1 |
| D10 | IO61NDB1 |
| D11 | IO62NPB1 |
| D12 | GCB1/IO68PPB1 |
| E1 | V _{CC} |
| E2 | GFC0/IO147NDB3 |
| E3 | GFC1/IO147PDB3 |
| E4 | V _{CC} B3 |
| E5 | IO155VPB3 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | GCC1/IO67PDB1 |
| E9 | V _{CC} B1 |
| E10 | V _{CC} |
| E11 | GCA0/IO69NDB1 |
| E12 | IO70NDB1 |
| F1 | GFB0/IO146NPB3 |
| F2 | V _{CC} OMPLF |
| F3 | GFB1/IO146PPB3 |
| F4 | IO144NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO67NDB1 |
| F9 | GCB0/IO68NPB1 |
| F10 | GND |
| F11 | GCA1/IO69PDB1 |
| F12 | GCA2/IO70PDB1 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P400 Function |
| G1 | GFA1/IO145PPB3 |
| G2 | GND |
| G3 | V _{CC} PLF |
| G4 | GFA0/IO145NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO77UPB1 |
| G9 | IO72NDB1 |
| G10 | GCC2/IO72PDB1 |
| G11 | IO71NDB1 |
| G12 | GCB2/IO71PDB1 |
| H1 | V _{CC} |
| H2 | GFB2/IO143PDB3 |
| H3 | GFC2/IO142PSB3 |
| H4 | GEC1/IO137PDB3 |
| H5 | V _{CC} |
| H6 | IO75PDB1 |
| H7 | IO75NDB1 |
| H8 | GDB2/IO81RSB2 |
| H9 | GDC0/IO77VPB1 |
| H10 | V _{CC} B1 |
| H11 | IO73PSB1 |
| H12 | V _{CC} |
| J1 | GEB1/IO136PDB3 |
| J2 | IO143NDB3 |
| J3 | V _{CC} B3 |
| J4 | GEC0/IO137NDB3 |
| J5 | IO125RSB2 |
| J6 | IO116RSB2 |
| J7 | V _{CC} |
| J8 | TCK |
| J9 | GDA2/IO80RSB2 |
| J10 | TDO |
| J11 | GDA1/IO79UDB1 |
| J12 | GDB1/IO78UDB1 |

| 144-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| K1 | GEB0/IO136NDB3 |
| K2 | GEA1/IO135PDB3 |
| K3 | GEA0/IO135NDB3 |
| K4 | GEA2/IO134RSB2 |
| K5 | IO127RSB2 |
| K6 | IO121RSB2 |
| K7 | GND |
| K8 | IO104RSB2 |
| K9 | GDC2/IO82RSB2 |
| K10 | GND |
| K11 | GDA0/IO79VDB1 |
| K12 | GDB0/IO78VDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO133RSB2 |
| L4 | IO128RSB2 |
| L5 | V _{CC} B2 |
| L6 | IO119RSB2 |
| L7 | IO114RSB2 |
| L8 | IO110RSB2 |
| L9 | TMS |
| L10 | V _{JTAG} |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO132RSB2 |
| M3 | IO129RSB2 |
| M4 | IO126RSB2 |
| M5 | IO124RSB2 |
| M6 | IO122RSB2 |
| M7 | IO117RSB2 |
| M8 | IO115RSB2 |
| M9 | TDI |
| M10 | V _{CC} B2 |
| M11 | V _{PUMP} |
| M12 | GNDQ |

| 144-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P600 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO10RSB0 |
| A6 | GND |
| A7 | IO34RSB0 |
| A8 | V _{CC} |
| A9 | IO50RSB0 |
| A10 | GBA0/IO58RSB0 |
| A11 | GBA1/IO59RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO173PDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO13RSB0 |
| B6 | IO19RSB0 |
| B7 | IO31RSB0 |
| B8 | IO39RSB0 |
| B9 | GBB0/IO56RSB0 |
| B10 | GBB1/IO57RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO173NDB3 |
| C2 | GFA2/IO161PPB3 |
| C3 | GAC2/IO172PDB3 |
| C4 | V _{CC} |
| C5 | IO16RSB0 |
| C6 | IO25RSB0 |
| C7 | IO28RSB0 |
| C8 | IO42RSB0 |
| C9 | IO45RSB0 |
| C10 | GBA2/IO60PDB1 |
| C11 | IO60NDB1 |
| C12 | GBC2/IO62PPB1 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P600 Function |
| D1 | IO169PDB3 |
| D2 | IO169NDB3 |
| D3 | IO172NDB3 |
| D4 | GAA2/IO174PPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO54RSB0 |
| D8 | GBC1/IO55RSB0 |
| D9 | GBB2/IO61PDB1 |
| D10 | IO61NDB1 |
| D11 | IO62NPB1 |
| D12 | GCB1/IO70PPB1 |
| E1 | V _{CC} |
| E2 | GFC0/IO164NDB3 |
| E3 | GFC1/IO164PDB3 |
| E4 | V _{CC} B3 |
| E5 | IO174NPB3 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | GCC1/IO69PDB1 |
| E9 | V _{CC} B1 |
| E10 | V _{CC} |
| E11 | GCA0/IO71NDB1 |
| E12 | IO72NDB1 |
| F1 | GFB0/IO163NPB3 |
| F2 | V _{COMPLF} |
| F3 | GFB1/IO163PPB3 |
| F4 | IO161NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO69NDB1 |
| F9 | GCB0/IO70NPB1 |
| F10 | GND |
| F11 | GCA1/IO71PDB1 |
| F12 | GCA2/IO72PDB1 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P600 Function |
| G1 | GFA1/IO162PPB3 |
| G2 | GND |
| G3 | V _{CC} PLF |
| G4 | GFA0/IO162NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO86PPB1 |
| G9 | IO74NDB1 |
| G10 | GCC2/IO74PDB1 |
| G11 | IO73NDB1 |
| G12 | GCB2/IO73PDB1 |
| H1 | V _{CC} |
| H2 | GFB2/IO160PDB3 |
| H3 | GFC2/IO159PSB3 |
| H4 | GEC1/IO146PDB3 |
| H5 | V _{CC} |
| H6 | IO80PDB1 |
| H7 | IO80NDB1 |
| H8 | GDB2/IO90RSB2 |
| H9 | GDC0/IO86NPB1 |
| H10 | V _{CC} B1 |
| H11 | IO84PSB1 |
| H12 | V _{CC} |
| J1 | GEB1/IO145PDB3 |
| J2 | IO160NDB3 |
| J3 | V _{CC} B3 |
| J4 | GEC0/IO146NDB3 |
| J5 | IO129RSB2 |
| J6 | IO131RSB2 |
| J7 | V _{CC} |
| J8 | TCK |
| J9 | GDA2/IO89RSB2 |
| J10 | TDO |
| J11 | GDA1/IO88PDB1 |
| J12 | GDB1/IO87PDB1 |

| 144-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P600 Function |
| K1 | GEB0/IO145NDB3 |
| K2 | GEA1/IO144PDB3 |
| K3 | GEA0/IO144NDB3 |
| K4 | GEA2/IO143RSB2 |
| K5 | IO119RSB2 |
| K6 | IO111RSB2 |
| K7 | GND |
| K8 | IO94RSB2 |
| K9 | GDC2/IO91RSB2 |
| K10 | GND |
| K11 | GDA0/IO88NDB1 |
| K12 | GDB0/IO87NDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO142RSB2 |
| L4 | IO136RSB2 |
| L5 | V _{CC} B2 |
| L6 | IO115RSB2 |
| L7 | IO103RSB2 |
| L8 | IO97RSB2 |
| L9 | TMS |
| L10 | V _{JTAG} |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO141RSB2 |
| M3 | IO138RSB2 |
| M4 | IO123RSB2 |
| M5 | IO126RSB2 |
| M6 | IO134RSB2 |
| M7 | IO108RSB2 |
| M8 | IO99RSB2 |
| M9 | TDI |
| M10 | V _{CC} B2 |
| M11 | V _{PUMP} |
| M12 | GNDQ |

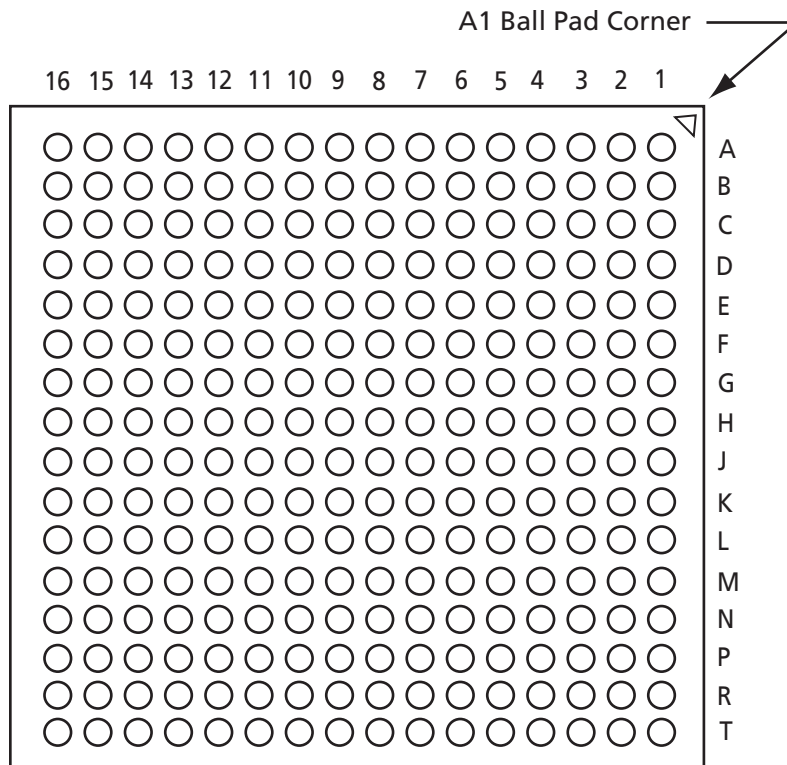
| 144-Pin FBGA | |
|--------------|------------------|
| Pin Number | A3P1000 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO10RSB0 |
| A6 | GND |
| A7 | IO44RSB0 |
| A8 | V _{CC} |
| A9 | IO69RSB0 |
| A10 | GBA0/IO76RSB0 |
| A11 | GBA1/IO77RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO224PDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO13RSB0 |
| B6 | IO26RSB0 |
| B7 | IO35RSB0 |
| B8 | IO60RSB0 |
| B9 | GBB0/IO74RSB0 |
| B10 | GBB1/IO75RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO224NDB3 |
| C2 | GFA2/IO206PPB3 |
| C3 | GAC2/IO223PDB3 |
| C4 | V _{CC} |
| C5 | IO16RSB0 |
| C6 | IO29RSB0 |
| C7 | IO32RSB0 |
| C8 | IO63RSB0 |
| C9 | IO66RSB0 |
| C10 | GBA2/IO78PDB1 |
| C11 | IO78NDB1 |
| C12 | GBC2/IO80PPB1 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| D1 | IO213PDB3 |
| D2 | IO213NDB3 |
| D3 | IO223NDB3 |
| D4 | GAA2/IO225PPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO72RSB0 |
| D8 | GBC1/IO73RSB0 |
| D9 | GBB2/IO79PDB1 |
| D10 | IO79NDB1 |
| D11 | IO80NPB1 |
| D12 | GCB1/IO92PPB1 |
| E1 | V _{CC} |
| E2 | GFC0/IO209NDB3 |
| E3 | GFC1/IO209PDB3 |
| E4 | VCCIB3 |
| E5 | IO225NPB3 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | GCC1/IO91PDB1 |
| E9 | V _{CC} B1 |
| E10 | V _{CC} |
| E11 | GCA0/IO93NDB1 |
| E12 | IO94NDB1 |
| F1 | GFB0/IO208NPB3 |
| F2 | V _{COMPLF} |
| F3 | GFB1/IO208PPB3 |
| F4 | IO206NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO91NDB1 |
| F9 | GCB0/IO92NPB1 |
| F10 | GND |
| F11 | GCA1/IO93PDB1 |
| F12 | GCA2/IO94PDB1 |

| 144-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| G1 | GFA1/IO207PPB3 |
| G2 | GND |
| G3 | V _{CC} PLF |
| G4 | GFA0/IO207NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO111PPB1 |
| G9 | IO96NDB1 |
| G10 | GCC2/IO96PDB1 |
| G11 | IO95NDB1 |
| G12 | GCB2/IO95PDB1 |
| H1 | V _{CC} |
| H2 | GFB2/IO205PDB3 |
| H3 | GFC2/IO204PSB3 |
| H4 | GEC1/IO190PDB3 |
| H5 | V _{CC} |
| H6 | IO105PDB1 |
| H7 | IO105NDB1 |
| H8 | GDB2/IO115RSB2 |
| H9 | GDC0/IO111NPB1 |
| H10 | V _{CC} B1 |
| H11 | IO101PSB1 |
| H12 | V _{CC} |
| J1 | GEB1/IO189PDB3 |
| J2 | IO205NDB3 |
| J3 | V _{CC} B3 |
| J4 | GEC0/IO190NDB3 |
| J5 | IO160RSB2 |
| J6 | IO157RSB2 |
| J7 | V _{CC} |
| J8 | TCK |
| J9 | GDA2/IO114RSB2 |
| J10 | TDO |
| J11 | GDA1/IO113PDB1 |
| J12 | GDB1/IO112PDB1 |

| 144-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P1000 Function |
| K1 | GEB0/IO189NDB3 |
| K2 | GEA1/IO188PDB3 |
| K3 | GEA0/IO188NDB3 |
| K4 | GEA2/IO187RSB2 |
| K5 | IO169RSB2 |
| K6 | IO152RSB2 |
| K7 | GND |
| K8 | IO117RSB2 |
| K9 | GDC2/IO116RSB2 |
| K10 | GND |
| K11 | GDA0/IO113NDB1 |
| K12 | GDB0/IO112NDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO186RSB2 |
| L4 | IO172RSB2 |
| L5 | V _{CC} B2 |
| L6 | IO153RSB2 |
| L7 | IO144RSB2 |
| L8 | IO140RSB2 |
| L9 | TMS |
| L10 | V _{JTAG} |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO185RSB2 |
| M3 | IO173RSB2 |
| M4 | IO168RSB2 |
| M5 | IO161RSB2 |
| M6 | IO156RSB2 |
| M7 | IO145RSB2 |
| M8 | IO141RSB2 |
| M9 | TDI |
| M10 | V _{CC} B2 |
| M11 | V _{PUMP} |
| M12 | GNDQ |

256-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-8 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 256-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P250 Function |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO07RSB0 |
| A6 | IO10RSB0 |
| A7 | IO11RSB0 |
| A8 | IO15RSB0 |
| A9 | IO20RSB0 |
| A10 | IO25RSB0 |
| A11 | IO29RSB0 |
| A12 | IO33RSB0 |
| A13 | GBB1/IO38RSB0 |
| A14 | GBA0/IO39RSB0 |
| A15 | GBA1/IO40RSB0 |
| A16 | GND |
| B1 | GAB2/IO117UDB3 |
| B2 | GAA2/IO118UDB3 |
| B3 | NC |
| B4 | GAB1/IO03RSB0 |
| B5 | IO06RSB0 |
| B6 | IO09RSB0 |
| B7 | IO12RSB0 |
| B8 | IO16RSB0 |
| B9 | IO21RSB0 |
| B10 | IO26RSB0 |
| B11 | IO30RSB0 |
| B12 | GBC1/IO36RSB0 |
| B13 | GBB0/IO37RSB0 |
| B14 | NC |
| B15 | GBA2/IO41PDB1 |
| B16 | IO41NDB1 |
| C1 | IO117VDB3 |
| C2 | IO118VDB3 |
| C3 | NC |
| C4 | NC |

| 256-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P250 Function |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |
| C7 | IO13RSB0 |
| C8 | IO17RSB0 |
| C9 | IO22RSB0 |
| C10 | IO27RSB0 |
| C11 | IO31RSB0 |
| C12 | GBC0/IO35RSB0 |
| C13 | IO34RSB0 |
| C14 | NC |
| C15 | IO42NPB1 |
| C16 | IO44PDB1 |
| D1 | IO114VDB3 |
| D2 | IO114UDB3 |
| D3 | GAC2/IO116UDB3 |
| D4 | NC |
| D5 | GNDQ |
| D6 | IO08RSB0 |
| D7 | IO14RSB0 |
| D8 | IO18RSB0 |
| D9 | IO23RSB0 |
| D10 | IO28RSB0 |
| D11 | IO32RSB0 |
| D12 | GNDQ |
| D13 | NC |
| D14 | GBB2/IO42PPB1 |
| D15 | NC |
| D16 | IO44NDB1 |
| E1 | IO113PDB3 |
| E2 | NC |
| E3 | IO116VDB3 |
| E4 | IO115UDB3 |
| E5 | VMV0 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | IO19RSB0 |

| 256-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P250 Function |
| E9 | IO24RSB0 |
| E10 | V _{CC} B0 |
| E11 | V _{CC} B0 |
| E12 | VMV1 |
| E13 | GBC2/IO43PDB1 |
| E14 | IO46RSB1 |
| E15 | NC |
| E16 | IO45PDB1 |
| F1 | IO113NDB3 |
| F2 | IO112PPB3 |
| F3 | NC |
| F4 | IO115VDB3 |
| F5 | V _{CC} B3 |
| F6 | GND |
| F7 | V _{CC} |
| F8 | V _{CC} |
| F9 | V _{CC} |
| F10 | V _{CC} |
| F11 | GND |
| F12 | V _{CC} B1 |
| F13 | IO43NDB1 |
| F14 | NC |
| F15 | IO47PPB1 |
| F16 | IO45NDB1 |
| G1 | IO111NDB3 |
| G2 | IO111PDB3 |
| G3 | IO112NPB3 |
| G4 | GFC1/IO110PPB3 |
| G5 | V _{CC} B3 |
| G6 | V _{CC} |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | V _{CC} |
| G12 | V _{CC} B1 |

| 256-Pin FBGA | | 256-Pin FBGA | | 256-Pin FBGA | |
|--------------|---------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P250 Function | Pin Number | A3P250 Function | Pin Number | A3P250 Function |
| G13 | GCC1/IO48PPB1 | K1 | GFC2/IO105PDB3 | M5 | VMV3 |
| G14 | IO47NPB1 | K2 | IO107NPB3 | M6 | V _{CC} B2 |
| G15 | IO54PDB1 | K3 | IO104PPB3 | M7 | V _{CC} B2 |
| G16 | IO54NDB1 | K4 | NC | M8 | NC |
| H1 | GFB0/IO109NPB3 | K5 | V _{CC} B3 | M9 | IO74RSB2 |
| H2 | GFA0/IO108NDB3 | K6 | V _{CC} | M10 | V _{CC} B2 |
| H3 | GFB1/IO109PPB3 | K7 | GND | M11 | V _{CC} B2 |
| H4 | V _{COMPLF} | K8 | GND | M12 | VMV2 |
| H5 | GFC0/IO110NPB3 | K9 | GND | M13 | NC |
| H6 | V _{CC} | K10 | GND | M14 | GDB1/IO59UPB1 |
| H7 | GND | K11 | V _{CC} | M15 | GDC1/IO58UDB1 |
| H8 | GND | K12 | V _{CC} B1 | M16 | IO56NDB1 |
| H9 | GND | K13 | IO52NPB1 | N1 | IO103NDB3 |
| H10 | GND | K14 | IO55RSB1 | N2 | IO101PPB3 |
| H11 | V _{CC} | K15 | IO53NPB1 | N3 | GEC1/IO100PPB3 |
| H12 | GCC0/IO48NPB1 | K16 | IO51NDB1 | N4 | NC |
| H13 | GCB1/IO49PPB1 | L1 | IO105NDB3 | N5 | GNDQ |
| H14 | GCA0/IO50NPB1 | L2 | IO104NPB3 | N6 | GEA2/IO97RSB2 |
| H15 | NC | L3 | NC | N7 | IO86RSB2 |
| H16 | GCB0/IO49NPB1 | L4 | IO102RSB3 | N8 | IO82RSB2 |
| J1 | GFA2/IO107PPB3 | L5 | V _{CC} B3 | N9 | IO75RSB2 |
| J2 | GFA1/IO108PDB3 | L6 | GND | N10 | IO69RSB2 |
| J3 | V _{CC} PLF | L7 | V _{CC} | N11 | IO64RSB2 |
| J4 | IO106NDB3 | L8 | V _{CC} | N12 | GNDQ |
| J5 | GFB2/IO106PDB3 | L9 | V _{CC} | N13 | NC |
| J6 | V _{CC} | L10 | V _{CC} | N14 | V _{JTAG} |
| J7 | GND | L11 | GND | N15 | GDC0/IO58VDB1 |
| J8 | GND | L12 | V _{CC} B1 | N16 | GDA1/IO60UDB1 |
| J9 | GND | L13 | GDB0/IO59VPB1 | P1 | GEB1/IO99PDB3 |
| J10 | GND | L14 | IO57VDB1 | P2 | GEB0/IO99NDB3 |
| J11 | V _{CC} | L15 | IO57UDB1 | P3 | NC |
| J12 | GCB2/IO52PPB1 | L16 | IO56PDB1 | P4 | NC |
| J13 | GCA1/IO50PPB1 | M1 | IO103PDB3 | P5 | IO92RSB2 |
| J14 | GCC2/IO53PPB1 | M2 | NC | P6 | IO89RSB2 |
| J15 | NC | M3 | IO101NPB3 | P7 | IO85RSB2 |
| J16 | GCA2/IO51PDB1 | M4 | GEC0/IO100NPB3 | P8 | IO81RSB2 |

| 256-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P250 Function |
| P9 | IO76RSB2 |
| P10 | IO71RSB2 |
| P11 | IO66RSB2 |
| P12 | NC |
| P13 | TCK |
| P14 | V _{PUMP} |
| P15 | TRST |
| P16 | GDA0/IO60VDB1 |
| R1 | GEA1/IO98PDB3 |
| R2 | GEA0/IO98NDB3 |
| R3 | NC |
| R4 | GEC2/IO95RSB2 |
| R5 | IO91RSB2 |
| R6 | IO88RSB2 |
| R7 | IO84RSB2 |
| R8 | IO80RSB2 |
| R9 | IO77RSB2 |
| R10 | IO72RSB2 |
| R11 | IO68RSB2 |
| R12 | IO65RSB2 |
| R13 | GDB2/IO62RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO94RSB2 |
| T3 | GEB2/IO96RSB2 |
| T4 | IO93RSB2 |
| T5 | IO90RSB2 |
| T6 | IO87RSB2 |
| T7 | IO83RSB2 |
| T8 | IO79RSB2 |
| T9 | IO78RSB2 |
| T10 | IO73RSB2 |
| T11 | IO70RSB2 |
| T12 | GDC2/IO63RSB2 |

| 256-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P250 Function |
| T13 | IO67RSB2 |
| T14 | GDA2/IO61RSB2 |
| T15 | TMS |
| T16 | GND |

| 256-Pin FBGA | | 256-Pin FBGA | | 256-Pin FBGA | |
|--------------|-----------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P400 Function | Pin Number | A3P400 Function | Pin Number | A3P400 Function |
| A1 | GND | C5 | GAC0/IO04RSB0 | E9 | IO31RSB0 |
| A2 | GAA0/IO00RSB0 | C6 | GAC1/IO05RSB0 | E10 | V _{CC} B0 |
| A3 | GAA1/IO01RSB0 | C7 | IO20RSB0 | E11 | V _{CC} B0 |
| A4 | GAB0/IO02RSB0 | C8 | IO24RSB0 | E12 | VMV1 |
| A5 | IO16RSB0 | C9 | IO33RSB0 | E13 | GBC2/IO62PDB1 |
| A6 | IO17RSB0 | C10 | IO39RSB0 | E14 | IO65RSB1 |
| A7 | IO22RSB0 | C11 | IO45RSB0 | E15 | IO52RSB0 |
| A8 | IO28RSB0 | C12 | GBC0/IO54RSB0 | E16 | IO66PDB1 |
| A9 | IO34RSB0 | C13 | IO48RSB0 | F1 | IO150NDB3 |
| A10 | IO37RSB0 | C14 | VMV0 | F2 | IO149NPB3 |
| A11 | IO41RSB0 | C15 | IO61NPB1 | F3 | IO09RSB0 |
| A12 | IO43RSB0 | C16 | IO63PDB1 | F4 | IO152UDB3 |
| A13 | GBB1/IO57RSB0 | D1 | IO151VDB3 | F5 | V _{CC} B3 |
| A14 | GBA0/IO58RSB0 | D2 | IO151UDB3 | F6 | GND |
| A15 | GBA1/IO59RSB0 | D3 | GAC2/IO153UDB3 | F7 | V _{CC} |
| A16 | GND | D4 | IO06RSB0 | F8 | V _{CC} |
| B1 | GAB2/IO154UDB3 | D5 | GNDQ | F9 | V _{CC} |
| B2 | GAA2/IO155UDB3 | D6 | IO10RSB0 | F10 | V _{CC} |
| B3 | IO12RSB0 | D7 | IO19RSB0 | F11 | GND |
| B4 | GAB1/IO03RSB0 | D8 | IO26RSB0 | F12 | V _{CC} B1 |
| B5 | IO13RSB0 | D9 | IO30RSB0 | F13 | IO62NDB1 |
| B6 | IO14RSB0 | D10 | IO40RSB0 | F14 | IO49RSB0 |
| B7 | IO21RSB0 | D11 | IO46RSB0 | F15 | IO64PPB1 |
| B8 | IO27RSB0 | D12 | GNDQ | F16 | IO66NDB1 |
| B9 | IO32RSB0 | D13 | IO47RSB0 | G1 | IO148NDB3 |
| B10 | IO38RSB0 | D14 | GBB2/IO61PPB1 | G2 | IO148PDB3 |
| B11 | IO42RSB0 | D15 | IO53RSB0 | G3 | IO149PPB3 |
| B12 | GBC1/IO55RSB0 | D16 | IO63NDB1 | G4 | GFC1/IO147PPB3 |
| B13 | GBB0/IO56RSB0 | E1 | IO150PDB3 | G5 | V _{CC} B3 |
| B14 | IO44RSB0 | E2 | IO08RSB0 | G6 | V _{CC} |
| B15 | GBA2/IO60PDB1 | E3 | IO153VDB3 | G7 | GND |
| B16 | IO60NDB1 | E4 | IO152VDB3 | G8 | GND |
| C1 | IO154VDB3 | E5 | VMV0 | G9 | GND |
| C2 | IO155VDB3 | E6 | V _{CC} B0 | G10 | GND |
| C3 | IO11RSB0 | E7 | V _{CC} B0 | G11 | V _{CC} |
| C4 | IO07RSB0 | E8 | IO25RSB0 | G12 | V _{CC} B1 |

| 256-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P400 Function |
| G13 | GCC1/IO67PPB1 |
| G14 | IO64NPB1 |
| G15 | IO73PDB1 |
| G16 | IO73NDB1 |
| H1 | GFB0/IO146NPB3 |
| H2 | GFA0/IO145NDB3 |
| H3 | GFB1/IO146PPB3 |
| H4 | V _{COMPLF} |
| H5 | GFC0/IO147NPB3 |
| H6 | V _{CC} |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | V _{CC} |
| H12 | GCC0/IO67NPB1 |
| H13 | GCB1/IO68PPB1 |
| H14 | GCA0/IO69NPB1 |
| H15 | NC |
| H16 | GCB0/IO68NPB1 |
| J1 | GFA2/IO144PPB3 |
| J2 | GFA1/IO145PDB3 |
| J3 | V _{CCPLF} |
| J4 | IO143NDB3 |
| J5 | GFB2/IO143PDB3 |
| J6 | V _{CC} |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | V _{CC} |
| J12 | GCB2/IO71PPB1 |
| J13 | GCA1/IO69PPB1 |
| J14 | GCC2/IO72PPB1 |
| J15 | NC |
| J16 | GCA2/IO70PDB1 |

| 256-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| K1 | GFC2/IO142PDB3 |
| K2 | IO144NPB3 |
| K3 | IO141PPB3 |
| K4 | IO120RSB2 |
| K5 | V _{CC} B3 |
| K6 | V _{CC} |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | V _{CC} |
| K12 | V _{CC} B1 |
| K13 | IO71NPB1 |
| K14 | IO74RSB1 |
| K15 | IO72NPB1 |
| K16 | IO70NDB1 |
| L1 | IO142NDB3 |
| L2 | IO141NPB3 |
| L3 | IO125RSB2 |
| L4 | IO139RSB3 |
| L5 | V _{CC} B3 |
| L6 | GND |
| L7 | V _{CC} |
| L8 | V _{CC} |
| L9 | V _{CC} |
| L10 | V _{CC} |
| L11 | GND |
| L12 | V _{CC} B1 |
| L13 | GDB0/IO78VPB1 |
| L14 | IO76VDB1 |
| L15 | IO76UDB1 |
| L16 | IO75PDB1 |
| M1 | IO140PDB3 |
| M2 | IO130RSB2 |
| M3 | IO138NPB3 |
| M4 | GEC0/IO137NPB3 |

| 256-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| M5 | VMV3 |
| M6 | V _{CC} B2 |
| M7 | V _{CC} B2 |
| M8 | IO108RSB2 |
| M9 | IO101RSB2 |
| M10 | V _{CC} B2 |
| M11 | V _{CC} B2 |
| M12 | VMV2 |
| M13 | IO83RSB2 |
| M14 | GDB1/IO78UPB1 |
| M15 | GDC1/IO77UDB1 |
| M16 | IO75NDB1 |
| N1 | IO140NDB3 |
| N2 | IO138PPB3 |
| N3 | GEC1/IO137PPB3 |
| N4 | IO131RSB2 |
| N5 | GNDQ |
| N6 | GEA2/IO134RSB2 |
| N7 | IO117RSB2 |
| N8 | IO111RSB2 |
| N9 | IO99RSB2 |
| N10 | IO94RSB2 |
| N11 | IO87RSB2 |
| N12 | GNDQ |
| N13 | IO93RSB2 |
| N14 | V _{JTAG} |
| N15 | GDC0/IO77VDB1 |
| N16 | GDA1/IO79UDB1 |
| P1 | GEB1/IO136PDB3 |
| P2 | GEB0/IO136NDB3 |
| P3 | VMV2 |
| P4 | IO129RSB2 |
| P5 | IO128RSB2 |
| P6 | IO122RSB2 |
| P7 | IO115RSB2 |
| P8 | IO110RSB2 |

| 256-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P400 Function |
| P9 | IO98RSB2 |
| P10 | IO95RSB2 |
| P11 | IO88RSB2 |
| P12 | IO84RSB2 |
| P13 | TCK |
| P14 | V _{PUMP} |
| P15 | TRST |
| P16 | GDA0/IO79VDB1 |
| R1 | GEA1/IO135PDB3 |
| R2 | GEA0/IO135NDB3 |
| R3 | IO127RSB2 |
| R4 | GEC2/IO132RSB2 |
| R5 | IO123RSB2 |
| R6 | IO118RSB2 |
| R7 | IO112RSB2 |
| R8 | IO106RSB2 |
| R9 | IO100RSB2 |
| R10 | IO96RSB2 |
| R11 | IO89RSB2 |
| R12 | IO85RSB2 |
| R13 | GDB2/IO81RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO126RSB2 |
| T3 | GEB2/IO133RSB2 |
| T4 | IO124RSB2 |
| T5 | IO116RSB2 |
| T6 | IO113RSB2 |
| T7 | IO107RSB2 |
| T8 | IO105RSB2 |
| T9 | IO102RSB2 |
| T10 | IO97RSB2 |
| T11 | IO92RSB2 |
| T12 | GDC2/IO82RSB2 |

| 256-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P400 Function |
| T13 | IO86RSB2 |
| T14 | GDA2/IO80RSB2 |
| T15 | TMS |
| T16 | GND |

| 256-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P600 Function |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO11RSB0 |
| A6 | IO16RSB0 |
| A7 | IO18RSB0 |
| A8 | IO28RSB0 |
| A9 | IO34RSB0 |
| A10 | IO37RSB0 |
| A11 | IO41RSB0 |
| A12 | IO43RSB0 |
| A13 | GBB1/IO57RSB0 |
| A14 | GBA0/IO58RSB0 |
| A15 | GBA1/IO59RSB0 |
| A16 | GND |
| B1 | GAB2/IO173PDB3 |
| B2 | GAA2/IO174PDB3 |
| B3 | GNDQ |
| B4 | GAB1/IO03RSB0 |
| B5 | IO13RSB0 |
| B6 | IO14RSB0 |
| B7 | IO21RSB0 |
| B8 | IO27RSB0 |
| B9 | IO32RSB0 |
| B10 | IO38RSB0 |
| B11 | IO42RSB0 |
| B12 | GBC1/IO55RSB0 |
| B13 | GBB0/IO56RSB0 |
| B14 | IO52RSB0 |
| B15 | GBA2/IO60PDB1 |
| B16 | IO60NDB1 |
| C1 | IO173NDB3 |
| C2 | IO174NDB3 |
| C3 | VMV3 |
| C4 | IO07RSB0 |

| 256-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P600 Function |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |
| C7 | IO20RSB0 |
| C8 | IO24RSB0 |
| C9 | IO33RSB0 |
| C10 | IO39RSB0 |
| C11 | IO44RSB0 |
| C12 | GBC0/IO54RSB0 |
| C13 | IO51RSB0 |
| C14 | VMV0 |
| C15 | IO61NPB1 |
| C16 | IO63PDB1 |
| D1 | IO171NDB3 |
| D2 | IO171PDB3 |
| D3 | GAC2/IO172PDB3 |
| D4 | IO06RSB0 |
| D5 | GNDQ |
| D6 | IO10RSB0 |
| D7 | IO19RSB0 |
| D8 | IO26RSB0 |
| D9 | IO30RSB0 |
| D10 | IO40RSB0 |
| D11 | IO45RSB0 |
| D12 | GNDQ |
| D13 | IO50RSB0 |
| D14 | GBB2/IO61PPB1 |
| D15 | IO53RSB0 |
| D16 | IO63NDB1 |
| E1 | IO166PDB3 |
| E2 | IO167NPB3 |
| E3 | IO172NDB3 |
| E4 | IO169NDB3 |
| E5 | VMV0 |
| E6 | V _{CC} B0 |
| E7 | V _{CC} B0 |
| E8 | IO25RSB0 |

| 256-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P600 Function |
| E9 | IO31RSB0 |
| E10 | V _{CC} B0 |
| E11 | V _{CC} B0 |
| E12 | VMV1 |
| E13 | GBC2/IO62PDB1 |
| E14 | IO67PPB1 |
| E15 | IO64PPB1 |
| E16 | IO66PDB1 |
| F1 | IO166NDB3 |
| F2 | IO168NPB3 |
| F3 | IO167PPB3 |
| F4 | IO169PDB3 |
| F5 | V _{CC} B3 |
| F6 | GND |
| F7 | V _{CC} |
| F8 | V _{CC} |
| F9 | V _{CC} |
| F10 | V _{CC} |
| F11 | GND |
| F12 | V _{CC} B1 |
| F13 | IO62NDB1 |
| F14 | IO64NPB1 |
| F15 | IO65PPB1 |
| F16 | IO66NDB1 |
| G1 | IO165NDB3 |
| G2 | IO165PDB3 |
| G3 | IO168PPB3 |
| G4 | GFC1/IO164PPB3 |
| G5 | V _{CC} B3 |
| G6 | V _{CC} |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | V _{CC} |
| G12 | V _{CC} B1 |

| 256-Pin FBGA | | 256-Pin FBGA | | 256-Pin FBGA | |
|--------------|---------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P600 Function | Pin Number | A3P600 Function | Pin Number | A3P600 Function |
| G13 | GCC1/IO69PPB1 | K1 | GFC2/IO159PDB3 | M5 | VMV3 |
| G14 | IO65NPB1 | K2 | IO161NPB3 | M6 | V _{CC} B2 |
| G15 | IO75PDB1 | K3 | IO156PPB3 | M7 | V _{CC} B2 |
| G16 | IO75NDB1 | K4 | IO129RSB2 | M8 | IO117RSB2 |
| H1 | GFB0/IO163NPB3 | K5 | V _{CC} B3 | M9 | IO110RSB2 |
| H2 | GFA0/IO162NDB3 | K6 | V _{CC} | M10 | V _{CC} B2 |
| H3 | GFB1/IO163PPB3 | K7 | GND | M11 | V _{CC} B2 |
| H4 | V _{COMPLF} | K8 | GND | M12 | VMV2 |
| H5 | GFC0/IO164NPB3 | K9 | GND | M13 | IO94RSB2 |
| H6 | V _{CC} | K10 | GND | M14 | GDB1/IO87PPB1 |
| H7 | GND | K11 | V _{CC} | M15 | GDC1/IO86PDB1 |
| H8 | GND | K12 | V _{CC} B1 | M16 | IO84NDB1 |
| H9 | GND | K13 | IO73NPB1 | N1 | IO150NDB3 |
| H10 | GND | K14 | IO80NPB1 | N2 | IO147PPB3 |
| H11 | V _{CC} | K15 | IO74NPB1 | N3 | GEC1/IO146PPB3 |
| H12 | GCC0/IO69NPB1 | K16 | IO72NDB1 | N4 | IO140RSB2 |
| H13 | GCB1/IO70PPB1 | L1 | IO159NDB3 | N5 | GNDQ |
| H14 | GCA0/IO71NPB1 | L2 | IO156NPB3 | N6 | GEA2/IO143RSB2 |
| H15 | IO67NPB1 | L3 | IO151PPB3 | N7 | IO126RSB2 |
| H16 | GCB0/IO70NPB1 | L4 | IO158PSB3 | N8 | IO120RSB2 |
| J1 | GFA2/IO161PPB3 | L5 | V _{CC} B3 | N9 | IO108RSB2 |
| J2 | GFA1/IO162PDB3 | L6 | GND | N10 | IO103RSB2 |
| J3 | V _{CC} PLF | L7 | V _{CC} | N11 | IO99RSB2 |
| J4 | IO160NDB3 | L8 | V _{CC} | N12 | GNDQ |
| J5 | GFB2/IO160PDB3 | L9 | V _{CC} | N13 | IO92RSB2 |
| J6 | V _{CC} | L10 | V _{CC} | N14 | V _{JTAG} |
| J7 | GND | L11 | GND | N15 | GDC0/IO86NDB1 |
| J8 | GND | L12 | V _{CC} B1 | N16 | GDA1/IO88PDB1 |
| J9 | GND | L13 | GDB0/IO87NPB1 | P1 | GEB1/IO145PDB3 |
| J10 | GND | L14 | IO85NDB1 | P2 | GEB0/IO145NDB3 |
| J11 | V _{CC} | L15 | IO85PDB1 | P3 | VMV2 |
| J12 | GCB2/IO73PPB1 | L16 | IO84PDB1 | P4 | IO138RSB2 |
| J13 | GCA1/IO71PPB1 | M1 | IO150PDB3 | P5 | IO136RSB2 |
| J14 | GCC2/IO74PPB1 | M2 | IO151NPB3 | P6 | IO131RSB2 |
| J15 | IO80PPB1 | M3 | IO147NPB3 | P7 | IO124RSB2 |
| J16 | GCA2/IO72PDB1 | M4 | GEC0/IO146NPB3 | P8 | IO119RSB2 |

| 256-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P600 Function |
| P9 | IO107RSB2 |
| P10 | IO104RSB2 |
| P11 | IO97RSB2 |
| P12 | VMV1 |
| P13 | TCK |
| P14 | V _{PUMP} |
| P15 | TRST |
| P16 | GDA0/IO88NDB1 |
| R1 | GEA1/IO144PDB3 |
| R2 | GEA0/IO144NDB3 |
| R3 | IO139RSB2 |
| R4 | GEC2/IO141RSB2 |
| R5 | IO132RSB2 |
| R6 | IO127RSB2 |
| R7 | IO121RSB2 |
| R8 | IO114RSB2 |
| R9 | IO109RSB2 |
| R10 | IO105RSB2 |
| R11 | IO98RSB2 |
| R12 | IO96RSB2 |
| R13 | GDB2/IO90RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO137RSB2 |
| T3 | GEB2/IO142RSB2 |
| T4 | IO134RSB2 |
| T5 | IO125RSB2 |
| T6 | IO123RSB2 |
| T7 | IO118RSB2 |
| T8 | IO115RSB2 |
| T9 | IO111RSB2 |
| T10 | IO106RSB2 |
| T11 | IO102RSB2 |
| T12 | GDC2/IO91RSB2 |

| 256-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P600 Function |
| T13 | IO93RSB2 |
| T14 | GDA2/IO89RSB2 |
| T15 | TMS |
| T16 | GND |

| 256-Pin FBGA | | 256-Pin FBGA | | 256-Pin FBGA | |
|--------------|------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P1000 Function | Pin Number | A3P1000 Function | Pin Number | A3P1000 Function |
| A1 | GND | C7 | IO25RSB0 | E13 | GBC2/IO80PDB1 |
| A2 | GAA0/IO00RSB0 | C8 | IO36RSB0 | E14 | IO83PPB1 |
| A3 | GAA1/IO01RSB0 | C9 | IO42RSB0 | E15 | IO86PPB1 |
| A4 | GAB0/IO02RSB0 | C10 | IO49RSB0 | E16 | IO87PDB1 |
| A5 | IO16RSB0 | C11 | IO56RSB0 | F1 | IO217NDB3 |
| A6 | IO22RSB0 | C12 | GBC0/IO72RSB0 | F2 | IO218NDB3 |
| A7 | IO28RSB0 | C13 | IO62RSB0 | F3 | IO216PDB3 |
| A8 | IO35RSB0 | C14 | VMV0 | F4 | IO216NDB3 |
| A9 | IO45RSB0 | C15 | IO78NDB1 | F5 | V _{CC} B3 |
| A10 | IO50RSB0 | C16 | IO81NDB1 | F6 | GND |
| A11 | IO55RSB0 | D1 | IO222NDB3 | F7 | V _{CC} |
| A12 | IO61RSB0 | D2 | IO222PDB3 | F8 | V _{CC} |
| A13 | GBB1/IO75RSB0 | D3 | GAC2/IO223PDB3 | F9 | V _{CC} |
| A14 | GBA0/IO76RSB0 | D4 | IO223NDB3 | F10 | V _{CC} |
| A15 | GBA1/IO77RSB0 | D5 | GNDQ | F11 | GND |
| A16 | GND | D6 | IO23RSB0 | F12 | V _{CC} B1 |
| B1 | GAB2/IO224PDB3 | D7 | IO29RSB0 | F13 | IO83NPB1 |
| B2 | GAA2/IO225PDB3 | D8 | IO33RSB0 | F14 | IO86NPB1 |
| B3 | GNDQ | D9 | IO46RSB0 | F15 | IO90PPB1 |
| B4 | GAB1/IO03RSB0 | D10 | IO52RSB0 | F16 | IO87NDB1 |
| B5 | IO17RSB0 | D11 | IO60RSB0 | G1 | IO210PSB3 |
| B6 | IO21RSB0 | D12 | GNDQ | G2 | IO213NDB3 |
| B7 | IO27RSB0 | D13 | IO80NDB1 | G3 | IO213PDB3 |
| B8 | IO34RSB0 | D14 | GBB2/IO79PDB1 | G4 | GFC1/IO209PPB3 |
| B9 | IO44RSB0 | D15 | IO79NDB1 | G5 | V _{CC} B3 |
| B10 | IO51RSB0 | D16 | IO82NSB1 | G6 | V _{CC} |
| B11 | IO57RSB0 | E1 | IO217PDB3 | G7 | GND |
| B12 | GBC1/IO73RSB0 | E2 | IO218PDB3 | G8 | GND |
| B13 | GBB0/IO74RSB0 | E3 | IO221NDB3 | G9 | GND |
| B14 | IO71RSB0 | E4 | IO221PDB3 | G10 | GND |
| B15 | GBA2/IO78PDB1 | E5 | VMV0 | G11 | V _{CC} |
| B16 | IO81PDB1 | E6 | V _{CC} B0 | G12 | V _{CC} B1 |
| C1 | IO224NDB3 | E7 | V _{CC} B0 | G13 | GCC1/IO91PPB1 |
| C2 | IO225NDB3 | E8 | IO38RSB0 | G14 | IO90NPB1 |
| C3 | VMV3 | E9 | IO47RSB0 | G15 | IO88PDB1 |
| C4 | IO11RSB0 | E10 | V _{CC} B0 | G16 | IO88NDB1 |
| C5 | GAC0/IO04RSB0 | E11 | V _{CC} B0 | H1 | GFB0/IO208NPB3 |
| C6 | GAC1/IO05RSB0 | E12 | VMV1 | H2 | GFA0/IO207NDB3 |

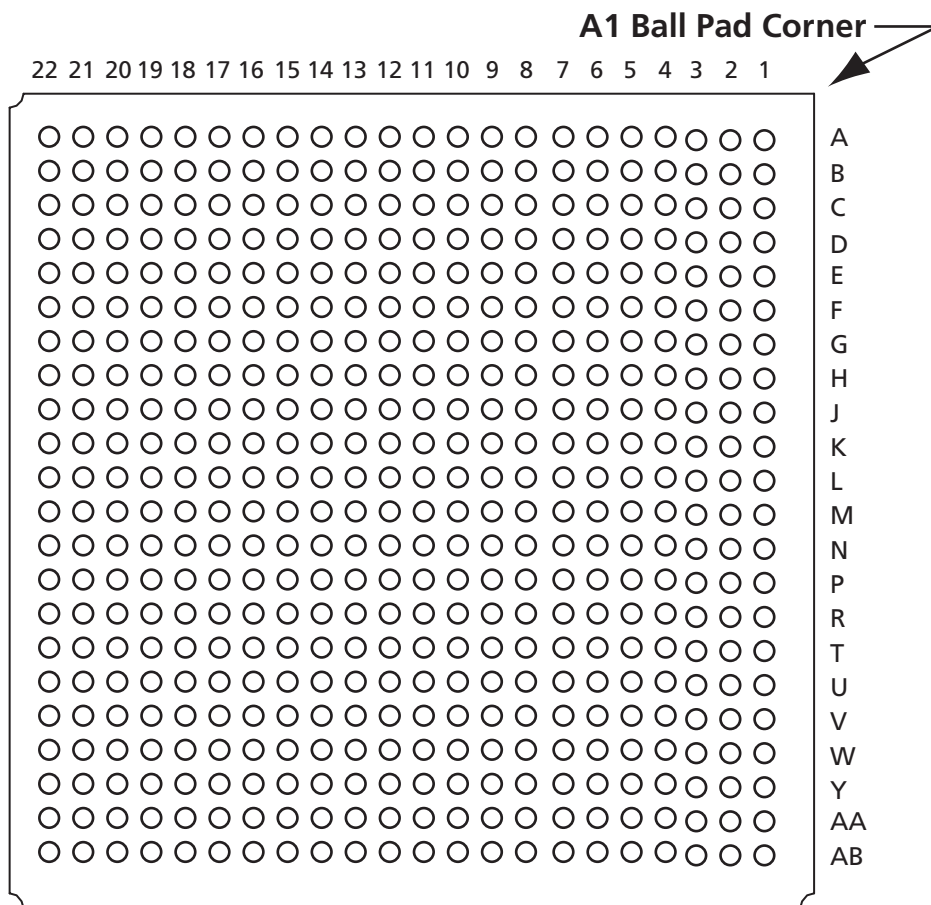
| 256-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P1000 Function |
| H3 | GFB1/IO208PPB3 |
| H4 | V _{COMPLF} |
| H5 | GFC0/IO209NPB3 |
| H6 | V _{CC} |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | V _{CC} |
| H12 | GCC0/IO91NPB1 |
| H13 | GCB1/IO92PPB1 |
| H14 | GCA0/IO93NPB1 |
| H15 | IO96NPB1 |
| H16 | GCB0/IO92NPB1 |
| J1 | GFA2/IO206PSB3 |
| J2 | GFA1/IO207PDB3 |
| J3 | V _{CCPLF} |
| J4 | IO205NDB3 |
| J5 | GFB2/IO205PDB3 |
| J6 | V _{CC} |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | V _{CC} |
| J12 | GCB2/IO95PPB1 |
| J13 | GCA1/IO93PPB1 |
| J14 | GCC2/IO96PPB1 |
| J15 | IO100PPB1 |
| J16 | GCA2/IO94PSB1 |
| K1 | GFC2/IO204PDB3 |
| K2 | IO204NDB3 |
| K3 | IO203NDB3 |
| K4 | IO203PDB3 |
| K5 | V _{CCB3} |
| K6 | V _{CC} |
| K7 | GND |
| K8 | GND |

| 256-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P1000 Function |
| K9 | GND |
| K10 | GND |
| K11 | V _{CC} |
| K12 | V _{CCB1} |
| K13 | IO95NPB1 |
| K14 | IO100NPB1 |
| K15 | IO102NDB1 |
| K16 | IO102PDB1 |
| L1 | IO202NDB3 |
| L2 | IO202PDB3 |
| L3 | IO196PPB3 |
| L4 | IO193PPB3 |
| L5 | V _{CCB3} |
| L6 | GND |
| L7 | V _{CC} |
| L8 | V _{CC} |
| L9 | V _{CC} |
| L10 | V _{CC} |
| L11 | GND |
| L12 | V _{CCB1} |
| L13 | GDB0/IO112NPB1 |
| L14 | IO106NDB1 |
| L15 | IO106PDB1 |
| L16 | IO107PDB1 |
| M1 | IO197NSB3 |
| M2 | IO196NPB3 |
| M3 | IO193NPB3 |
| M4 | GEC0/IO190NPB3 |
| M5 | VMV3 |
| M6 | V _{CCB2} |
| M7 | V _{CCB2} |
| M8 | IO147RSB2 |
| M9 | IO136RSB2 |
| M10 | V _{CCB2} |
| M11 | V _{CCB2} |
| M12 | VMV2 |
| M13 | IO110NDB1 |
| M14 | GDB1/IO112PPB1 |

| 256-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P1000 Function |
| M15 | GDC1/IO111PDB1 |
| M16 | IO107NDB1 |
| N1 | IO194PSB3 |
| N2 | IO192PPB3 |
| N3 | GEC1/IO190PPB3 |
| N4 | IO192NPB3 |
| N5 | GNDQ |
| N6 | GEA2/IO187RSB2 |
| N7 | IO161RSB2 |
| N8 | IO155RSB2 |
| N9 | IO141RSB2 |
| N10 | IO129RSB2 |
| N11 | IO124RSB2 |
| N12 | GNDQ |
| N13 | IO110PDB1 |
| N14 | V _{JTAG} |
| N15 | GDC0/IO111NDB1 |
| N16 | GDA1/IO113PDB1 |
| P1 | GEB1/IO189PDB3 |
| P2 | GEB0/IO189NDB3 |
| P3 | VMV2 |
| P4 | IO179RSB2 |
| P5 | IO171RSB2 |
| P6 | IO165RSB2 |
| P7 | IO159RSB2 |
| P8 | IO151RSB2 |
| P9 | IO137RSB2 |
| P10 | IO134RSB2 |
| P11 | IO128RSB2 |
| P12 | VMV1 |
| P13 | TCK |
| P14 | V _{PUMP} |
| P15 | TRST |
| P16 | GDA0/IO113NDB1 |
| R1 | GEA1/IO188PDB3 |
| R2 | GEA0/IO188NDB3 |
| R3 | IO184RSB2 |
| R4 | GEC2/IO185RSB2 |

| 256-Pin FBGA | |
|--------------|------------------|
| Pin Number | A3P1000 Function |
| R5 | IO168RSB2 |
| R6 | IO163RSB2 |
| R7 | IO157RSB2 |
| R8 | IO149RSB2 |
| R9 | IO143RSB2 |
| R10 | IO138RSB2 |
| R11 | IO131RSB2 |
| R12 | IO125RSB2 |
| R13 | GDB2/IO115RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO183RSB2 |
| T3 | GEB2/IO186RSB2 |
| T4 | IO172RSB2 |
| T5 | IO170RSB2 |
| T6 | IO164RSB2 |
| T7 | IO158RSB2 |
| T8 | IO153RSB2 |
| T9 | IO142RSB2 |
| T10 | IO135RSB2 |
| T11 | IO130RSB2 |
| T12 | GDC2/IO116RSB2 |
| T13 | IO120RSB2 |
| T14 | GDA2/IO114RSB2 |
| T15 | TMS |
| T16 | GND |

484-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-9 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|--------------------|--------------|--------------------|--------------|-----------------|
| Pin Number | A3P400 Function | Pin Number | A3P400 Function | Pin Number | A3P400 Function |
| A1 | GND | B15 | NC | D7 | GAB0/IO02RSB0 |
| A2 | GND | B16 | NC | D8 | IO16RSB0 |
| A3 | V _{CC} B0 | B17 | NC | D9 | IO17RSB0 |
| A4 | NC | B18 | NC | D10 | IO22RSB0 |
| A5 | NC | B19 | NC | D11 | IO28RSB0 |
| A6 | IO15RSB0 | B20 | NC | D12 | IO34RSB0 |
| A7 | IO18RSB0 | B21 | V _{CC} B1 | D13 | IO37RSB0 |
| A8 | NC | B22 | GND | D14 | IO41RSB0 |
| A9 | NC | C1 | V _{CC} B3 | D15 | IO43RSB0 |
| A10 | IO23RSB0 | C2 | NC | D16 | GBB1/IO57RSB0 |
| A11 | IO29RSB0 | C3 | NC | D17 | GBA0/IO58RSB0 |
| A12 | IO35RSB0 | C4 | NC | D18 | GBA1/IO59RSB0 |
| A13 | IO36RSB0 | C5 | GND | D19 | GND |
| A14 | NC | C6 | NC | D20 | NC |
| A15 | NC | C7 | NC | D21 | NC |
| A16 | IO50RSB0 | C8 | V _{CC} | D22 | NC |
| A17 | IO51RSB0 | C9 | V _{CC} | E1 | NC |
| A18 | NC | C10 | NC | E2 | NC |
| A19 | NC | C11 | NC | E3 | GND |
| A20 | V _{CC} B0 | C12 | NC | E4 | GAB2/IO154UDB3 |
| A21 | GND | C13 | NC | E5 | GAA2/IO155UDB3 |
| A22 | GND | C14 | V _{CC} | E6 | IO12RSB0 |
| B1 | GND | C15 | V _{CC} | E7 | GAB1/IO03RSB0 |
| B2 | V _{CC} B3 | C16 | NC | E8 | IO13RSB0 |
| B3 | NC | C17 | NC | E9 | IO14RSB0 |
| B4 | NC | C18 | GND | E10 | IO21RSB0 |
| B5 | NC | C19 | NC | E11 | IO27RSB0 |
| B6 | NC | C20 | NC | E12 | IO32RSB0 |
| B7 | NC | C21 | NC | E13 | IO38RSB0 |
| B8 | NC | C22 | V _{CC} B1 | E14 | IO42RSB0 |
| B9 | NC | D1 | NC | E15 | GBC1/IO55RSB0 |
| B10 | NC | D2 | NC | E16 | GBB0/IO56RSB0 |
| B11 | NC | D3 | NC | E17 | IO44RSB0 |
| B12 | NC | D4 | GND | E18 | GBA2/IO60PDB1 |
| B13 | NC | D5 | GAA0/IO00RSB0 | E19 | IO60NDB1 |
| B14 | NC | D6 | GAA1/IO01RSB0 | E20 | GND |

| 484-Pin FBGA | |
|--------------|-----------------|
| Pin Number | A3P400 Function |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | NC |
| F3 | NC |
| F4 | IO154VDB3 |
| F5 | IO155VDB3 |
| F6 | IO11RSB0 |
| F7 | IO07RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO20RSB0 |
| F11 | IO24RSB0 |
| F12 | IO33RSB0 |
| F13 | IO39RSB0 |
| F14 | IO45RSB0 |
| F15 | GBC0/IO54RSB0 |
| F16 | IO48RSB0 |
| F17 | VMV0 |
| F18 | IO61NPB1 |
| F19 | IO63PDB1 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | NC |
| G2 | NC |
| G3 | NC |
| G4 | IO151VDB3 |
| G5 | IO151UDB3 |
| G6 | GAC2/IO153UDB3 |
| G7 | IO06RSB0 |
| G8 | GNDQ |
| G9 | IO10RSB0 |
| G10 | IO19RSB0 |
| G11 | IO26RSB0 |
| G12 | IO30RSB0 |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| G13 | IO40RSB0 |
| G14 | IO46RSB0 |
| G15 | GNDQ |
| G16 | IO47RSB0 |
| G17 | GBB2/IO61PPB1 |
| G18 | IO53RSB0 |
| G19 | IO63NDB1 |
| G20 | NC |
| G21 | NC |
| G22 | NC |
| H1 | NC |
| H2 | NC |
| H3 | V _{CC} |
| H4 | IO150PDB3 |
| H5 | IO08RSB0 |
| H6 | IO153VDB3 |
| H7 | IO152VDB3 |
| H8 | VMV0 |
| H9 | V _{CC} B0 |
| H10 | V _{CC} B0 |
| H11 | IO25RSB0 |
| H12 | IO31RSB0 |
| H13 | V _{CC} B0 |
| H14 | V _{CC} B0 |
| H15 | VMV1 |
| H16 | GBC2/IO62PDB1 |
| H17 | IO65RSB1 |
| H18 | IO52RSB0 |
| H19 | IO66PDB1 |
| H20 | V _{CC} |
| H21 | NC |
| H22 | NC |
| J1 | NC |
| J2 | NC |
| J3 | NC |
| J4 | IO150NDB3 |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| J5 | IO149NPB3 |
| J6 | IO09RSB0 |
| J7 | IO152UDB3 |
| J8 | V _{CC} B3 |
| J9 | GND |
| J10 | V _{CC} |
| J11 | V _{CC} |
| J12 | V _{CC} |
| J13 | V _{CC} |
| J14 | GND |
| J15 | V _{CC} B1 |
| J16 | IO62NDB1 |
| J17 | IO49RSB0 |
| J18 | IO64PPB1 |
| J19 | IO66NDB1 |
| J20 | NC |
| J21 | NC |
| J22 | NC |
| K1 | NC |
| K2 | NC |
| K3 | NC |
| K4 | IO148NDB3 |
| K5 | IO148PDB3 |
| K6 | IO149PPB3 |
| K7 | GFC1/IO147PPB3 |
| K8 | V _{CC} B3 |
| K9 | V _{CC} |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | V _{CC} |
| K15 | V _{CC} B1 |
| K16 | GCC1/IO67PPB1 |
| K17 | IO64NPB1 |
| K18 | IO73PDB1 |

| 484-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P400 Function |
| K19 | IO73NDB1 |
| K20 | NC |
| K21 | NC |
| K22 | NC |
| L1 | NC |
| L2 | NC |
| L3 | NC |
| L4 | GFB0/IO146NPB3 |
| L5 | GFA0/IO145NDB3 |
| L6 | GFB1/IO146PPB3 |
| L7 | V _{COMPLF} |
| L8 | GFC0/IO147NPB3 |
| L9 | V _{CC} |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | V _{CC} |
| L15 | GCC0/IO67NPB1 |
| L16 | GCB1/IO68PPB1 |
| L17 | GCA0/IO69NPB1 |
| L18 | NC |
| L19 | GCB0/IO68NPB1 |
| L20 | NC |
| L21 | NC |
| L22 | NC |
| M1 | NC |
| M2 | NC |
| M3 | NC |
| M4 | GFA2/IO144PPB3 |
| M5 | GFA1/IO145PDB3 |
| M6 | V _{CCPLF} |
| M7 | IO143NDB3 |
| M8 | GFB2/IO143PDB3 |
| M9 | V _{CC} |
| M10 | GND |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | V _{CC} |
| M15 | GCB2/IO71PPB1 |
| M16 | GCA1/IO69PPB1 |
| M17 | GCC2/IO72PPB1 |
| M18 | NC |
| M19 | GCA2/IO70PDB1 |
| M20 | NC |
| M21 | NC |
| M22 | NC |
| N1 | NC |
| N2 | NC |
| N3 | NC |
| N4 | GFC2/IO142PDB3 |
| N5 | IO144NPB3 |
| N6 | IO141PPB3 |
| N7 | IO120RSB2 |
| N8 | V _{CC} B3 |
| N9 | V _{CC} |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | V _{CC} |
| N15 | V _{CC} B1 |
| N16 | IO71NPB1 |
| N17 | IO74RSB1 |
| N18 | IO72NPB1 |
| N19 | IO70NDB1 |
| N20 | NC |
| N21 | NC |
| N22 | NC |
| P1 | NC |
| P2 | NC |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| P3 | NC |
| P4 | IO142NDB3 |
| P5 | IO141NPB3 |
| P6 | IO125RSB2 |
| P7 | IO139RSB3 |
| P8 | V _{CC} B3 |
| P9 | GND |
| P10 | V _{CC} |
| P11 | V _{CC} |
| P12 | V _{CC} |
| P13 | V _{CC} |
| P14 | GND |
| P15 | V _{CC} B1 |
| P16 | GDB0/IO78VVPB1 |
| P17 | IO76VDB1 |
| P18 | IO76UDB1 |
| P19 | IO75PDB1 |
| P20 | NC |
| P21 | NC |
| P22 | NC |
| R1 | NC |
| R2 | NC |
| R3 | V _{CC} |
| R4 | IO140PDB3 |
| R5 | IO130RSB2 |
| R6 | IO138NPB3 |
| R7 | GEC0/IO137NPB3 |
| R8 | VMV3 |
| R9 | V _{CC} B2 |
| R10 | V _{CC} B2 |
| R11 | IO108RSB2 |
| R12 | IO101RSB2 |
| R13 | V _{CC} B2 |
| R14 | V _{CC} B2 |
| R15 | VMV2 |
| R16 | IO83RSB2 |

| 484-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P400 Function |
| R17 | GDB1/IO78UPB1 |
| R18 | GDC1/IO77UDB1 |
| R19 | IO75NDB1 |
| R20 | V _{CC} |
| R21 | NC |
| R22 | NC |
| T1 | NC |
| T2 | NC |
| T3 | NC |
| T4 | IO140NDB3 |
| T5 | IO138PPB3 |
| T6 | GEC1/IO137PPB3 |
| T7 | IO131RSB2 |
| T8 | GNDQ |
| T9 | GEA2/IO134RSB2 |
| T10 | IO117RSB2 |
| T11 | IO111RSB2 |
| T12 | IO99RSB2 |
| T13 | IO94RSB2 |
| T14 | IO87RSB2 |
| T15 | GNDQ |
| T16 | IO93RSB2 |
| T17 | V _{JTAG} |
| T18 | GDC0/IO77VDB1 |
| T19 | GDA1/IO79UDB1 |
| T20 | NC |
| T21 | NC |
| T22 | NC |
| U1 | NC |
| U2 | NC |
| U3 | NC |
| U4 | GEB1/IO136PDB3 |
| U5 | GEB0/IO136NDB3 |
| U6 | VMV2 |
| U7 | IO129RSB2 |
| U8 | IO128RSB2 |

| 484-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P400 Function |
| U9 | IO122RSB2 |
| U10 | IO115RSB2 |
| U11 | IO110RSB2 |
| U12 | IO98RSB2 |
| U13 | IO95RSB2 |
| U14 | IO88RSB2 |
| U15 | IO84RSB2 |
| U16 | TCK |
| U17 | V _{PUMP} |
| U18 | TRST |
| U19 | GDA0/IO79VDB1 |
| U20 | NC |
| U21 | NC |
| U22 | NC |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO135PDB3 |
| V5 | GEA0/IO135NDB3 |
| V6 | IO127RSB2 |
| V7 | GEC2/IO132RSB2 |
| V8 | IO123RSB2 |
| V9 | IO118RSB2 |
| V10 | IO112RSB2 |
| V11 | IO106RSB2 |
| V12 | IO100RSB2 |
| V13 | IO96RSB2 |
| V14 | IO89RSB2 |
| V15 | IO85RSB2 |
| V16 | GDB2/IO81RSB2 |
| V17 | TDI |
| V18 | NC |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | NC |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO126RSB2 |
| W6 | GEB2/IO133RSB2 |
| W7 | IO124RSB2 |
| W8 | IO116RSB2 |
| W9 | IO113RSB2 |
| W10 | IO107RSB2 |
| W11 | IO105RSB2 |
| W12 | IO102RSB2 |
| W13 | IO97RSB2 |
| W14 | IO92RSB2 |
| W15 | GDC2/IO82RSB2 |
| W16 | IO86RSB2 |
| W17 | GDA2/IO80RSB2 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | V _{CC} B3 |
| Y2 | NC |
| Y3 | NC |
| Y4 | NC |
| Y5 | GND |
| Y6 | NC |
| Y7 | NC |
| Y8 | V _{CC} |
| Y9 | V _{CC} |
| Y10 | NC |
| Y11 | NC |
| Y12 | NC |
| Y13 | NC |
| Y14 | V _{CC} |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| Y15 | V _{CC} |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | V _{CC} B1 |
| AA1 | GND |
| AA2 | V _{CC} B3 |
| AA3 | NC |
| AA4 | NC |
| AA5 | NC |
| AA6 | NC |
| AA7 | NC |
| AA8 | NC |
| AA9 | NC |
| AA10 | NC |
| AA11 | NC |
| AA12 | NC |
| AA13 | NC |
| AA14 | NC |
| AA15 | NC |
| AA16 | NC |
| AA17 | NC |
| AA18 | NC |
| AA19 | NC |
| AA20 | NC |
| AA21 | V _{CC} B1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | V _{CC} B2 |
| AB4 | NC |
| AB5 | NC |
| AB6 | IO121RSB2 |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P400 Function |
| AB7 | IO119RSB2 |
| AB8 | IO114RSB2 |
| AB9 | IO109RSB2 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO104RSB2 |
| AB13 | IO103RSB2 |
| AB14 | NC |
| AB15 | NC |
| AB16 | IO91RSB2 |
| AB17 | IO90RSB2 |
| AB18 | NC |
| AB19 | NC |
| AB20 | V _{CC} B2 |
| AB21 | GND |
| AB22 | GND |

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|--------------------|--------------|--------------------|--------------|-----------------|
| Pin Number | A3P600 Function | Pin Number | A3P600 Function | Pin Number | A3P600 Function |
| A1 | GND | B15 | NC | D7 | GAB0/IO02RSB0 |
| A2 | GND | B16 | IO47RSB0 | D8 | IO11RSB0 |
| A3 | VCCIB0 | B17 | IO49RSB0 | D9 | IO16RSB0 |
| A4 | NC | B18 | NC | D10 | IO18RSB0 |
| A5 | NC | B19 | NC | D11 | IO28RSB0 |
| A6 | IO09RSB0 | B20 | NC | D12 | IO34RSB0 |
| A7 | IO15RSB0 | B21 | V _{CC} B1 | D13 | IO37RSB0 |
| A8 | NC | B22 | GND | D14 | IO41RSB0 |
| A9 | NC | C1 | V _{CC} B3 | D15 | IO43RSB0 |
| A10 | IO22RSB0 | C2 | NC | D16 | GBB1/IO57RSB0 |
| A11 | IO23RSB0 | C3 | NC | D17 | GAA0/IO58RSB0 |
| A12 | IO29RSB0 | C4 | NC | D18 | GAA1/IO59RSB0 |
| A13 | IO35RSB0 | C5 | GND | D19 | GND |
| A14 | NC | C6 | NC | D20 | NC |
| A15 | NC | C7 | NC | D21 | NC |
| A16 | IO46RSB0 | C8 | V _{CC} | D22 | NC |
| A17 | IO48RSB0 | C9 | V _{CC} | E1 | NC |
| A18 | NC | C10 | NC | E2 | NC |
| A19 | NC | C11 | NC | E3 | GND |
| A20 | V _{CC} B0 | C12 | NC | E4 | GAB2/IO173PDB3 |
| A21 | GND | C13 | NC | E5 | GAA2/IO174PDB3 |
| A22 | GND | C14 | V _{CC} | E6 | GNDQ |
| B1 | GND | C15 | V _{CC} | E7 | GAB1/IO03RSB0 |
| B2 | V _{CC} B3 | C16 | NC | E8 | IO13RSB0 |
| B3 | NC | C17 | NC | E9 | IO14RSB0 |
| B4 | NC | C18 | GND | E10 | IO21RSB0 |
| B5 | NC | C19 | NC | E11 | IO27RSB0 |
| B6 | IO08RSB0 | C20 | NC | E12 | IO32RSB0 |
| B7 | IO12RSB0 | C21 | NC | E13 | IO38RSB0 |
| B8 | NC | C22 | V _{CC} B1 | E14 | IO42RSB0 |
| B9 | NC | D1 | NC | E15 | GBC1/IO55RSB0 |
| B10 | IO17RSB0 | D2 | NC | E16 | GBB0/IO56RSB0 |
| B11 | NC | D3 | NC | E17 | IO52RSB0 |
| B12 | NC | D4 | GND | E18 | GAA2/IO60PDB1 |
| B13 | IO36RSB0 | D5 | GAA0/IO00RSB0 | E19 | IO60NDB1 |
| B14 | NC | D6 | GAA1/IO01RSB0 | E20 | GND |



| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|-----------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P600 Function | Pin Number | A3P600 Function | Pin Number | A3P600 Function |
| E21 | NC | G13 | IO40RSB0 | J5 | IO168NPB3 |
| E22 | NC | G14 | IO45RSB0 | J6 | IO167PPB3 |
| F1 | NC | G15 | GNDQ | J7 | IO169PDB3 |
| F2 | NC | G16 | IO50RSB0 | J8 | V _{CC} B3 |
| F3 | NC | G17 | GBB2/IO61PPB1 | J9 | GND |
| F4 | IO173NDB3 | G18 | IO53RSB0 | J10 | V _{CC} |
| F5 | IO174NDB3 | G19 | IO63NDB1 | J11 | V _{CC} |
| F6 | VMV3 | G20 | NC | J12 | V _{CC} |
| F7 | IO07RSB0 | G21 | NC | J13 | V _{CC} |
| F8 | GAC0/IO04RSB0 | G22 | NC | J14 | GND |
| F9 | GAC1/IO05RSB0 | H1 | NC | J15 | V _{CC} B1 |
| F10 | IO20RSB0 | H2 | NC | J16 | IO62NDB1 |
| F11 | IO24RSB0 | H3 | V _{CC} | J17 | IO64NPB1 |
| F12 | IO33RSB0 | H4 | IO166PDB3 | J18 | IO65PPB1 |
| F13 | IO39RSB0 | H5 | IO167NPB3 | J19 | IO66NDB1 |
| F14 | IO44RSB0 | H6 | IO172NDB3 | J20 | NC |
| F15 | GBC0/IO54RSB0 | H7 | IO169NDB3 | J21 | IO68PDB1 |
| F16 | IO51RSB0 | H8 | VMV0 | J22 | IO68NDB1 |
| F17 | VMV0 | H9 | V _{CC} B0 | K1 | IO157PDB3 |
| F18 | IO61NPB1 | H10 | V _{CC} B0 | K2 | IO157NDB3 |
| F19 | IO63PDB1 | H11 | IO25RSB0 | K3 | NC |
| F20 | NC | H12 | IO31RSB0 | K4 | IO165NDB3 |
| F21 | NC | H13 | V _{CC} B0 | K5 | IO165PDB3 |
| F22 | NC | H14 | V _{CC} B0 | K6 | IO168PPB3 |
| G1 | IO170NDB3 | H15 | VMV1 | K7 | GFC1/IO164PPB3 |
| G2 | IO170PDB3 | H16 | GBC2/IO62PDB1 | K8 | V _{CC} B3 |
| G3 | NC | H17 | IO67PPB1 | K9 | V _{CC} |
| G4 | IO171NDB3 | H18 | IO64PPB1 | K10 | GND |
| G5 | IO171PDB3 | H19 | IO66PDB1 | K11 | GND |
| G6 | GAC2/IO172PDB3 | H20 | V _{CC} | K12 | GND |
| G7 | IO06RSB0 | H21 | NC | K13 | GND |
| G8 | GNDQ | H22 | NC | K14 | V _{CC} |
| G9 | IO10RSB0 | J1 | NC | K15 | V _{CC} B1 |
| G10 | IO19RSB0 | J2 | NC | K16 | GCC1/IO69PPB1 |
| G11 | IO26RSB0 | J3 | NC | K17 | IO65NPB1 |
| G12 | IO30RSB0 | J4 | IO166NDB3 | K18 | IO75PDB1 |

| 484-Pin FBGA | |
|--------------|---------------------|
| Pin Number | A3P600 Function |
| K19 | IO75NDB1 |
| K20 | NC |
| K21 | IO76NDB1 |
| K22 | IO76PDB1 |
| L1 | NC |
| L2 | IO155PDB3 |
| L3 | NC |
| L4 | GFB0/IO163NPB3 |
| L5 | GFA0/IO162NDB3 |
| L6 | GFB1/IO163PPB3 |
| L7 | V _{COMPLF} |
| L8 | GFC0/IO164NPB3 |
| L9 | V _{CC} |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | V _{CC} |
| L15 | GCC0/IO69NPB1 |
| L16 | GCB1/IO70PPB1 |
| L17 | GCA0/IO71NPB1 |
| L18 | IO67NPB1 |
| L19 | GCB0/IO70NPB1 |
| L20 | IO77PDB1 |
| L21 | IO77NDB1 |
| L22 | IO78NPB1 |
| M1 | NC |
| M2 | IO155NDB3 |
| M3 | IO158NPB3 |
| M4 | GFA2/IO161PPB3 |
| M5 | GFA1/IO162PDB3 |
| M6 | V _{CCPLF} |
| M7 | IO160NDB3 |
| M8 | GFB2/IO160PDB3 |
| M9 | V _{CC} |
| M10 | GND |

| 484-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P600 Function |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | V _{CC} |
| M15 | GCB2/IO73PPB1 |
| M16 | GCA1/IO71PPB1 |
| M17 | GCC2/IO74PPB1 |
| M18 | IO80PPB1 |
| M19 | GCA2/IO72PDB1 |
| M20 | IO79PPB1 |
| M21 | IO78PPB1 |
| M22 | NC |
| N1 | IO154NDB3 |
| N2 | IO154PDB3 |
| N3 | NC |
| N4 | GFC2/IO159PDB3 |
| N5 | IO161NPB3 |
| N6 | IO156PPB3 |
| N7 | IO129RSB2 |
| N8 | V _{CCB3} |
| N9 | V _{CC} |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | V _{CC} |
| N15 | V _{CCB1} |
| N16 | IO73NPB1 |
| N17 | IO80NPB1 |
| N18 | IO74NPB1 |
| N19 | IO72NDB1 |
| N20 | NC |
| N21 | IO79NPB1 |
| N22 | NC |
| P1 | NC |
| P2 | IO153PDB3 |

| 484-Pin FBGA | |
|--------------|-------------------|
| Pin Number | A3P600 Function |
| P3 | IO153NDB3 |
| P4 | IO159NDB3 |
| P5 | IO156NPB3 |
| P6 | IO151PPB3 |
| P7 | IO158PPB3 |
| P8 | V _{CCB3} |
| P9 | GND |
| P10 | V _{CC} |
| P11 | V _{CC} |
| P12 | V _{CC} |
| P13 | V _{CC} |
| P14 | GND |
| P15 | V _{CCB1} |
| P16 | GDB0/IO87NPB1 |
| P17 | IO85NDB1 |
| P18 | IO85PDB1 |
| P19 | IO84PDB1 |
| P20 | NC |
| P21 | IO81PDB1 |
| P22 | NC |
| R1 | NC |
| R2 | NC |
| R3 | V _{CC} |
| R4 | IO150PDB3 |
| R5 | IO151NPB3 |
| R6 | IO147NPB3 |
| R7 | GEC0/IO146NPB3 |
| R8 | VMV3 |
| R9 | V _{CCB2} |
| R10 | V _{CCB2} |
| R11 | IO117RSB2 |
| R12 | IO110RSB2 |
| R13 | V _{CCB2} |
| R14 | V _{CCB2} |
| R15 | VMV2 |
| R16 | IO94RSB2 |

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|-------------------|--------------|-------------------|--------------|--------------------|
| Pin Number | A3P600 Function | Pin Number | A3P600 Function | Pin Number | A3P600 Function |
| R17 | GDB1/IO87PPB1 | U9 | IO131RSB2 | W1 | NC |
| R18 | GDC1/IO86PDB1 | U10 | IO124RSB2 | W2 | IO148PDB3 |
| R19 | IO84NDB1 | U11 | IO119RSB2 | W3 | NC |
| R20 | V _{CC} | U12 | IO107RSB2 | W4 | GND |
| R21 | IO81NDB1 | U13 | IO104RSB2 | W5 | IO137RSB2 |
| R22 | IO82PDB1 | U14 | IO97RSB2 | W6 | GEB2/IO142RSB2 |
| T1 | IO152PDB3 | U15 | VMV1 | W7 | IO134RSB2 |
| T2 | IO152NDB3 | U16 | TCK | W8 | IO125RSB2 |
| T3 | NC | U17 | V _{PUMP} | W9 | IO123RSB2 |
| T4 | IO150NDB3 | U18 | TRST | W10 | IO118RSB2 |
| T5 | IO147PPB3 | U19 | GDA0/IO88NDB1 | W11 | IO115RSB2 |
| T6 | GEC1/IO146PPB3 | U20 | NC | W12 | IO111RSB2 |
| T7 | IO140RSB2 | U21 | IO83NDB1 | W13 | IO106RSB2 |
| T8 | GNDQ | U22 | NC | W14 | IO102RSB2 |
| T9 | GEA2/IO143RSB2 | V1 | NC | W15 | GDC2/IO91RSB2 |
| T10 | IO126RSB2 | V2 | NC | W16 | IO93RSB2 |
| T11 | IO120RSB2 | V3 | GND | W17 | GDA2/IO89RSB2 |
| T12 | IO108RSB2 | V4 | GEA1/IO144PDB3 | W18 | TMS |
| T13 | IO103RSB2 | V5 | GEA0/IO144NDB3 | W19 | GND |
| T14 | IO99RSB2 | V6 | IO139RSB2 | W20 | NC |
| T15 | GNDQ | V7 | GEC2/IO141RSB2 | W21 | NC |
| T16 | IO92RSB2 | V8 | IO132RSB2 | W22 | NC |
| T17 | V _{JTAG} | V9 | IO127RSB2 | Y1 | V _{CC} B3 |
| T18 | GDC0/IO86NDB1 | V10 | IO121RSB2 | Y2 | IO148NDB3 |
| T19 | GDA1/IO88PDB1 | V11 | IO114RSB2 | Y3 | NC |
| T20 | NC | V12 | IO109RSB2 | Y4 | NC |
| T21 | IO83PDB1 | V13 | IO105RSB2 | Y5 | GND |
| T22 | IO82NDB1 | V14 | IO98RSB2 | Y6 | NC |
| U1 | IO149PDB3 | V15 | IO96RSB2 | Y7 | NC |
| U2 | IO149NDB3 | V16 | GDB2/IO90RSB2 | Y8 | V _{CC} |
| U3 | NC | V17 | TDI | Y9 | V _{CC} |
| U4 | GEB1/IO145PDB3 | V18 | GNDQ | Y10 | NC |
| U5 | GEB0/IO145NDB3 | V19 | TDO | Y11 | NC |
| U6 | VMV2 | V20 | GND | Y12 | NC |
| U7 | IO138RSB2 | V21 | NC | Y13 | NC |
| U8 | IO136RSB2 | V22 | NC | Y14 | V _{CC} |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P600 Function |
| Y15 | V _{CC} |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | V _{CC} B1 |
| AA1 | GND |
| AA2 | V _{CC} B3 |
| AA3 | NC |
| AA4 | NC |
| AA5 | NC |
| AA6 | IO135RSB2 |
| AA7 | IO133RSB2 |
| AA8 | NC |
| AA9 | NC |
| AA10 | NC |
| AA11 | NC |
| AA12 | NC |
| AA13 | NC |
| AA14 | NC |
| AA15 | NC |
| AA16 | IO101RSB2 |
| AA17 | NC |
| AA18 | NC |
| AA19 | NC |
| AA20 | NC |
| AA21 | V _{CC} B1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | V _{CC} B2 |
| AB4 | NC |
| AB5 | NC |
| AB6 | IO130RSB2 |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P600 Function |
| AB7 | IO128RSB2 |
| AB8 | IO122RSB2 |
| AB9 | IO116RSB2 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO113RSB2 |
| AB13 | IO112RSB2 |
| AB14 | NC |
| AB15 | NC |
| AB16 | IO100RSB2 |
| AB17 | IO95RSB2 |
| AB18 | NC |
| AB19 | NC |
| AB20 | V _{CC} B2 |
| AB21 | GND |
| AB22 | GND |

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|--------------------|--------------|--------------------|--------------|------------------|
| Pin Number | A3P1000 Function | Pin Number | A3P1000 Function | Pin Number | A3P1000 Function |
| A1 | GND | B15 | IO63RSB0 | D7 | GAB0/IO02RSB0 |
| A2 | GND | B16 | IO66RSB0 | D8 | IO16RSB0 |
| A3 | V _{CC} B0 | B17 | IO68RSB0 | D9 | IO22RSB0 |
| A4 | IO07RSB0 | B18 | IO70RSB0 | D10 | IO28RSB0 |
| A5 | IO09RSB0 | B19 | NC | D11 | IO35RSB0 |
| A6 | IO13RSB0 | B20 | NC | D12 | IO45RSB0 |
| A7 | IO18RSB0 | B21 | V _{CC} B1 | D13 | IO50RSB0 |
| A8 | IO20RSB0 | B22 | GND | D14 | IO55RSB0 |
| A9 | IO26RSB0 | C1 | V _{CC} B3 | D15 | IO61RSB0 |
| A10 | IO32RSB0 | C2 | IO220PDB3 | D16 | GBB1/IO75RSB0 |
| A11 | IO40RSB0 | C3 | NC | D17 | GBA0/IO76RSB0 |
| A12 | IO41RSB0 | C4 | NC | D18 | GBA1/IO77RSB0 |
| A13 | IO53RSB0 | C5 | GND | D19 | GND |
| A14 | IO59RSB0 | C6 | IO10RSB0 | D20 | NC |
| A15 | IO64RSB0 | C7 | IO14RSB0 | D21 | NC |
| A16 | IO65RSB0 | C8 | V _{CC} | D22 | NC |
| A17 | IO67RSB0 | C9 | V _{CC} | E1 | IO219NDB3 |
| A18 | IO69RSB0 | C10 | IO30RSB0 | E2 | NC |
| A19 | NC | C11 | IO37RSB0 | E3 | GND |
| A20 | V _{CC} B0 | C12 | IO43RSB0 | E4 | GAB2/IO224PDB3 |
| A21 | GND | C13 | NC | E5 | GAA2/IO225PDB3 |
| A22 | GND | C14 | V _{CC} | E6 | GNDQ |
| B1 | GND | C15 | V _{CC} | E7 | GAB1/IO03RSB0 |
| B2 | V _{CC} B3 | C16 | NC | E8 | IO17RSB0 |
| B3 | NC | C17 | NC | E9 | IO21RSB0 |
| B4 | IO06RSB0 | C18 | GND | E10 | IO27RSB0 |
| B5 | IO08RSB0 | C19 | NC | E11 | IO34RSB0 |
| B6 | IO12RSB0 | C20 | NC | E12 | IO44RSB0 |
| B7 | IO15RSB0 | C21 | NC | E13 | IO51RSB0 |
| B8 | IO19RSB0 | C22 | V _{CC} B1 | E14 | IO57RSB0 |
| B9 | IO24RSB0 | D1 | IO219PDB3 | E15 | GBC1/IO73RSB0 |
| B10 | IO31RSB0 | D2 | IO220NDB3 | E16 | GBB0/IO74RSB0 |
| B11 | IO39RSB0 | D3 | NC | E17 | IO71RSB0 |
| B12 | IO48RSB0 | D4 | GND | E18 | GBA2/IO78PDB1 |
| B13 | IO54RSB0 | D5 | GAA0/IO00RSB0 | E19 | IO81PDB1 |
| B14 | IO58RSB0 | D6 | GAA1/IO01RSB0 | E20 | GND |

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P1000 Function | Pin Number | A3P1000 Function | Pin Number | A3P1000 Function |
| E21 | NC | G13 | IO52RSB0 | J5 | IO218NDB3 |
| E22 | IO84PDB1 | G14 | IO60RSB0 | J6 | IO216PDB3 |
| F1 | NC | G15 | GNDQ | J7 | IO216NDB3 |
| F2 | IO215PDB3 | G16 | IO80NDB1 | J8 | V _{CC} B3 |
| F3 | IO215NDB3 | G17 | GBB2/IO79PDB1 | J9 | GND |
| F4 | IO224NDB3 | G18 | IO79NDB1 | J10 | V _{CC} |
| F5 | IO225NDB3 | G19 | IO82NPB1 | J11 | V _{CC} |
| F6 | VMV3 | G20 | IO85PDB1 | J12 | V _{CC} |
| F7 | IO11RSB0 | G21 | IO85NDB1 | J13 | V _{CC} |
| F8 | GAC0/IO04RSB0 | G22 | NC | J14 | GND |
| F9 | GAC1/IO05RSB0 | H1 | NC | J15 | V _{CC} B1 |
| F10 | IO25RSB0 | H2 | NC | J16 | IO83NPB1 |
| F11 | IO36RSB0 | H3 | V _{CC} | J17 | IO86NPB1 |
| F12 | IO42RSB0 | H4 | IO217PDB3 | J18 | IO90PPB1 |
| F13 | IO49RSB0 | H5 | IO218PDB3 | J19 | IO87NDB1 |
| F14 | IO56RSB0 | H6 | IO221NDB3 | J20 | NC |
| F15 | GBC0/IO72RSB0 | H7 | IO221PDB3 | J21 | IO89PDB1 |
| F16 | IO62RSB0 | H8 | VMV0 | J22 | IO89NDB1 |
| F17 | VMV0 | H9 | V _{CC} B0 | K1 | IO211PDB3 |
| F18 | IO78NDB1 | H10 | V _{CC} B0 | K2 | IO211NDB3 |
| F19 | IO81NDB1 | H11 | IO38RSB0 | K3 | NC |
| F20 | IO82PPB1 | H12 | IO47RSB0 | K4 | IO210PPB3 |
| F21 | NC | H13 | V _{CC} B0 | K5 | IO213NDB3 |
| F22 | IO84NDB1 | H14 | V _{CC} B0 | K6 | IO213PDB3 |
| G1 | IO214NDB3 | H15 | VMV1 | K7 | GFC1/IO209PPB3 |
| G2 | IO214PDB3 | H16 | GBC2/IO80PDB1 | K8 | V _{CC} B3 |
| G3 | NC | H17 | IO83PPB1 | K9 | V _{CC} |
| G4 | IO222NDB3 | H18 | IO86PPB1 | K10 | GND |
| G5 | IO222PDB3 | H19 | IO87PDB1 | K11 | GND |
| G6 | GAC2/IO223PDB3 | H20 | V _{CC} | K12 | GND |
| G7 | IO223NDB3 | H21 | NC | K13 | GND |
| G8 | GNDQ | H22 | NC | K14 | V _{CC} |
| G9 | IO23RSB0 | J1 | IO212NDB3 | K15 | V _{CC} B1 |
| G10 | IO29RSB0 | J2 | IO212PDB3 | K16 | GCC1/IO91PPB1 |
| G11 | IO33RSB0 | J3 | NC | K17 | IO90NPB1 |
| G12 | IO46RSB0 | J4 | IO217NDB3 | K18 | IO88PDB1 |

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|------------------------|--------------|--------------------|--------------|--------------------|
| Pin Number | A3P1000 Function | Pin Number | A3P1000 Function | Pin Number | A3P1000 Function |
| K19 | IO88NDB1 | M11 | GND | P3 | IO199NDB3 |
| K20 | IO94NPB1 | M12 | GND | P4 | IO202NDB3 |
| K21 | IO98NDB1 | M13 | GND | P5 | IO202PDB3 |
| K22 | IO98PDB1 | M14 | V _{CC} | P6 | IO196PPB3 |
| L1 | NC | M15 | GCB2/IO95PPB1 | P7 | IO193PPB3 |
| L2 | IO200PDB3 | M16 | GCA1/IO93PPB1 | P8 | V _{CC} B3 |
| L3 | IO210NPB3 | M17 | GCC2/IO96PPB1 | P9 | GND |
| L4 | GFB0/IO208NPB3 | M18 | IO100PPB1 | P10 | V _{CC} |
| L5 | GFA0/IO207NDB3 | M19 | GCA2/IO94PPB1 | P11 | V _{CC} |
| L6 | GFB1/IO208PPB3 | M20 | IO101PPB1 | P12 | V _{CC} |
| L7 | V _{CC} COMPLF | M21 | IO99PPB1 | P13 | V _{CC} |
| L8 | GFC0/IO209NPB3 | M22 | NC | P14 | GND |
| L9 | V _{CC} | N1 | IO201NDB3 | P15 | V _{CC} B1 |
| L10 | GND | N2 | IO201PDB3 | P16 | GDB0/IO112NPB1 |
| L11 | GND | N3 | NC | P17 | IO106NDB1 |
| L12 | GND | N4 | GFC2/IO204PDB3 | P18 | IO106PDB1 |
| L13 | GND | N5 | IO204NDB3 | P19 | IO107PDB1 |
| L14 | V _{CC} | N6 | IO203NDB3 | P20 | NC |
| L15 | GCC0/IO91NPB1 | N7 | IO203PDB3 | P21 | IO104PDB1 |
| L16 | GCB1/IO92PPB1 | N8 | V _{CC} B3 | P22 | IO103NDB1 |
| L17 | GCA0/IO93NPB1 | N9 | V _{CC} | R1 | NC |
| L18 | IO96NPB1 | N10 | GND | R2 | IO197PPB3 |
| L19 | GCB0/IO92NPB1 | N11 | GND | R3 | V _{CC} |
| L20 | IO97PDB1 | N12 | GND | R4 | IO197NPB3 |
| L21 | IO97NDB1 | N13 | GND | R5 | IO196NPB3 |
| L22 | IO99NPB1 | N14 | V _{CC} | R6 | IO193NPB3 |
| M1 | NC | N15 | V _{CC} B1 | R7 | GEC0/IO190NPB3 |
| M2 | IO200NDB3 | N16 | IO95NPB1 | R8 | VMV3 |
| M3 | IO206NDB3 | N17 | IO100NPB1 | R9 | V _{CC} B2 |
| M4 | GFA2/IO206PDB3 | N18 | IO102NDB1 | R10 | V _{CC} B2 |
| M5 | GFA1/IO207PDB3 | N19 | IO102PDB1 | R11 | IO147RSB2 |
| M6 | V _{CC} PLF | N20 | NC | R12 | IO136RSB2 |
| M7 | IO205NDB3 | N21 | IO101NPB1 | R13 | V _{CC} B2 |
| M8 | GFB2/IO205PDB3 | N22 | IO103PDB1 | R14 | V _{CC} B2 |
| M9 | V _{CC} | P1 | NC | R15 | VMV2 |
| M10 | GND | P2 | IO199PDB3 | R16 | IO110NDB1 |

| 484-Pin FBGA | | 484-Pin FBGA | | 484-Pin FBGA | |
|--------------|-------------------|--------------|-------------------|--------------|--------------------|
| Pin Number | A3P1000 Function | Pin Number | A3P1000 Function | Pin Number | A3P1000 Function |
| R17 | GDB1/IO112PPB1 | U9 | IO165RSB2 | W1 | NC |
| R18 | GDC1/IO111PDB1 | U10 | IO159RSB2 | W2 | IO191PDB3 |
| R19 | IO107NDB1 | U11 | IO151RSB2 | W3 | NC |
| R20 | V _{CC} | U12 | IO137RSB2 | W4 | GND |
| R21 | IO104NDB1 | U13 | IO134RSB2 | W5 | IO183RSB2 |
| R22 | IO105PDB1 | U14 | IO128RSB2 | W6 | GEB2/IO186RSB2 |
| T1 | IO198PDB3 | U15 | VMV1 | W7 | IO172RSB2 |
| T2 | IO198NDB3 | U16 | TCK | W8 | IO170RSB2 |
| T3 | NC | U17 | V _{PUMP} | W9 | IO164RSB2 |
| T4 | IO194PPB3 | U18 | TRST | W10 | IO158RSB2 |
| T5 | IO192PPB3 | U19 | GDA0/IO113NDB1 | W11 | IO153RSB2 |
| T6 | GEC1/IO190PPB3 | U20 | NC | W12 | IO142RSB2 |
| T7 | IO192NPB3 | U21 | IO108NDB1 | W13 | IO135RSB2 |
| T8 | GNDQ | U22 | IO109PDB1 | W14 | IO130RSB2 |
| T9 | GEA2/IO187RSB2 | V1 | NC | W15 | GDC2/IO116RSB2 |
| T10 | IO161RSB2 | V2 | NC | W16 | IO120RSB2 |
| T11 | IO155RSB2 | V3 | GND | W17 | GDA2/IO114RSB2 |
| T12 | IO141RSB2 | V4 | GEA1/IO188PDB3 | W18 | TMS |
| T13 | IO129RSB2 | V5 | GEA0/IO188NDB3 | W19 | GND |
| T14 | IO124RSB2 | V6 | IO184RSB2 | W20 | NC |
| T15 | GNDQ | V7 | GEC2/IO185RSB2 | W21 | NC |
| T16 | IO110PDB1 | V8 | IO168RSB2 | W22 | NC |
| T17 | V _{JTAG} | V9 | IO163RSB2 | Y1 | V _{CC} B3 |
| T18 | GDC0/IO111NDB1 | V10 | IO157RSB2 | Y2 | IO191NDB3 |
| T19 | GDA1/IO113PDB1 | V11 | IO149RSB2 | Y3 | NC |
| T20 | NC | V12 | IO143RSB2 | Y4 | IO182RSB2 |
| T21 | IO108PDB1 | V13 | IO138RSB2 | Y5 | GND |
| T22 | IO105NDB1 | V14 | IO131RSB2 | Y6 | IO177RSB2 |
| U1 | IO195PDB3 | V15 | IO125RSB2 | Y7 | IO174RSB2 |
| U2 | IO195NDB3 | V16 | GDB2/IO115RSB2 | Y8 | V _{CC} |
| U3 | IO194NPB3 | V17 | TDI | Y9 | V _{CC} |
| U4 | GEB1/IO189PDB3 | V18 | GNDQ | Y10 | IO154RSB2 |
| U5 | GEB0/IO189NDB3 | V19 | TDO | Y11 | IO148RSB2 |
| U6 | VMV2 | V20 | GND | Y12 | IO140RSB2 |
| U7 | IO179RSB2 | V21 | NC | Y13 | NC |
| U8 | IO171RSB2 | V22 | IO109NDB1 | Y14 | V _{CC} |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P1000 Function |
| Y15 | V _{CC} |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | V _{CC} B1 |
| AA1 | GND |
| AA2 | V _{CC} B3 |
| AA3 | NC |
| AA4 | IO181RSB2 |
| AA5 | IO178RSB2 |
| AA6 | IO175RSB2 |
| AA7 | IO169RSB2 |
| AA8 | IO166RSB2 |
| AA9 | IO160RSB2 |
| AA10 | IO152RSB2 |
| AA11 | IO146RSB2 |
| AA12 | IO139RSB2 |
| AA13 | IO133RSB2 |
| AA14 | NC |
| AA15 | NC |
| AA16 | IO122RSB2 |
| AA17 | IO119RSB2 |
| AA18 | IO117RSB2 |
| AA19 | NC |
| AA20 | NC |
| AA21 | V _{CC} B1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | V _{CC} B2 |
| AB4 | IO180RSB2 |
| AB5 | IO176RSB2 |
| AB6 | IO173RSB2 |

| 484-Pin FBGA | |
|--------------|--------------------|
| Pin Number | A3P1000 Function |
| AB7 | IO167RSB2 |
| AB8 | IO162RSB2 |
| AB9 | IO156RSB2 |
| AB10 | IO150RSB2 |
| AB11 | IO145RSB2 |
| AB12 | IO144RSB2 |
| AB13 | IO132RSB2 |
| AB14 | IO127RSB2 |
| AB15 | IO126RSB2 |
| AB16 | IO123RSB2 |
| AB17 | IO121RSB2 |
| AB18 | IO118RSB2 |
| AB19 | NC |
| AB20 | V _{CC} B2 |
| AB21 | GND |
| AB22 | GND |

Part Number and Revision Date

Part Number 51700097-003-4
Revised December 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v1.4) | Page |
|--------------------------------|--|-------------|
| v1.3 (June 2008) | The "48-Pin QFP" table is new. | 3-2 |
| | The "68-Pin QFN" table is new. | 3-5 |
| v1.2 (February 2008) | Pin numbers were added to the "48-Pin QFN" package diagram. Note 2 was added below the diagram. | 3-1 |
| | The "132-Pin QFN" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new. | 3-6 |
| v1.1 (January 2008) | The "48-Pin QFN" section is new. | 3-1 |
| v1.0 (January 2008) | In the "100-Pin VQFP" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0. | 3-16 |
| v2.2 (July 2007) | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is v1.0. | N/A |
| v2.0 (April 2007) | The following pin tables were updated for A3P600: "208-Pin PQFP", "256-Pin FBGA", and "484-Pin FBGA". The "144-Pin FBGA" table for A3P600 is new. | 4-27 – 4-63 |
| Advance v0.7 (January 2007) | Notes were added to the package diagrams identifying if they were top or bottom view. | N/A |
| | The A3P030 "132-Pin QFN" table is new. | 4-2 |
| | The A3P060 "132-Pin QFN" table is new. | 4-4 |
| | The A3P125 "132-Pin QFN" table is new. | 4-6 |
| | The A3P250 "132-Pin QFN" table is new. | 4-8 |
| | The A3P030 "100-Pin VQFP" table is new. | 4-11 |

| Previous Version | Changes in Current Version (v1.4) | Page |
|--------------------------------|--|------|
| Advance v0.5 (January 2006) | The A3P060 "100-Pin VQFP" pin table was updated. | 4-13 |
| | The A3P125 "100-Pin VQFP" pin table was updated. | 4-13 |
| | The A3P060 "144-Pin TQFP" pin table was updated. | 4-16 |
| | The A3P125 "144-Pin TQFP" pin table was updated. | 4-18 |
| | The A3P125 "208-Pin PQFP" pin table was updated. | 4-21 |
| | The A3P400 "208-Pin PQFP" pin table was updated. | 4-25 |
| | The A3P060 "144-Pin FBGA" pin table was updated. | 4-32 |
| | The A3P125 "144-Pin FBGA" pin table is new. | 4-34 |
| | The A3P400 "144-Pin FBGA" is new. | 4-38 |
| | The A3P400 "256-Pin FBGA" was updated. | 4-48 |
| | The A3P1000 "256-Pin FBGA" was updated. | 4-54 |
| | The A3P400 "484-Pin FBGA" was updated. | 4-58 |
| | The A3P1000 "484-Pin FBGA" was updated. | 4-68 |
| Advance v0.2 (continued) | The A3P250 "100-Pin VQFP*" pin table was updated. | 4-14 |
| | The A3P250 "208-Pin PQFP*" pin table was updated. | 4-23 |
| | The A3P1000 "208-Pin PQFP*" pin table was updated. | 4-29 |
| | The A3P250 "144-Pin FBGA*" pin table was updated. | 4-36 |
| | The A3P1000 "144-Pin FBGA*" pin table was updated. | 4-32 |
| | The A3P250 "256-Pin FBGA*" pin table was updated. | 4-45 |
| | The A3P1000 "256-Pin FBGA*" pin table was updated. | 4-54 |
| | The A3P1000 "484-Pin FBGA*" pin table was updated. | 4-68 |

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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