## Document Title

**4 Mbit CMOS 3.3 Volt-only Low Pin Count Flash Memory**

## Revision History

| Rev. No. | History | Issue Date | Remark |
|---|---|---|---|
| 0.0 | Initial issue | March 3, 2006 | Preliminary |
| 0.1 | Correct the part number from A49LF040A to A49LF040AT on page 29 | March 28, 2006 | |

AMIC

# A49LF040A

## Preliminary — 4 Mbit CMOS 3.3Volt-only Low Pin Count Flash Memory

### FEATURES

- **Single Power Supply Operation**
  - Low voltage range: 3.0 V - 3.6 V for Read and Write Operations
- **Standard Intel Low Pin Count Interface**
  - Read compatible to Intel® Low Pin Count (LPC) interface
- **Memory Configuration**
  - 512K x 8 (4 Mbit)
- **Block Architecture**
  - 4Mbit: eight uniform 64KByte blocks
  - Supports full chip erase for Address/Address Multiplexed (A/A Mux) mode
- **Automatic Erase and Program Operation**
  - Embedded Byte Program and Block/Chip Erase algorithms
  - Typical 10 µs/byte programming time
  - Typical 1s block erase time
- **Two Operational Modes**
  - Low Pin Count Interface (LPC) Mode for in-system operation
  - Address/Address Multiplexed (A/A Mux) Interface Mode for programming equipment
- **Low Pin Count (LPC) Mode**
  - 33 MHz synchronous operation with PCI bus
  - 5-signal communication interface for in-system read and write operations
  - Standard SDP Command Set
  - $\overline{\text{Data}}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$) features
  - Block Locking Register for all blocks
  - 4 ID pins for multi-chip selection
  - 5 GPI pins for General Purpose Input Register
  - $\overline{\text{TBL}}$ pin for hardware write protection to Boot Block
  - $\overline{\text{WP}}$ pin for hardware write protection to whole memory array except Boot Block
- **Address/Address Multiplexed (A/A Mux) Mode**
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast programming on EPROM programmers
  - Standard SDP Command Set
  - $\overline{\text{Data}}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$) features
- **Lower Power Consumption**
  - Typical 12mA active read current
  - Typical 24mA program/erase current
- **High Product Endurance**
  - Guarantee 100,000 program/erase cycles for each block
  - Minimum 20 years data retention
- **Compatible Pin-out and Packaging**
  - 32-pin (8 mm x 14 mm) TSOP (TYPE I)
  - 32-pin PLCC
  - Optional Pb-free (Lead-free) package
  - All Pb-free (Lead-free) products are RoHS compliant

### General Description

The A49LF040A flash memory device is designed to be read-compatible with the Intel Low Pin Count (LPC) Interface Specification 1.1. This device is designed to use a single low voltage, range from 3.0 Volt to 3.6 Volt power supply to perform in-system or off-system read and write operations. It provides protection for the storage and update of code and data in addition to adding system design flexibility through five general-purpose inputs. Two interface modes are supported by the A49LF040A: Low Pin Count (LPC) Interface mode for In-System programming and Address/Address Multiplexed (A/A Mux) mode for fast factory programming of PC-BIOS applications.

The memory is divided into eight uniform 64Kbyte blocks that can be erased independently without affecting the data in other blocks. Blocks also can be protected individually to prevent accidental Program or Erase commands from modifying the memory. The boot block can be write protected by a hardware method controlled by the $\overline{\text{TBL}}$ pin or a register-based protection turned on/off by the Block Locking Registers (LPC mode only). The rest of blocks except boot block in the device also can be write protected by $\overline{\text{WP}}$ pin or Block Locking Registers (LPC mode only). The Program and Erase operations are executed by issuing the Program/Erase commands into the command interface by which activating the internal control logic to automatically process the Program/Erase procedures. The device can be programmed on a byte-by-byte basis after performing the Erase operation. In addition to the Block Erase operation, the Chip Erase feature is provided in A/A Mux mode that allows the whole memory to be erased in one single Erase operation. The A49LF040A provides the status detection such as $\overline{\text{Data}}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$) Functions in both FWH/LPC and A/A Mux modes. The process or completion of Program and Erase operations can be detected by reading the status bits.

The A49LF040A is offered in 32-lead TSOP and 32-lead PLCC packages with optional environmental friendly lead-free package. See Figures 1 and 2 for pin assignments and Table 1 for pin descriptions.

## Pin Configurations

Figure 1: Pin Assignments for 32-Lead PLCC

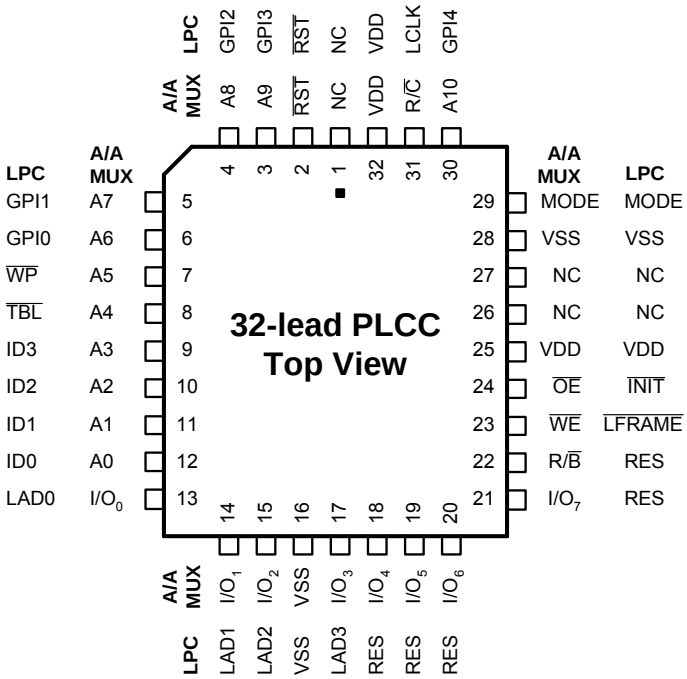
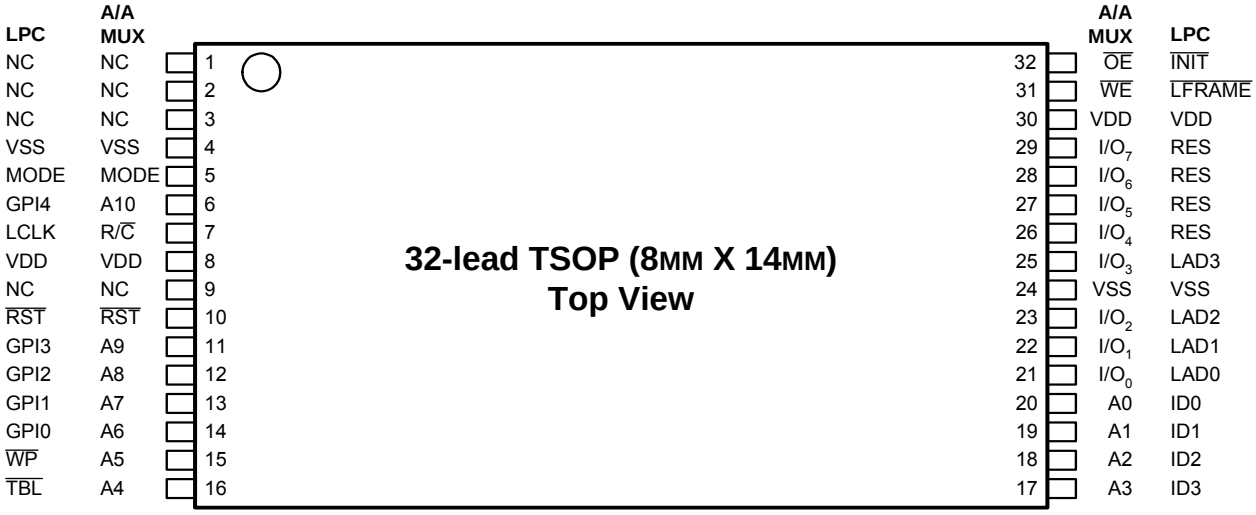



Figure 2: Pin Assignments for 32-Lead TSOP



## Block Diagram

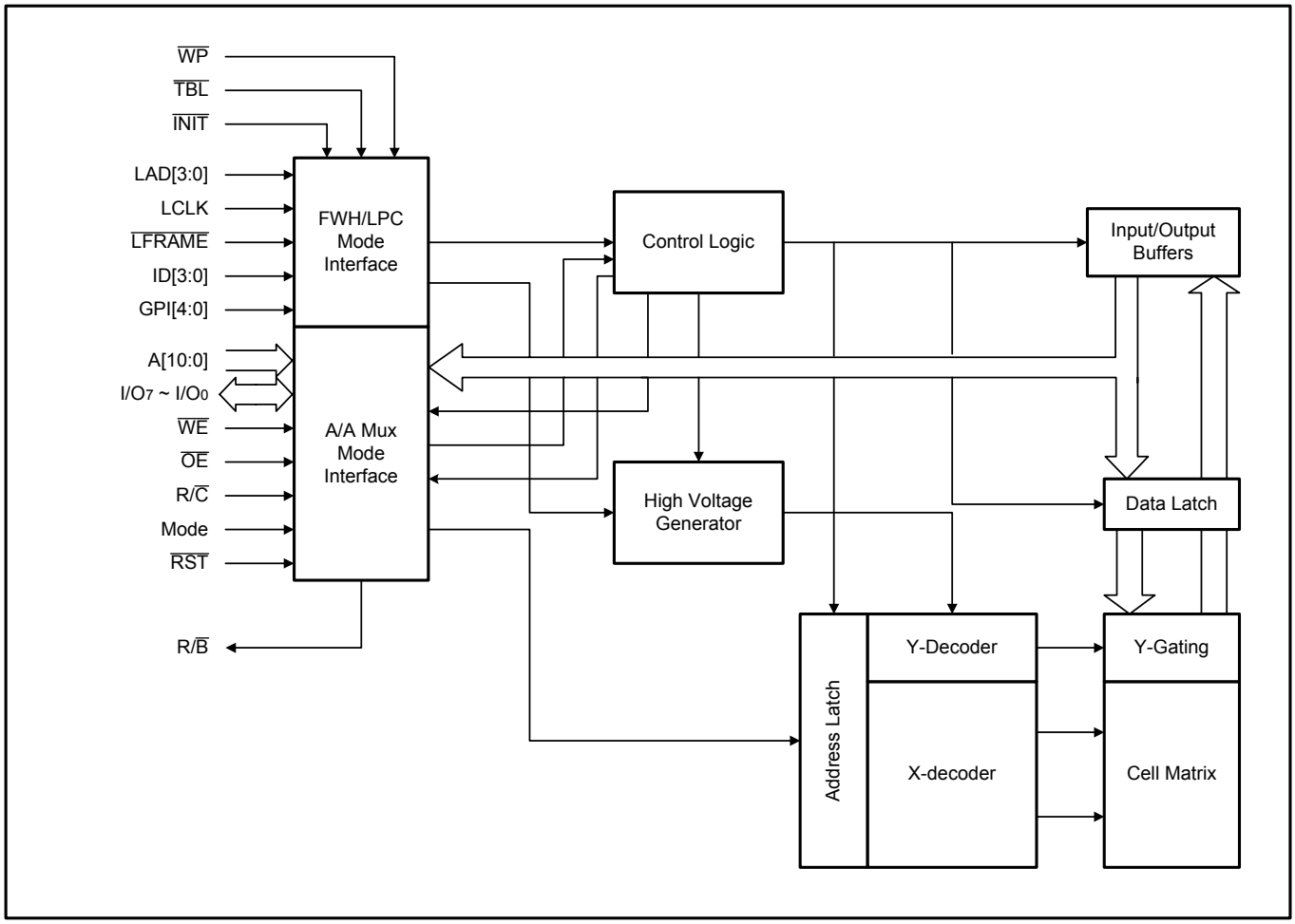


Table 1: Pin Description

| Symbol | Pin Name | Type | Interface | | Descriptions |
|---|---|---|---|---|---|
| | | | A/A Mux | LPC | |
| $A_{10}$-$A_0$ | Address | IN | X | | Inputs for addresses during Read and Write operations in A/A Mux mode. Row and column addresses are latched by R/$\overline{C}$ pin. |
| $I/O_7$-$I/O_0$ | Data | I/O | X | | To output data during Read cycle and receive input data during Write cycle in A/A Mux mode. The outputs are in tri-state when $\overline{OE}$ is high. |
| $\overline{OE}$ | Output Enable | IN | X | | To control the data output buffers. |
| $\overline{WE}$ | Write Enable | IN | X | | To control the Write operations. |
| MODE | Interface Mode Select | IN | X | X | To determine which interface is operational. When held high, A/A Mux mode is enabled and when held low, LPC mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin is internally pulled down with a resistor between 20-100 K ˜ |
| $\overline{INIT}$ | Initialize | IN | | X | This is the second reset pin for in-system use. $\overline{INIT}$ and $\overline{RST}$ pins are internally combined and initialize a device reset when driven low. |
| ID[3:0] | Identification Inputs | IN | | X | These four pins are part of the mechanism that allows multiple LPC devices to be attached to the same bus. To identify the component, the correct strapping of these pins must be set. The boot device must have ID[3:0]=0000 and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled down with a resistor between 20-100 KΩ. |
| GPI[4:0] | General Purpose Inputs | IN | | X | These individual inputs can be used for additional board flexibility. The state of these pins can be read immediately at boot, through LPC internal registers. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated. |
| $\overline{TBL}$ | Top Block Lock | IN | | X | To prevent any write operations to the Boot Block when driven low, regardless of the state of the block lock registers. When $\overline{TBL}$ is high it disables hardware write protection for the top Boot Block. This pin cannot be left unconnected. |
| LAD[3:0] | LPC Interface I/Os | I/O | | X | I/O Communications in LPC mode. |
| LCLK | Clock | IN | | X | To provide a clock input to the device. This pin is the same as that for the PCI clock and adheres to the PCI specifications. |
| $\overline{LFRAME}$ | Frame | IN | | X | To indicate start of a data transfer operation. $\overline{LFRAME}$ is also used to abort an LPC cycle in progress. |
| $\overline{RST}$ | Reset | IN | X | X | To reset the operation of the device |
| $\overline{WP}$ | Write Protect | IN | | X | When low, prevents any write operations to all but the highest addressable block. When $\overline{WP}$ is high it disables hardware write protection for these blocks. This pin cannot be left unconnected. |
| R/$\overline{C}$ | Row/Column Select | IN | X | | This pin determines whether the address pins are pointing to the row addresses or the column addresses in A/A Mux mode. |
| R/$\overline{B}$ | Ready/Busy | OUT | X | | This pin is used to determine if the device is busy in write operations. Valid only in A/A Mux mode. |
| RES | Reserved | | | X | Reserved. These pins must be left unconnected. |
| VDD | Power Supply | PWR | X | X | To provide power supply (3.0-3.6Volt). |
| VSS | Ground | PWR | X | X | Circuit ground. All VSS pins must be grounded. |
| NC | No Connection | | X | X | Unconnected pins. |

Notes: IN=Input, OUT=output, I/O=Input/Output, PWR=Power

### Absolute Maximum Ratings*

Temperature Under Bias . . . . . .. . . . -55°C to + 125°C
Storage Temperature . . . . . -65°C to + 125°C
D.C. Voltage on Any Pins with Respect to Ground (1)
. . . . . -0.5V to VDD + 0.5V
Package Power Dissipation Capability (Ta=25°C)
. . . . . -0.5V to VDD + 0.5V
Output Short Circuit Current (2) . . . . . 50mA

### Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VDD + 0.5V. During voltage transitions, input or I/O pins may overshoot to VDD + 2.0V for periods up to 20ns.
2. No more than one output is shorted at a time. Duration of the short circuit should not be greater than one second.

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specifications are not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Operating Ranges**
**Commercial (C) Devices**
Ambient Temperature ($T_A$) . . . . . 0°C to +85°C
**VDD Supply Voltages**
VDD for all devices . . . . . +3.0V to +3.6V
Operating ranges define those limits between which the functionally of the device is guaranteed.

## MODE SELECTION

The A49LF040A flash memory devices can operate in two distinct interface modes: the Low Pin Count Interface (LPC) mode and the Address/Address Multiplexed (A/A Mux) mode. The Mode pin is used to set the interface mode selection. If the Mode pin is set to logic High, the device is in A/A Mux mode; while if the Mode pin is set Low, the device is in the LPC mode. The Mode pin must be configured prior to device operation. The Mode pin is internally pulled down if the pin is not connected. In LPC mode, the device is configured to interface with its host using Intel's Low Pin Count proprietary protocol. Communication between Host and the A49LF040A occurs via the 4-bit I/O communication signals, LAD[3:0] and the $\overline{\text{LFRAME}}$ . In A/A Mux mode, the device is programmed via an 11-bit address $A_{10}$-$A_0$ and an 8-bit data $I/O_7$-$I/O_0$. The address inputs are multiplexed in row and column selected by control signal R/$\overline{C}$ pin. The column addresses are mapped to the higher internal addresses, and the row addresses are mapped to the lower internal addresses. See the Device Memory Maps in Figure 3 for address assignment.

## LPC MODE OPERATION

The LPC interface consists of four data signals (LAD[3:0]), one control signal ( $\overline{\text{LFRAME}}$ ) and a clock (LCLK). The data signals, control signal and clock comply with PCI specifications. Operations such as Memory Read and Memory Write use Intel LPC propriety protocol. JEDEC Standard SDP (Software Data Protection) Byte-Program and Block-Erase command sequences are incorporated into the LPC memory cycles. Chip-Erase command is only available in A/A Mux mode. The addresses and data are transferred through LAD[3:0] synchronized with the input clock LCLK during a LPC memory cycle. The pulse of $\overline{\text{LFRAME}}$ is inserted for at least one clock period to indicate the start of a LPC memory cycle. The address or data on LAD[3:0] is latched on the rising edge of LCLK. The device enters standby mode when $\overline{\text{LFRAME}}$ is high and no internal operation is in progress. The device is in ready mode when $\overline{\text{LFRAME}}$ is low and no activity is on the LPC bus.

### LPC Read Operation

LPC Read operations read from the memory cells or specific registers in the LPC device. A valid LPC Read operation starts when $\overline{\text{LFRAME}}$ is Low as LCLK rises and a START value "0000b" is on LAD[3:0] then the next nibble "010X" is on LAD[3:0]. Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for LPC Read operations. Refer to Table 2 for LPC Read Cycle Definition.

### LPC Write Operation

LPC Write operations write to the LPC Interface or LPC registers. A valid LPC Write operation starts when $\overline{\text{LFRAME}}$ is Low as LCLK rises and a START value "0000b" is on LAD[3:0] then the next nibble "011X" is on LAD[3:0]. Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for LPC Write operations. Refer to Table 3 for LPC write Cycle Definition.

### LPC Abort Operation

If $\overline{\text{LFRAME}}$ is driven low for one or more clock cycles during a LPC cycle, the cycle will be terminated and the device will wait for the ABORT command. The host may drive the LAD[3:0] with "1111b" (ABORT command) to return the device to Ready mode. If abort occurs during a Write operation such as checking the operation status with Data Polling ($I/O_7$) or Toggle Bit ($I/O_6$) pins, the read status cycle will be aborted but the internal write operation will not be affected. In this case, only the reset operation initiated by $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ pin can terminate the Write operation.

### Response To Invalid Fields

During LPC operations, the LPC will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is as follows:

Table 2: LPC Read Cycle

| Clock Cycle | Field Name | Field Contents LAD[3:0][1] | LAD[3:0] Direction | Comments |
|---|---|---|---|---|
| 1 | START | 0000 | IN | $\overline{\text{LFRAME}}$ must be active (low) for the part to respond. Only the last start field (before $\overline{\text{LFRAME}}$ transitioning high) should be recognized. |
| 2 | CYCTYPE + DIR | 010X | IN | Indicates the type of cycle. Bits 3:2 must be "01b" for memory cycle. Bit 1 indicates the type of transfer "0" for Read. Bit 0 is reserved. |
| 3-10 | ADDRESS | YYYY | IN | Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. See Table 4 for address bits definition and Table 5 for valid memory address range. |
| 11 | TAR0 | 1111 | IN Then Float | In this clock cycle, the host has driven the bus to all 1s and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 12 | TAR1 | 1111(float) | Float Then OUT | The A49LF040A takes control of the bus during this cycle. |
| 13 | SYNC | 0000 | OUT | The A49LF040A outputs the value "0000b" indicating that data will be available during the next clock cycle. |
| 14 | DATA | ZZZZ | OUT | This field is the least-significant nibble of the data byte. |
| 15 | DATA | ZZZZ | OUT | This field is the most-significant nibble of the data byte. |
| 16 | TAR0 | 1111 | OUT Then Float | In this clock cycle, the A49LF040A drives the bus to all '1's and then floats the bus. This is the first part of the bus "turnaround cycle". |
| 17 | TAR1 | 1111(float) | Float Then IN | Host resumes control of the bus during this cycle. |

1. Field contents are valid on the rising edge of the present clock cycle.

LPC Single-Byte Read Waveforms

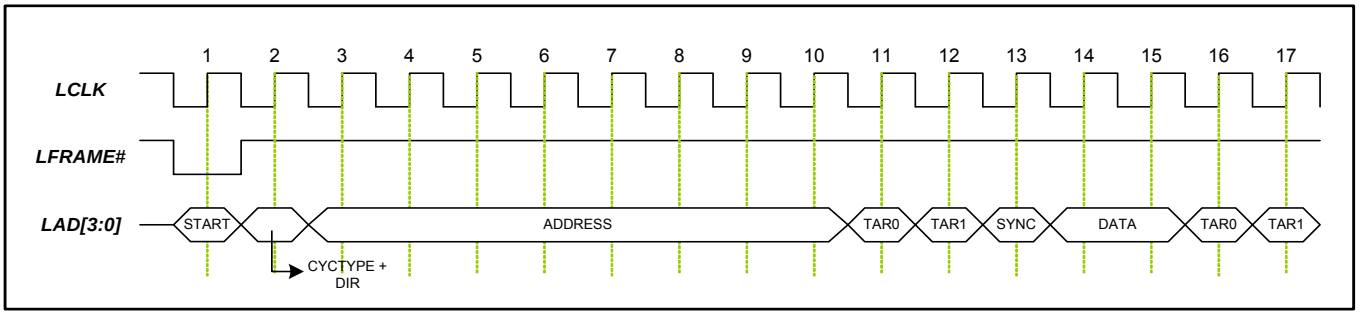
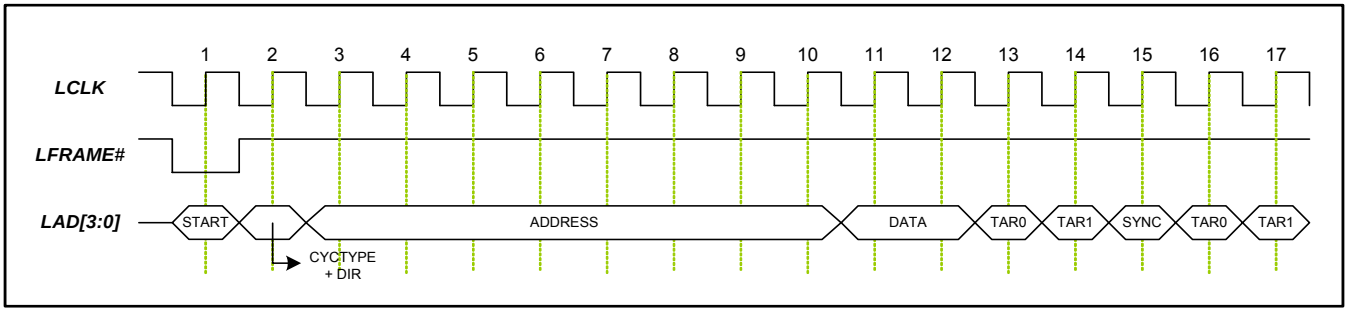


Table 3: LPC Write Cycle

| Clock Cycle | Field Name | Field Contents LAD[3:0][1] | LAD[3:0] Direction | Comments |
|---|---|---|---|---|
| 1 | START | 0000 | IN | $\overline{\text{LFRAME}}$ must be active (low) for the part to respond. Only the last start field (before $\overline{\text{LFRAME}}$ transitioning high) should be recognized. |
| 2 | CYCTYPE + DIR | 011X | IN | Indicates the type of cycle. Bits 3:2 must be "01b" for memory cycle. Bit 1 indicates the type of transfer "1" for Write. Bit 0 is reserved. |
| 3-10 | ADDRESS | YYYY | IN | Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. See Table 4 for address bits definition and Table 5 for valid memory address range. |
| 11 | DATA | ZZZZ | IN | This field is the least-significant nibble of the data byte. |
| 12 | DATA | ZZZZ | IN | This field is the most-significant nibble of the data byte. |
| 13 | TAR0 | 1111 | IN then Float | In this clock cycle, the host has driven the bus to all '1's and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 14 | TAR1 | 1111(float) | Float then OUT | The A49LF040A takes control of the bus during this cycle. |
| 15 | SYNC | 0000 | OUT | The A49LF040A outputs the values "0000b", indicating that it has received data or a flash command. |
| 16 | TAR0 | 1111 | OUT then Float | In this clock cycle, the A49LF040A has driven the bus to all '1's and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 17 | TAR1 | 1111(float) | Float then IN | Host resumes control of the bus during this cycle. |

1. Field contents are valid on the rising edge of the present clock cycle.

LPC Write Waveforms



**Address out of range:** The A49LF040A will only response to address range as specified in Table 4. Address A22 has the special function of directing reads and writes to the flash memory (A22=1) or to the register space (A22=0).
**ID mismatch:** The A49LF040A will compare ID bits in the address field with the hardware ID strapping. If there is a mismatch, the device will ignore the cycle. Refer to Table 6 Multiple Device Selection Configuration for detail.

## Device Memory Hardware Write Protection

The Top Boot Lock ( $\overline{TBL}$ ) and Write Protect ( $\overline{WP}$ ) pins are provided for hardware write protection of device memory in the A49LF040A. The $\overline{TBL}$ pin is used to write protect the top boot block (64 Kbytes) at the highest flash memory address range for the A49LF040A. $\overline{WP}$ pin write protects the remaining blocks in the flash memory. An active low signal at the $\overline{TBL}$ pin prevents Program and Erase operations of the top boot block. When $\overline{TBL}$ pin is held high, write protection of the top boot block is then determined by the Boot Block Locking register. The $\overline{WP}$ pin serves the same function for the remaining blocks of the device memory. The $\overline{TBL}$ and $\overline{WP}$ pins write protection functions operate independently of one another. Both $\overline{TBL}$ and $\overline{WP}$ pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the $\overline{TBL}$ or $\overline{WP}$ pin during a Program or Erase operation could cause unpredictable results. $\overline{TBL}$ and $\overline{WP}$ pins cannot be left unconnected. $\overline{TBL}$ is internally ORed with the top Boot Block Locking register. When $\overline{TBL}$ is low, the top Boot Block is hardware write protected regardless of the state of the Write-Lock bit for the Boot Block Locking register. Clearing the Write-Lock bit in the register when $\overline{TBL}$ is low will have no functional effect, even though the register may indicate that the block is no longer locked. $\overline{WP}$ is internally ORed with the Block Locking register. When $\overline{WP}$ is low, the blocks are hardware write protected regardless of the state of the Write-Lock bit for the corresponding Block Locking registers. Clearing the Write-Lock bit in any register when $\overline{WP}$ is low will have no functional effect, even though the register may indicate that the block is no longer locked.

## Reset

A $V_{IL}$ on $\overline{INIT}$ or $\overline{RST}$ pin initiates a device reset. $\overline{INIT}$ and $\overline{RST}$ pins have the same function internally. It is required to drive $\overline{INIT}$ or $\overline{RST}$ pins low during a system reset to ensure proper CPU initialization. During a Read operation, driving $\overline{INIT}$ or $\overline{RST}$ pins low deselects the device and places the output drivers, LAD[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time $T_{RSTP}$. A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 19, Reset Timing Parameters for more information. A device reset during an active Program or Erase will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation. In this case, the device can take up to $T_{RSTE}$ to abort a Program or Erase operation.

### Write Operation Status Detection

The A49LF040A device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: $\overline{Data}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$). The End-of-Write detection mode is incorporated into the LPC Read cycle. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a $\overline{Data}$ Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either $I/O_7$ or $I/O_6$. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

### $\overline{Data}$ Polling ($I/O_7$)

When the A49LF040A device is in the internal Program operation, any attempt to read $I/O_7$ will produce the complement of the true data. Once the Program operation is completed, $I/O_7$ will produce true data. Note that even though $I/O_7$ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read $I/O_7$ will produce a '0'. Once the internal Erase operation is completed, $I/O_7$ will produce a '1'. Proper status will not be given using $\overline{Data}$ Polling if the address is in the invalid range.

### Toggle Bit ($I/O_6$)

During the internal Program or Erase operation, any consecutive attempts to read $I/O_6$ will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop.

## Multiple Device Selection

The four ID pins, ID[3:0], allow multiple devices to be attached to the same bus by using different ID strapping in a system. When the A49LF040A is used as a boot device, ID[3:0] must be strapped as 0000, all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.). The ID bits in the address field are inverse of the hardware strapping. The address bits [A23, A21:A19] for A49LF004 are used to select the device with proper IDs. See Table 6 for IDs. The A49LF040A will compare the strapping values, if there is a mismatch, the device will ignore the remainder of the cycle and go into standby mode. Since there is no ID support in A/A Mux mode, to program multiple devices a stand-alone PROM programmer is recommended.

## REGISTERS

There are two types of registers available on the A49LF040A, the General Purpose Inputs Register, and the JEDEC ID Registers. These registers appear at their respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read or write any register during an internal Write operation will be ignored. Refer to Table 7 for the LPC register memory map.

### General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of GPI[4:0] pins at power-up on the A49LF040A. It is recommended that the GPI[4:0] pins be in the desired state before $\overline{\text{LFRAME}}$ is brought low for the beginning of the next bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. See Table 8 for the GPI_REG bits and function, and Table 7 for memory address locations for its respective device strapping.

Table 8: General Purpose Inputs Register

| Bit | Bit Name | Function | Pin Number | |
|---|---|---|---|---|
| | | | 32-PLCC | 32-TSOP |
| 7:5 | - | Reserved | - | - |
| 4 | GPI[4] | GPI_REG Bit 4 | 30 | 6 |
| 3 | GPI[3] | GPI_REG Bit 3 | 3 | 11 |
| 2 | GPI[2] | GPI_REG Bit 2 | 4 | 12 |
| 1 | GPI[1] | GPI_REG Bit 1 | 5 | 13 |
| 0 | GPI[0] | GPI_REG Bit 0 | 6 | 14 |

#### Block Locking Registers

A49LF040A provides software controlled lock protection through a set of Block Locking registers. The Block Locking Registers are read/write registers and it is accessible through standard addressable memory locations specified in Table 7.

See Table 9 for Bit definition of the Block Lock Register.

**Write-Lock.** The Write-Lock Bit determines whether the contents of the Block can be modified (using the Program or Erase Command). When the Write-Lock Bit is set to '1', the block is write protected; any operations that attempt to change the data in the block will fail and the Status Register will report the error. When the Write-Lock Bit is reset to '0', the block is not write protected through the Locking Register and may be modified unless write protected through some other means. If Top Block Lock, $\overline{\text{TBL}}$ , is Low, $V_{IL}$, then the Top Block (Block 7) is write protected and cannot be modified. Similarly, if Write Protect, $\overline{\text{WP}}$ , is Low, $V_{IL}$, then the Main Blocks (Blocks 0 to 6) are write protected and cannot be modified. After power-up or reset the Write-Lock Bit is always set to '1' (write protected).

**Read-Lock.** The Read-Lock bit determines whether the contents of the Block can be read (from Read mode). When the Read-Lock Bit is set to '1', the block is read protected; any operation that attempts to read the contents of the block will read 00h instead. When the Read-Lock Bit is reset to '0', read operations in the Block return the data programmed into the block as expected. After power-up or reset the Read-Lock Bit is always reset to '0' (not read protected).

**Lock-Down.** The Lock-Down Bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock-Down Bit is set to '1', further modification to the Write-Lock, Read-Lock and Lock-Down Bits cannot be performed. A reset or power-up is required before changes to these bits can be made. When the Lock-Down Bit is reset to '0', the Write-Lock, Read-Lock and Lock-Down Bits can be changed.

#### JEDEC ID Registers

The JEDEC ID registers identify the device as A49LF040A and manufacturer as AMIC in LPC mode. See Table 7 for memory address locations for its respective JEDEC ID location.

Table 4: Address Bit Definition

| $A_{31}$:$A_{23}$ | $A_{23}$ | $A_{22}$ | $A_{21}$:$A_{19}$ | $A_{18}$:$A_0$ |
|---|---|---|---|---|
| 1111 1111b | ID[3] | 1 = Memory access<br>0 = Register access | ID[2:0] | Device memory address |

Table 5: Address Decoding Range

| ID Strapping | Device Access | $A_{21}$:$A_{19}$ | Memory Size |
|---|---|---|---|
| Device #0 – 7 | Memory Access | FFFF FFFFH: FFC0 0000H | 4 MByte |
| | Register Access | FFBF FFFFH: FF80 0000H | 4 MByte |
| Device #8 - 15 | Memory Access | FF7F FFFFH: FF40 0000H | 4 MByte |
| | Register Access | FF3F FFFFH: FF00 0000H | 4 MByte |

Table 6: Multiple Device Selection Configurations

| Device# | Hardware Strapping ID[3:0] | Address Bits Decoding | | | |
|---|---|---|---|---|---|
| | | A23 | A21 | A20 | A19 |
| 0 (Boot device) | 0000 | 1 | 1 | 1 | 1 |
| 1 | 0001 | 1 | 1 | 1 | 0 |
| 2 | 0010 | 1 | 1 | 0 | 1 |
| 3 | 0011 | 1 | 1 | 0 | 0 |
| 4 | 0100 | 1 | 0 | 1 | 1 |
| 5 | 0101 | 1 | 0 | 1 | 0 |
| 6 | 0110 | 1 | 0 | 0 | 1 |
| 7 | 0111 | 1 | 0 | 0 | 0 |
| 8 | 1000 | 0 | 1 | 1 | 1 |
| 9 | 1001 | 0 | 1 | 1 | 0 |
| 10 | 1010 | 0 | 1 | 0 | 1 |
| 11 | 1011 | 0 | 1 | 0 | 0 |
| 12 | 1100 | 0 | 0 | 1 | 1 |
| 13 | 1101 | 0 | 0 | 1 | 0 |
| 14 | 1110 | 0 | 0 | 0 | 1 |
| 15 | 1111 | 0 | 0 | 0 | 0 |

Table 7: LPC Register Memory Map (Boot Device)

| Memory Address | Mnemonic | Register Name | Default | Type |
|---|---|---|---|---|
| FFBF0002h | T_BLOCK_LK | Top Block Lock Register (Block 7) | 01h | R/W |
| FFBE0002h | T_MINUS01_LK | Top Block [-1] Lock Register (Block 6) | 01h | R/W |
| FFBD0002h | T_MINUS02_LK | Top Block [-2] Lock Register (Block 5) | 01h | R/W |
| FFBC0002h | T_MINUS03_LK | Top Block [-3] Lock Register (Block 4) | 01h | R/W |
| FFBB0002h | T_MINUS04_LK | Top Block [-4] Lock Register (Block 3) | 01h | R/W |
| FFBA0002h | T_MINUS05_LK | Top Block [-5] Lock Register (Block 2) | 01h | R/W |
| FFB90002h | T_MINUS06_LK | Top Block [-6] Lock Register (Block 1) | 01h | R/W |
| FFB80002h | T_MINUS07_LK | Top Block [-7] Lock Register (Block 0) | 01h | R/W |
| FFBC0100h | GPI_REG | LPC General Purpose Input Register | N/A | R |
| FFBC0000h | MANUF_REG | Manufacturer ID Register | 37h | R |
| FFBC0001h | DEV_REG | Device ID Register | 9Dh | R |
| FFBC0003h | CONT_REG | Continuation ID Register | 7Fh | R |

Table 9: Lock Register Bit Definition

| Data | Reserved Bit 7:3 | Read-Lock Bit 2 | Lock-Down Bit 1 | Write-Lock Bit 0 | Function |
|---|---|---|---|---|---|
| 00h | 00000 | 0 | 0 | 0 | Full Access. |
| 01h | 00000 | 0 | 0 | 1 | Write locked. Default state at power-up. |
| 02h | 00000 | 0 | 1 | 0 | Locked open (full access locked down). |
| 03h | 00000 | 0 | 1 | 1 | Write-locked down. |
| 04h | 00000 | 1 | 0 | 0 | Read locked. |
| 05h | 00000 | 1 | 0 | 1 | Read and Write locked. |
| 06h | 00000 | 1 | 1 | 0 | Read-locked down |
| 07h | 00000 | 1 | 1 | 1 | Read- and Write-locked down |

| Data | Function |
|---|---|
| 7:3 | **Reserved** |
| 2 | **Read-Lock**<br>1 = Prevents read operations in the block where set<br>0 = Normal operation for reads in the block where clear. This is the default state. |
| 1 | **Lock-Down**<br>1 = Prevents further set or clear operations to the Write-Lock and Read-Lock bits. Lock-Down only can be set but not clear. The block will remain lock-down until reset (with $\overline{RST}$ or $\overline{INIT}$ being Low), or until the device is power-on reset.<br>0 = Normal operation for Write-Lock and Read-Lock bit altering in the block where clear. This is the default state. |
| 0 | **Write-Lock**<br>1 = Prevents program or erase operations in the block where set. This is the default state.<br>0 = Normal operation for programming and erase in the block where clear. |

## ADDRESS/ADDRESS MULTIPLEXED (A/A MUX) MODE

### Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of $\overline{WE}$. During the software command sequence the row address is latched on the falling edge of R/$\overline{C}$ and the column address is latched on the rising edge of R/$\overline{C}$. Refer to Table 10 and Table 11 for operation modes and the command sequence.

### Read

The Read operation of the A49LF040A device is controlled by $\overline{OE}$. $\overline{OE}$ is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 10 for further details.

### Reset

A $V_{IL}$ on $\overline{RST}$ pin initiates a device reset.

### Byte-Program Operation

The A49LF040A device is programmed on a byte-by-byte basis. Before programming, one must ensure that the block, in which the byte which is being programmed exists, is fully erased. The Byte-Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address and data in the last byte sequence. During the Byte-Program operation, the row address (A10-A0) is latched on the falling edge of R/$\overline{C}$ and the column Address (A18-A11) is latched on the rising edge of R/$\overline{C}$. The data bus is latched in the rising edge of $\overline{WE}$. See Figure 11 for Program operation timing diagram, Figure 14 for timing waveforms, and Figure 19 for its flowchart. During the Program operation, the only valid reads are $\overline{Data}$ Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Table 10: A/A Mux Mode Operation Selection

| Mode | $\overline{RST}$ | $\overline{OE}$ | $\overline{WE}$ | Address | I/O |
|---|---|---|---|---|---|
| Read | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $A_{IN}$ | $D_{OUT}$ |
| Write | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | $A_{IN}$ | $D_{IN}$ |
| Standby | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | High Z |
| Output Disable | $V_{IH}$ | $V_{IH}$ | X | X | High Z |
| Reset | $V_{IL}$ | X | X | X | High Z |
| Product Identification | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | A18 – A2 = X, A1 = $V_{IL}$, A0 = $V_{IL}$ | Manufacturer ID |
| | | | | A18 – A2 = X, A1 = $V_{IL}$, A0 = $V_{IH}$ | Device ID |
| | | | | A18 – A2 = X, A1 = $V_{IH}$, A0 = $V_{IH}$ | Continuation ID |

### Block-Erase Operation

The Block-Erase Operation allows the system to erase the device in 64 KByte uniform block size for the A49LF040A. The Block-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block-Erase command (30H or 50H) and block address. The internal Block-Erase operation begins after the sixth $\overline{WE}$ pulse. The End-of-Erase can be determined using either $\overline{Data}$ Polling or Toggle Bit methods. See Figure 15 for timing waveforms. Any commands written during the Block- Erase operation will be ignored.

### Chip-Erase

The A49LF040A device provides a Chip-Erase operation only in A/A Mux mode, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased. The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth $\overline{WE}$. During the internal Erase operation, the only valid read is Toggle Bit or $\overline{Data}$ Polling. See Table 11 for the command sequence, Figure 16 for timing diagram, and Figure 21 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

### Write Operation Status Detection

The A49LF040A device provides two software means to detect the completion of a Write cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: $\overline{Data}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$). The End-of-Write detection mode is enabled after the rising edge of $\overline{WE}$ which initiates the internal Write operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a $\overline{Data}$ Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle.

If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either $I/O_7$ or $I/O_6$. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.
In addition to $I/O_6$ and $I/O_7$ to detect the write status, a $R/\overline{B}$ pin is also available to detect the end of a Program or Erase operation. $R/\overline{B}$ is actively pulled low ($V_{IL}$) during the internal write cycles and is released to high ($V_{IH}$) at the completion of the cycle.

### $\overline{\text{Data}}$ Polling ($I/O_7$)

When the A49LF040A device is in the internal Program operation, any attempt to read $I/O_7$ will produce the complement of the true data. Once the Program operation is completed, $I/O_7$ will produce true data. Note that even though $I/O_7$ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read $I/O_7$ will produce a '0'. Once the internal Erase operation is completed, $I/O_7$ will produce a '1'. The $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth $\overline{\text{WE}}$ pulse for Program operation. For Block- or Chip-Erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of sixth $\overline{\text{WE}}$ pulse. See Figure 12 for $\overline{\text{Data}}$ Polling timing diagram. Proper status will not be given using $\overline{\text{Data}}$ Polling if the address is in the invalid range.

### Toggle Bit ($I/O_6$)

During the internal Program or Erase operation, any consecutive attempts to read $I/O_6$ will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth $\overline{\text{WE}}$ pulse for Program operation. For Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth $\overline{\text{WE}}$ pulse. See Figure 13 for Toggle Bit timing diagram.

## Data Protection

The A49LF040A device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

### Hardware Data Protection

Noise/Glitch Protection: A $\overline{\text{WE}}$ pulse of less than 5 ns will not initiate a Write cycle.
$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 1.5V.
Write Inhibit Mode: Forcing $\overline{\text{OE}}$ low, $\overline{\text{WE}}$ high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

### Software Data Protection (SDP)

The A49LF040A provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequences. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of a six-byte load sequence. The A49LF040A device is shipped with the Software Data Protection permanently enabled. See Table 11 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode, within $T_{RC}$.

## Electrical Specifications

The AC and DC specifications for the LPC Interface signals (LAD[3:0], LCLK, $\overline{\text{LFRAME}}$ , and $\overline{\text{RST}}$ ) as defined in Section 4.2.2 of the *PCI Local Bus Specification, Rev. 2.1*. Refer to Table 12 for the DC voltage and current specifications. Refer to the specifications on Table 12 to Table 22 for Clock, Read/Write, and Reset operations.

## Product Identification

The product identification mode identifies the Manufacturer ID, Continuation ID, and Device ID of the A49LF040A. See Table 10 for detail information.

Figure 3: System Memory Map and Device Memory Map for A49LF040A

D Visio.Drawing.6 |

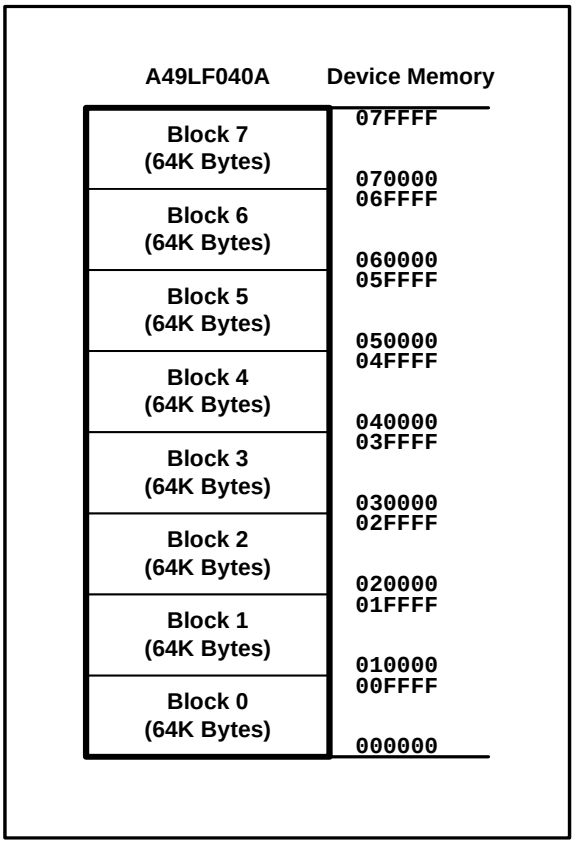



Table 11: Software Data Protection Command Definition

| Command | Bus Cycles | 1st Cycle(1) | | 2nd Cycle | | 3rd Cycle | | 4th Cycle | | 5th Cycle | | 6th Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr(2) | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| **Block Erase** | 6 | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 80H | YYYY 5555H | AAH | YYYY 2AAAH | 55H | BA(4) | 30H/50H(5) |
| **Chip Erase(3)** | 6 | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 80H | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 10H |
| **Byte Program** | 4 | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | A0H | PA(6) | PD(6) | | | | |
| **Product ID Entry** | 3 | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 90H | | | | | | |
| **Product ID Exit(7)** | 1 | XXXX XXXXH | F0H | | | | | | | | | | |
| **Product ID Exit(7)** | 3 | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | F0H | | | | | | |

Notes:
1. LPC Mode uses consecutive Write cycles to complete a command sequence; A/A Mux Mode uses consecutive bus cycles to complete a command sequence.
2. YYYY = A[31:16]. In LPC mode, during SDP command sequence, YYYY must be within memory address range specified in Table 5. In A/A Mux mode, YYYY can be $V_{IL}$ or $V_{IH}$, but no other value.
3. Chip erase is available in A/A Mux Mode only.
4. BA: Block Erase Address.
5. Either 30H or 50H are acceptable for Block Erase.
6. PA: Program Byte Address; PD: Byte data to be programmed.
7. Both Product ID Exit commands are equivalent.

**Operating Range**

| Range | Ambient Temperature | $V_{DD}$ |
|---|---|---|
| Commercial | 0°C to +85°C | 3.0-3.6V |

**AC Conditions of Test**

| |
|---|
| Input Rise/Fall Time . . . . . 3ns |
| Output Load . . . . . CL = 30pF |

Table 12: DC Operating Characteristics (All Interfaces)

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | Units | |
| $I_{DD}$ | Active $V_{DD}$ Current: Read | | 12 | mA | Address Input=$V_{IL}/V_{IH}$, at F=1/$T_{RC}$Min, $V_{DD}=V_{DD}$Max(A/A Mux Mode) |
| | Active $V_{DD}$ Current: Write(1) | | 24 | mA | $\overline{OE}$ =$V_{IH}$, $\overline{WE}$ =$V_{IH}$ |
| $I_{SB}$ | Standby $V_{DD}$ Current (LPC Mode) | | 100 | µA | $\overline{LFRAME}$ =0.9$V_{DD}$, f=33MHz, $V_{DD}=V_{DD}$Max, All other inputs ≥ 0.9$V_{DD}$ or ≤ 0.1$V_{DD}$ |
| $I_{RY}$(2) | Ready Mode $V_{DD}$ Current (LPC Mode) | | 10 | mA | $\overline{LFRAME}$ =$V_{IL}$, f=33MHz, $V_{DD}=V_{DD}$Max, All other inputs ≥ 0.9$V_{DD}$ or ≤ 0.1$V_{DD}$ |
| $I_I$ | Input Current for Mode and ID[3:0] Pins | | 100 | µA | $V_{IN}$=0V to $V_{DD}$, $V_{DD}=V_{DD}$Max |
| $I_{LI}$ | Input Leakage Current | | 1 | µA | $V_{IN}$=0V to $V_{DD}$, $V_{DD}=V_{DD}$Max |
| $I_{LO}$ | Output Leakage Current | | 1 | µA | $V_{OUT}$=0V to $V_{DD}$, $V_{DD}=V_{DD}$Max |
| $V_{IHI}$(3) | $\overline{INIT}$ Input High Voltage | 1.0 | $V_{DD}$+0.5 | V | $V_{DD}=V_{DD}$Max |
| $V_{ILI}$(3) | $\overline{INIT}$ Input Low Voltage | -0.5 | 0.4 | V | $V_{DD}=V_{DD}$Min |
| $V_{IH}$ | Input High Voltage | 0.5$V_{DD}$ | $V_{DD}$+0.5 | V | $V_{DD}=V_{DD}$Max |
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.3$V_{DD}$ | V | $V_{DD}=V_{DD}$Min |
| $V_{OL}$ | Output Low Voltage | | 0.1$V_{DD}$ | V | IOL=1500µA, $V_{DD}=V_{DD}$Min |
| $V_{OH}$ | Output High Voltage | 0.9$V_{DD}$ | | V | IOH=-500µA, $V_{DD}=V_{DD}$Min |

Notes:
1. $I_{DD}$ active while Erase or Program is in progress.
2. The device is in Ready Mode when no activity is on the LPC bus.
3. Do not violate processor or chipset specification regarding $\overline{INIT}$ voltage.

Table 13: Recommended System Power-Up Timings

| Symbol | Parameter | Min | Units |
|---|---|---|---|
| $T_{PU-READ}$(1) | Power-up to Read Operation | 100 | µs |
| $T_{PU-WRITE}$(1) | Power-up to Write Operation | 100 | µs |

Notes:
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 14: Pin Impedance ($V_{DD}$=3.3V, Ta=25°C, f=1MHz, other pins open)

| Parameter | Description | Test Condition | Max |
|---|---|---|---|
| $C_{I/O}$ (1) | I/O Pin Capacitance | $V_{I/O}$ = 0V | 12pF |
| $C_{IN}$ (1) | Input Capacitance | $V_{IN}$ = 0V | 12pF |
| $L_{PIN}$ (2) | Pin Inductance | | 20nH |

Notes:
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI specifications.

Table 15: Clock Timing Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CYC}$ | LCLK Cycle Time | 30 | | ns |
| $T_{HIGH}$ | LCLK High Time | 11 | | ns |
| $T_{LOW}$ | LCLK Low Time | 11 | | ns |
| | LCLK Slew Rate (peak-to-peak) | 1 | 4 | V/ns |

Figure 4: LCLK Waveform

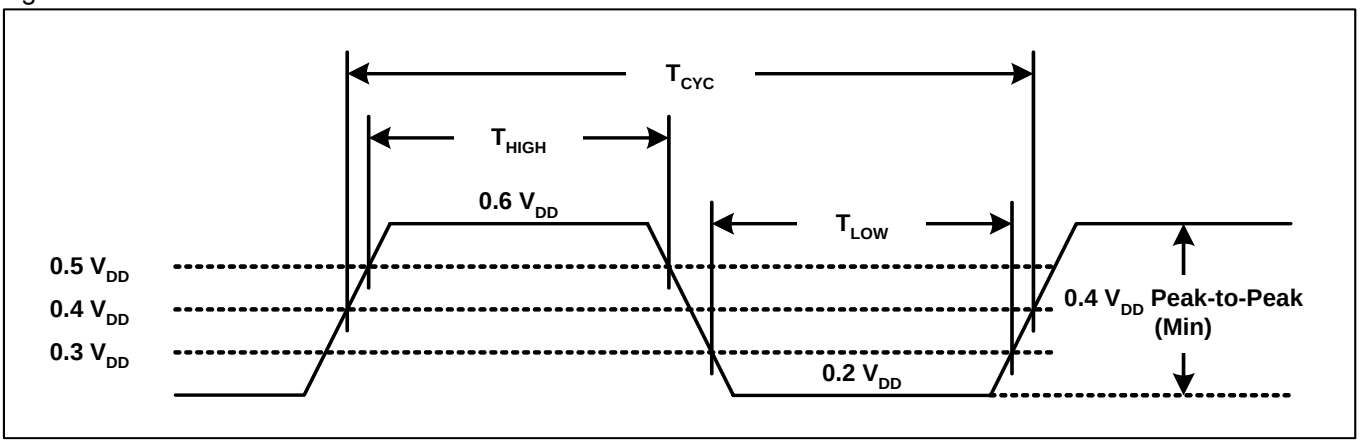



Table 16: LPC Mode Read/Write Cycle Timing Parameters, $V_{DD}$=3.0-3.6V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{SU}$ | Input Set Up Time to LCLK Rising | 7 | | ns |
| $T_{DH}$ | LCLK Rising to Data Hold Time | 0 | | ns |
| $T_{VAL}$ | LCLK Rising to Data Valid | 2 | 11 | ns |
| $T_{ON}$ | LCLK Rising to Active (Float to Active Delay) | 2 | | ns |
| $T_{OFF}$ | LCLK Rising to Inactive (Active to Float Delay) | | 28 | ns |

Table 17: LPC Mode Interface Measurement Condition Parameters

| Symbol | Value | Units |
|---|---|---|
| $V_{TH}$ | 0.6 $V_{DD}$ | V |
| $V_{TL}$ | 0.2 $V_{DD}$ | V |
| $V_{TEST}$ | 0.4 $V_{DD}$ | V |
| $V_{MAX}$ | 0.4 $V_{DD}$ | V |
| Input Signal Edge Rate | 1V/ns | |

Figure 5: Input Timing Parameters

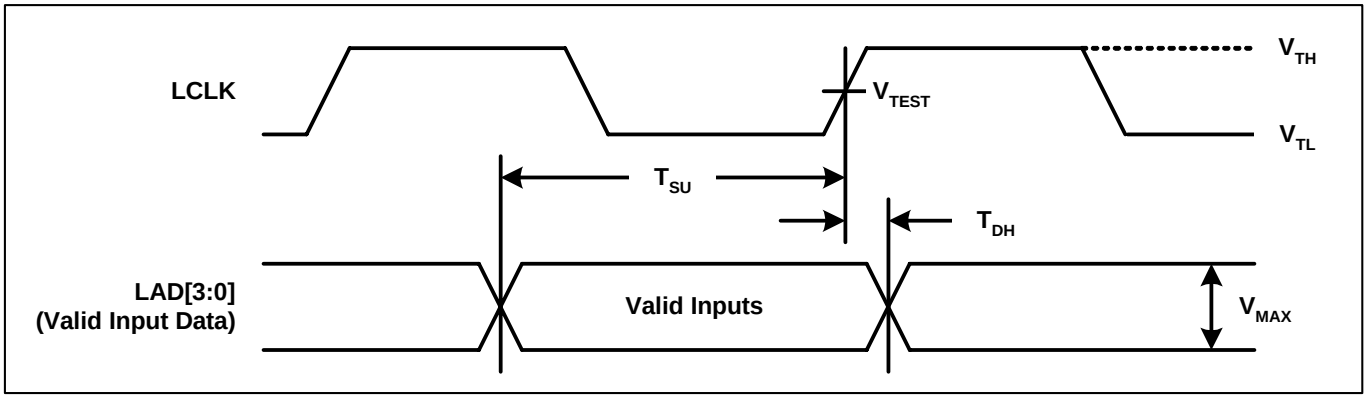



Figure 6: Output Timing Parameters

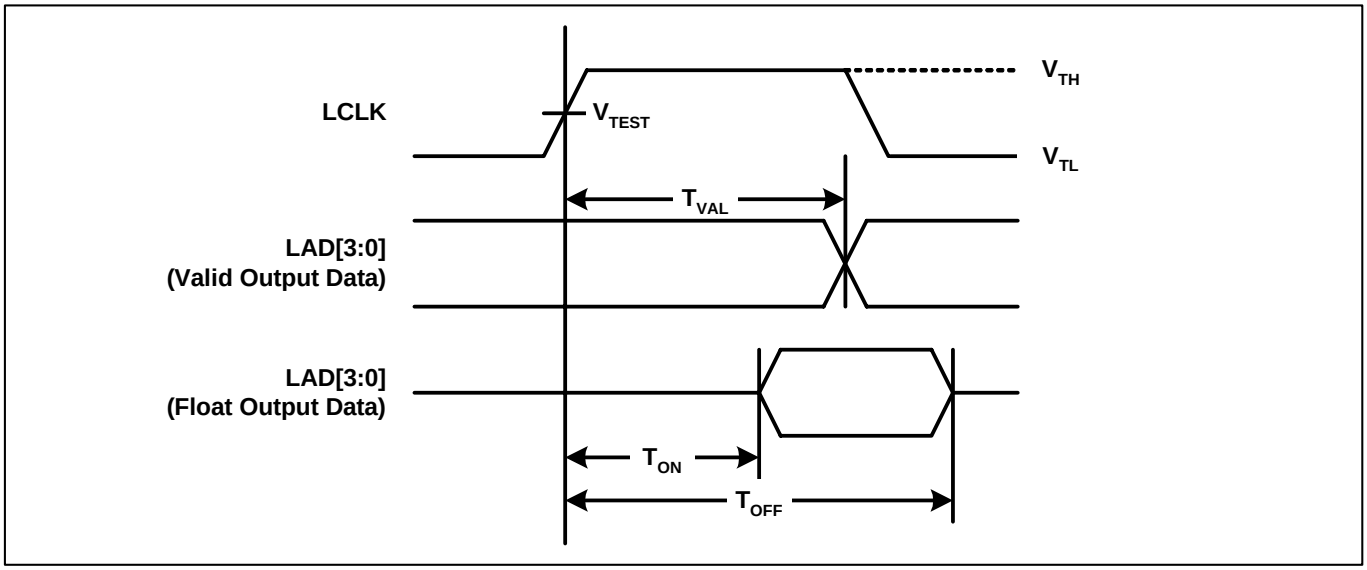


Table 18: LPC Mode Interface AC Input/Output Characteristics

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{OH}$ (AC) | Switching Current High | $0 < V_{OUT} \le 0.3V_{DD}$ | $-12\ V_{DD}$ | | mA |
| | | $0.3V_{DD} < V_{OUT} \le 0.9V_{DD}$ | $-17.1(V_{DD}-V_{OUT})$ | | mA |
| | | $0.7V_{DD} < V_{OUT} \le V_{DD}$ | | Equation C | mA |
| | (Test Point) | $V_{OUT} = 0.7V_{DD}$ | | $-32\ V_{DD}$ | mA |
| $I_{OL}$ (AC) | Switching Current Low | $V_{DD} > V_{OUT} \ge 0.6V_{DD}$ | $16V_{DD}$ | | mA |
| | | $0.6V_{DD} > V_{OUT} > 0.1V_{DD}$ | $26.7V_{OUT}$ | | mA |
| | | $0.18V_{DD} > V_{OUT} > 0$ | | Equation D | mA |
| | (Test Point) | $V_{OUT}=0.18V_{DD}$ | | $38V_{DD}$ | mA |
| $I_{CL}$ | Low Clamp Current | $-3 < V_{IN} \le -1$ | $-25+(V_{IN}+1)/0.015$ | | mA |
| $I_{CH}$ | High Clamp Current | $V_{DD}+4 > V_{IN} > V_{DD}+1$ | $25+(V_{IN}-V_{DD}-1)/0.015$ | | mA |
| slewr | Output Rise Slew Rate | $0.2V_{DD}$-$0.6V_{DD}$ load | 1 | 4 | V/ns |
| slewf | Output Fall Slew Rate | $0.6V_{DD}$-$0.2V_{DD}$ load | 1 | 4 | V/ns |

Notes:
1. See PCI specification.
2. PCI specification output load is used.

Table 19: LPC Mode Interface Reset Timing Parameters, $V_{DD}$=3.0-3.6V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{PRST}$ | $V_{DD}$ Stable to Reset Low | 1 | | ms |
| $T_{KRST}$ | Clock Stable to Reset Low | 100 | | µs |
| $T_{RSTP}$ | $\overline{RST}$ Pulse Width | 100 | | ns |
| $T_{RSTF}$ | $\overline{RST}$ Low to Output Float | | 48 | ns |
| $T_{RST}$(1) | $\overline{RST}$ High to $\overline{LFRAME}$ Low | 1 | | µs |
| $T_{RSTE}$ | $\overline{RST}$ Low to Reset During Erase or Program | | 10 | µs |
| | $\overline{RST}$ or $\overline{INIT}$ Slew Rate | 50 | | mV/ns |

Notes:
1. There will be a latency of $T_{RSTE}$ if a reset procedure is performed during a Program or Erase operation.

Figure 7: Reset Timing Diagram

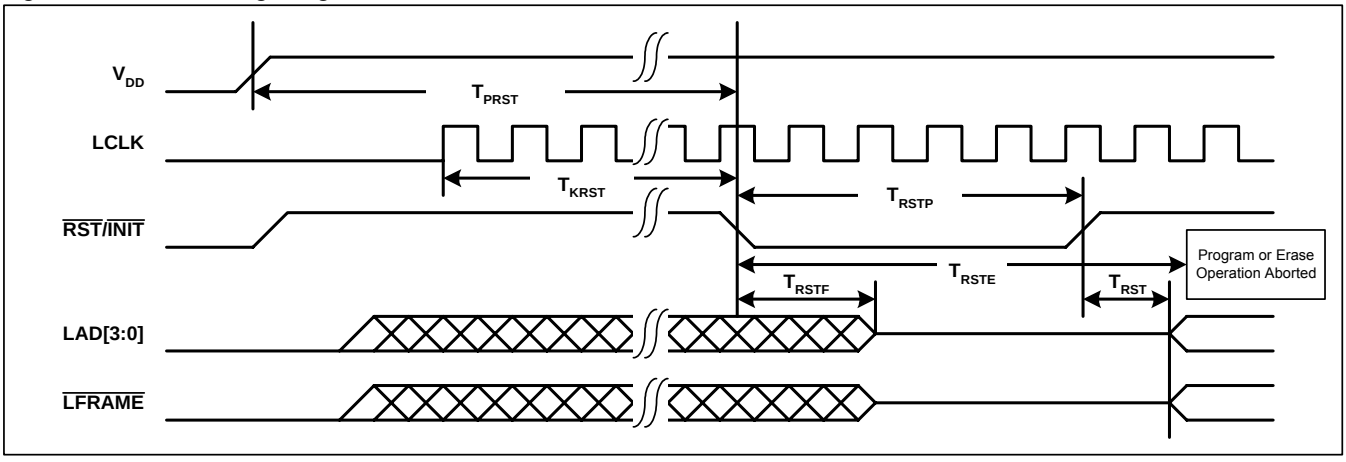
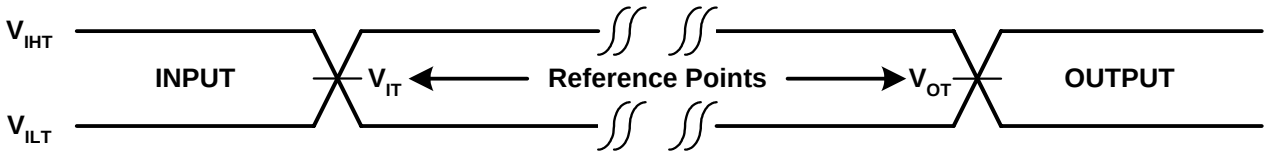


Figure 8: A/A Mux Mode AC Input/Output Reference Waveforms

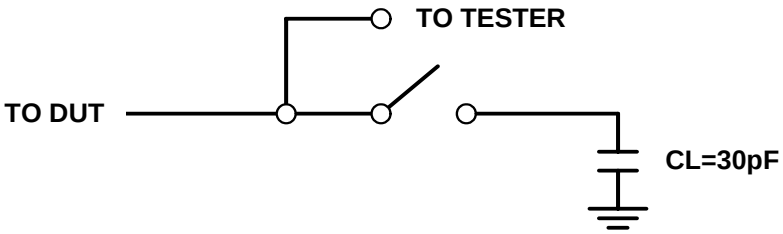



AC test inputs are driven at $V_{IHT}$ ($0.9V_{DD}$) for a logic HIGH and $V_{ILT}$ ($0.1V_{DD}$) for a logic LOW. Measurement reference points for inputs and outputs are $V_{IT}$ ($0.5V_{DD}$) and $V_{OT}$ ($0.5V_{DD}$). Input rise and fall times (10% <-> 90%) are < 5ns

Note:

$V_{IT}$: $V_{INPUT}$ Test
$V_{OT}$: $V_{OUTPUT}$ Test
$V_{IHT}$: $V_{INPUT}$ HIGH Test
$V_{ILT}$: $V_{INPUT}$ LOW Test

Figure 9: A/A Mux Mode Test Load Condition



## A/A MUX MODE AC CHARACTERISTICS

Table 20: Read Cycle Timing Parameters $V_{DD}$=3.0-3.6V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RC}$ | Read Cycle Time | 270 | | ns |
| $T_{RST}$ | $\overline{RST}$ High to Row Address Setup | 1 | | μs |
| $T_{AS}$ | R/$\overline{C}$ Address Set-up Time | 45 | | ns |
| $T_{AH}$ | R/$\overline{C}$ Address Hold Time | 45 | | ns |
| $T_{AA}$ | Address Access Time | | 120 | ns |
| $T_{OE}$ | Output Enable Access Time | | 60 | ns |
| $T_{OLZ}$ | $\overline{OE}$ Low to Active Output | 0 | | ns |
| $T_{OHZ}$ | $\overline{OE}$ High to High-Z Output | | 35 | ns |
| $T_{OH}$ | Output Hold from Address Change | 0 | | ns |

Table 21: Program/Erase Cycle Timing Parameters, $V_{DD}$=3.0-3.6V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RST}$ | $\overline{RST}$ High to Row Address Setup | 1 | | μs |
| $T_{AS}$ | R/$\overline{C}$ Address Setup Time | 50 | | ns |
| $T_{AH}$ | R/$\overline{C}$ Address Hold Time | 50 | | ns |
| $T_{CWH}$ | R/$\overline{C}$ to Write Enable High Time | 50 | | ns |
| $T_{OES}$ | $\overline{OE}$ High Setup Time | 20 | | ns |
| $T_{OEH}$ | $\overline{OE}$ High Hold Time | 20 | | ns |
| $T_{OEP}$ | $\overline{OE}$ to $\overline{Data}$ Polling Delay | | 40 | ns |
| $T_{OET}$ | $\overline{OE}$ to Toggle Bit Delay | | 40 | ns |
| $T_{WP}$ | $\overline{WE}$ Pulse Width | 100 | | ns |
| $T_{WPH}$ | $\overline{WE}$ Pulse Width High | 100 | | ns |
| $T_{DS}$ | Data Setup Time | 50 | | ns |
| $T_{DH}$ | Data Hold Time | 5 | | ns |
| $T_{IDA}$ | Product ID Access and Exit Time | | 150 | ns |
| $T_{BP}$ | Byte Programming Time | | 300 | μs |
| $T_{BE}$ | Block Erase Time | | 8 | s |
| $T_{SCE}$ | Chip Erase Time | | 10 | s |

Table 22: Reset Timing Parameters, $V_{DD}$=3.0-3.6V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{PRST}$ | $V_{DD}$ Stable to Reset Low | 1 | | ms |
| $T_{RSTP}$ | $\overline{RST}$ Pulse Width | 100 | | ns |
| $T_{RSTF}$ | $\overline{RST}$ Low to Output Float | | 48 | ns |
| $T_{RST}$(1) | $\overline{RST}$ High to $\overline{LFRAME}$ Low | 1 | | μs |
| $T_{RSTE}$ | $\overline{RST}$ Low to Reset During Erase or Program | | 10 | μs |

Notes:
1. There will be a reset latency of $T_{RSTE}$ if a reset procedure is performed during a Program or Erase operation.

Figure 10: A/A Mux Mode Read Cycle Timing Diagram

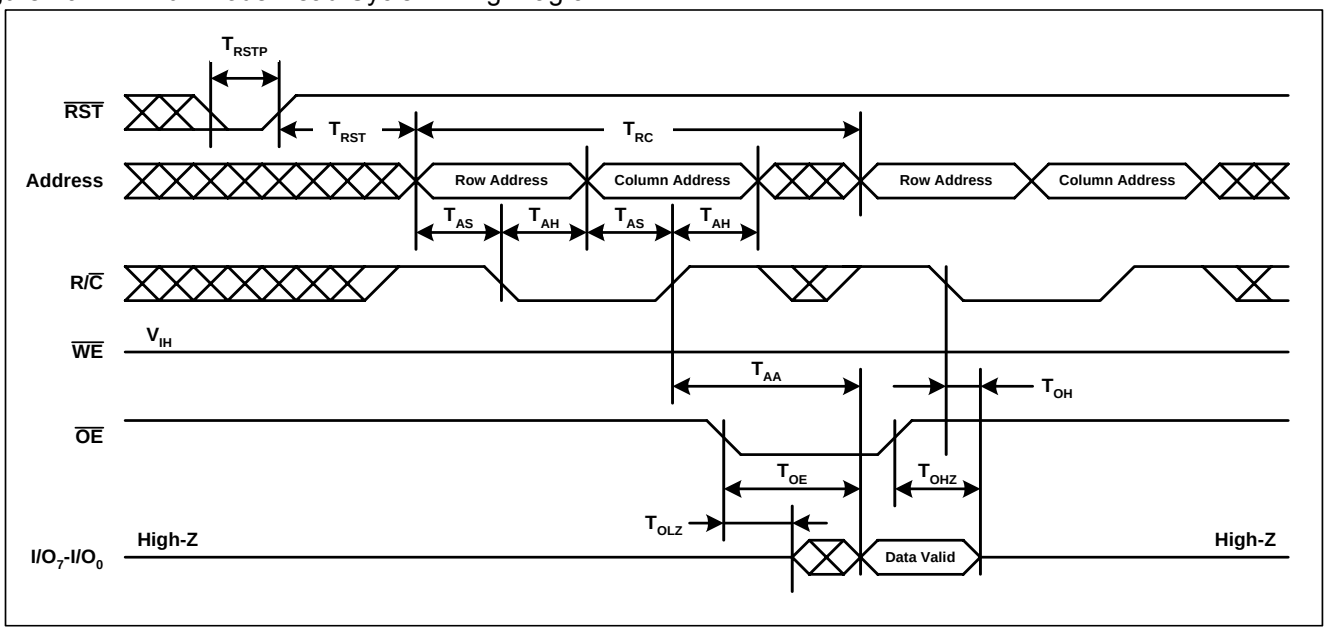



Figure 11: A/A Mux Mode Write Cycle Timing Diagram

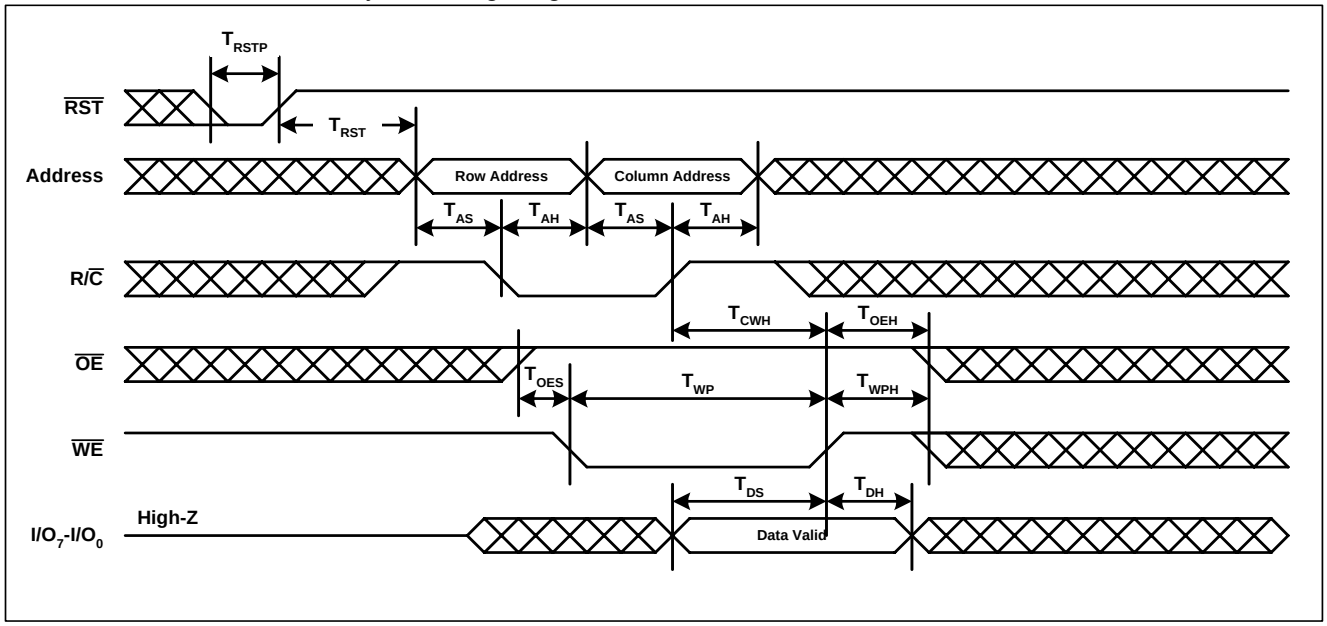


Figure 12: A/A Mux Mode $\overline{\text{Data}}$ Polling Timing Diagram

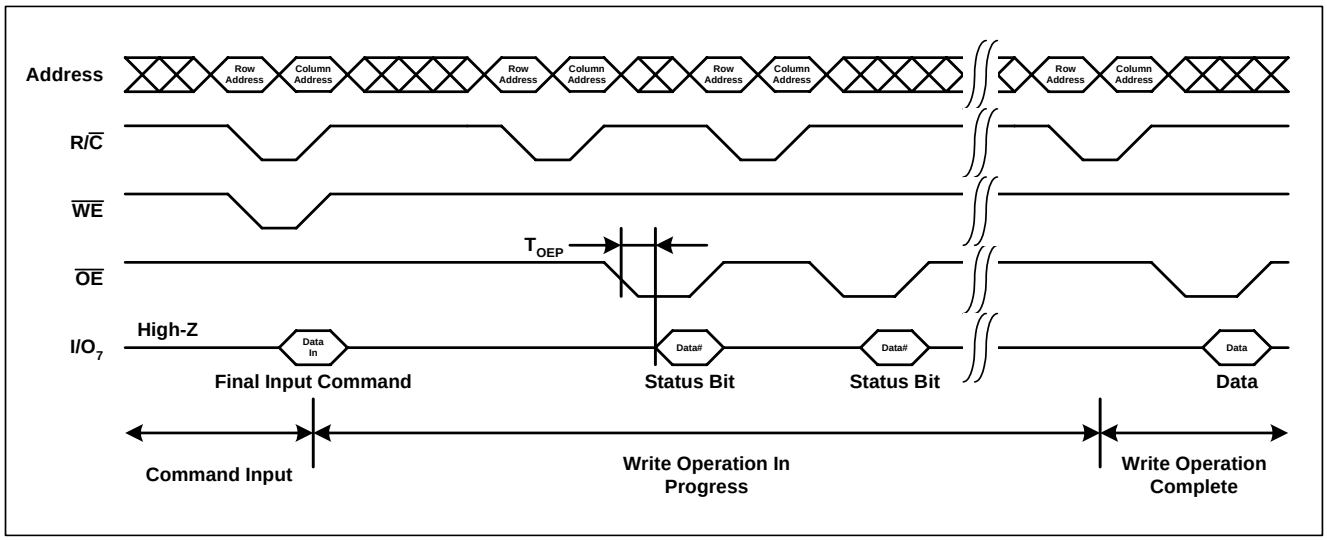



Figure 13: A/A Mux Mode Toggle Bit Timing Diagram

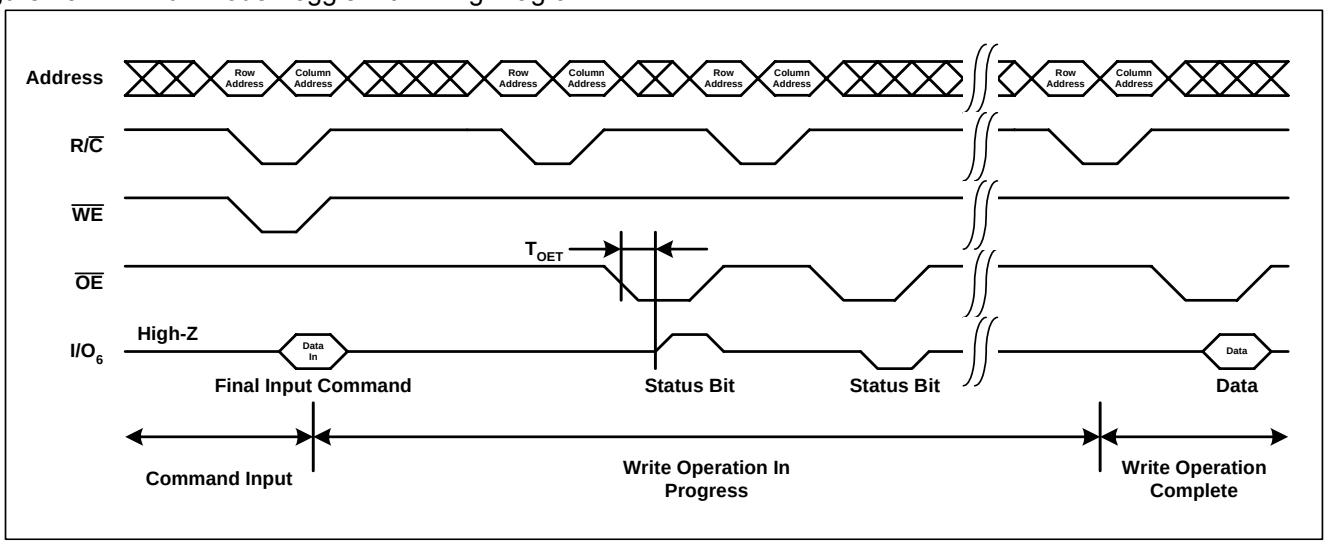


Figure 14: A/A Mux Mode Byte Program Timing Diagram

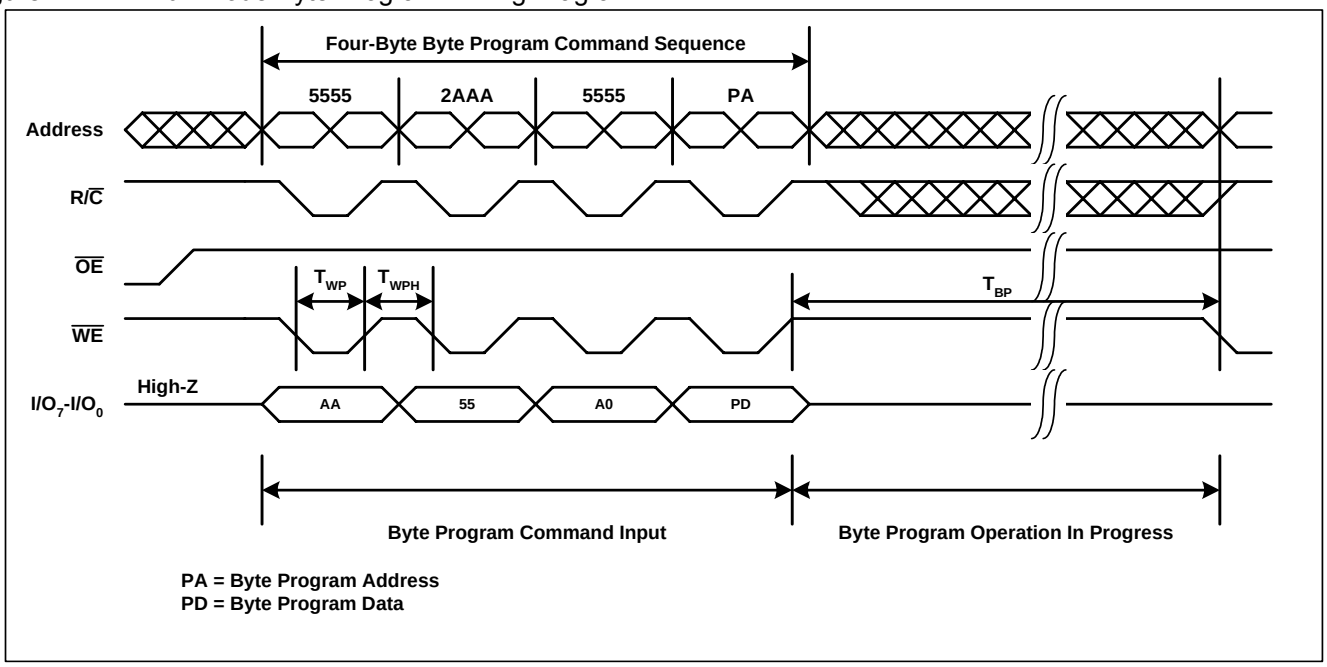



Figure 15: A/A Mux Mode Block Erase Timing Diagram

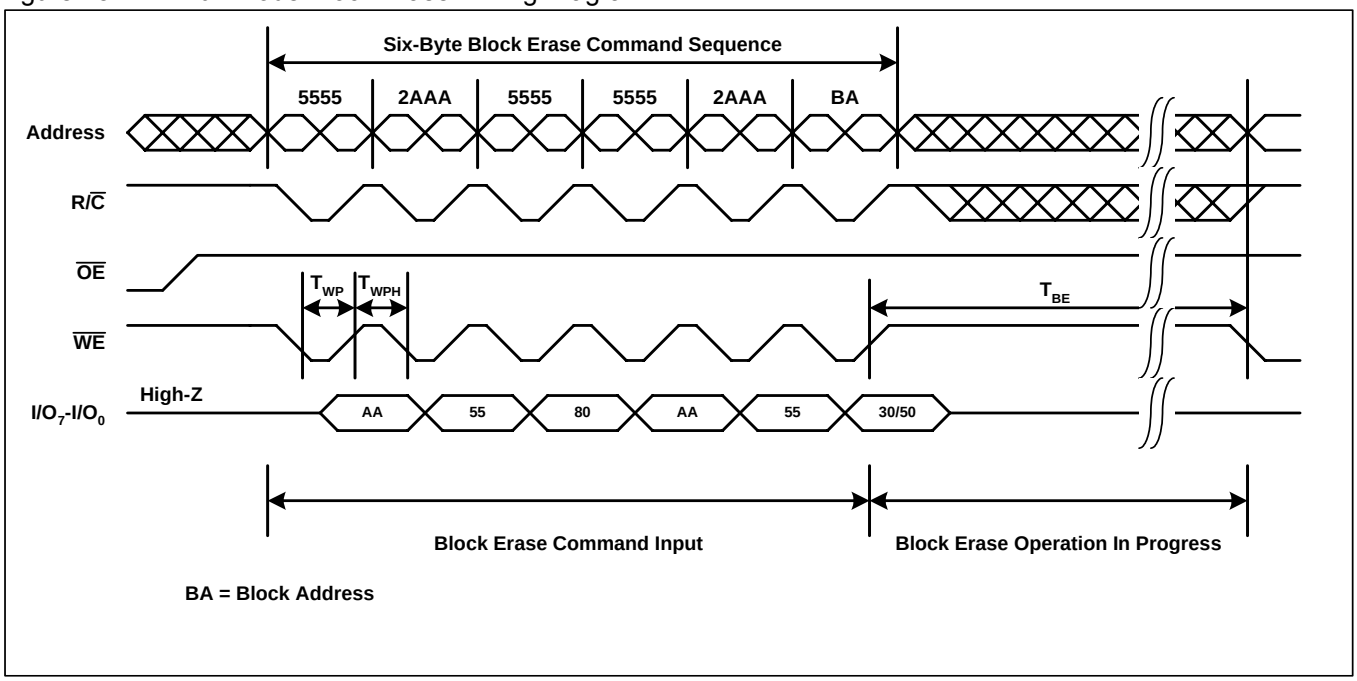


Figure 16: A/A Mux Mode Chip Erase Timing Diagram

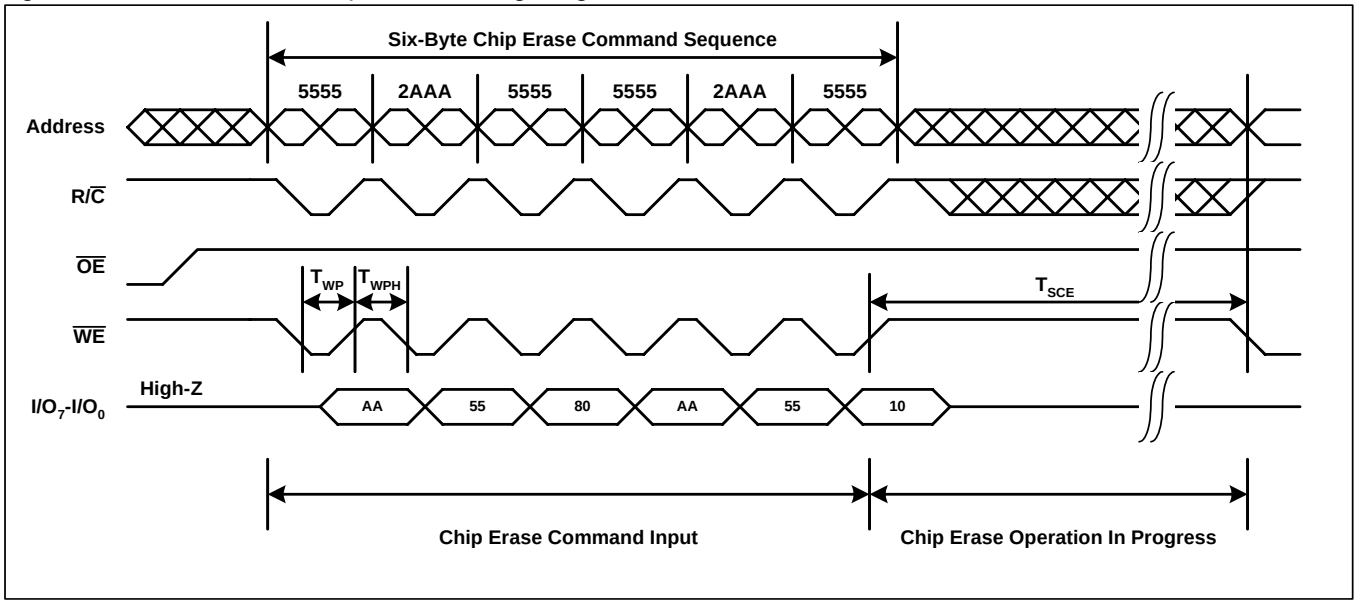



Figure 17: A/A Mux Mode Product ID Entry and Read Timing Diagram

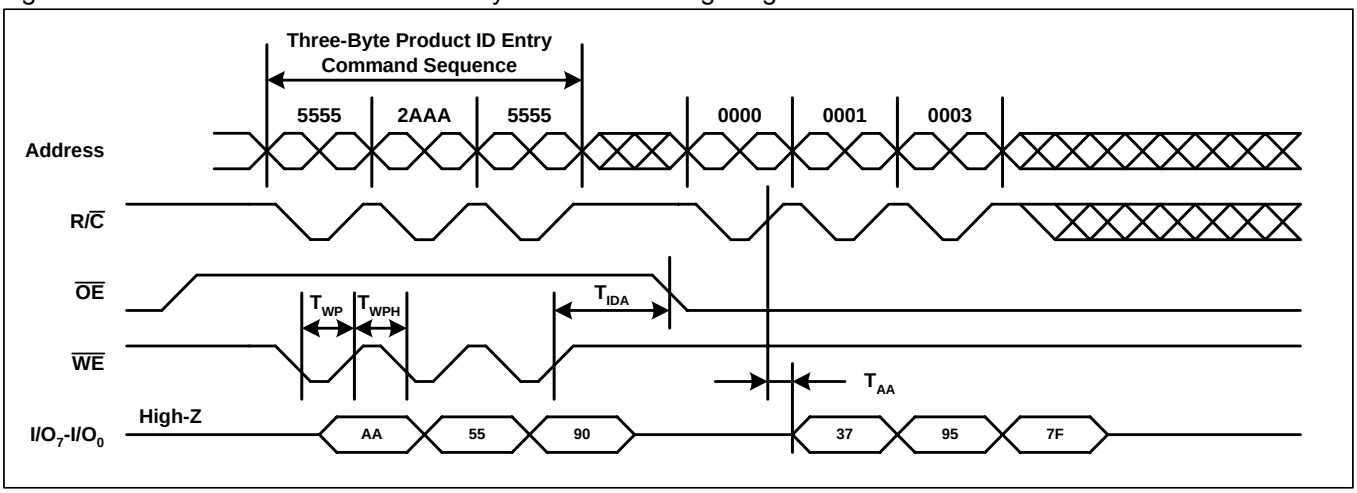



Figure 18: A/A Mux Mode Product ID Exit and Reset Timing Diagram

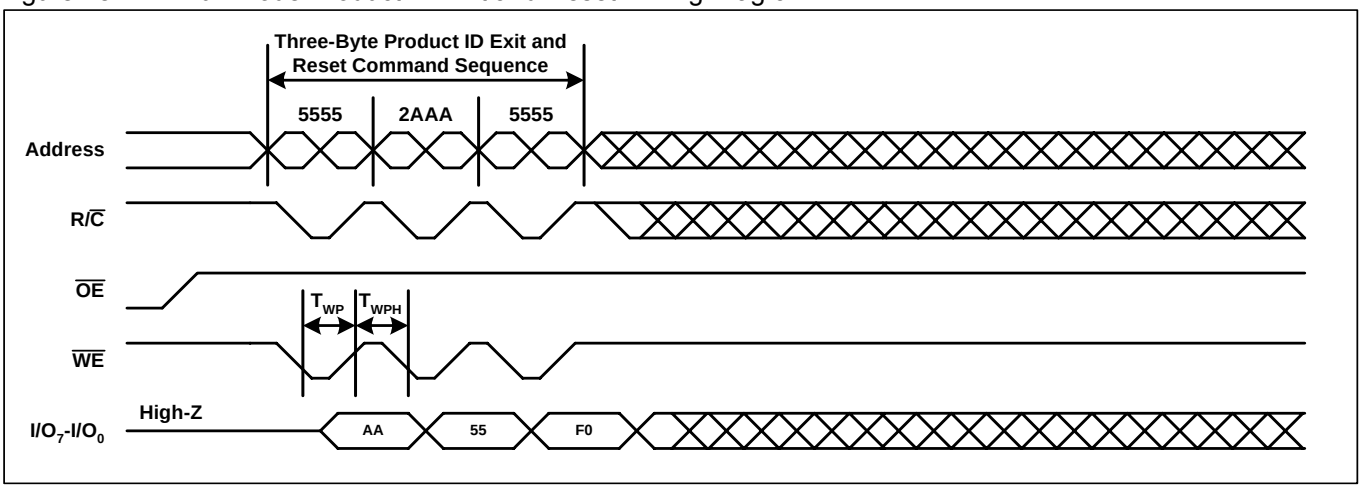


Figure 19: Automatic Byte Program Algorithm

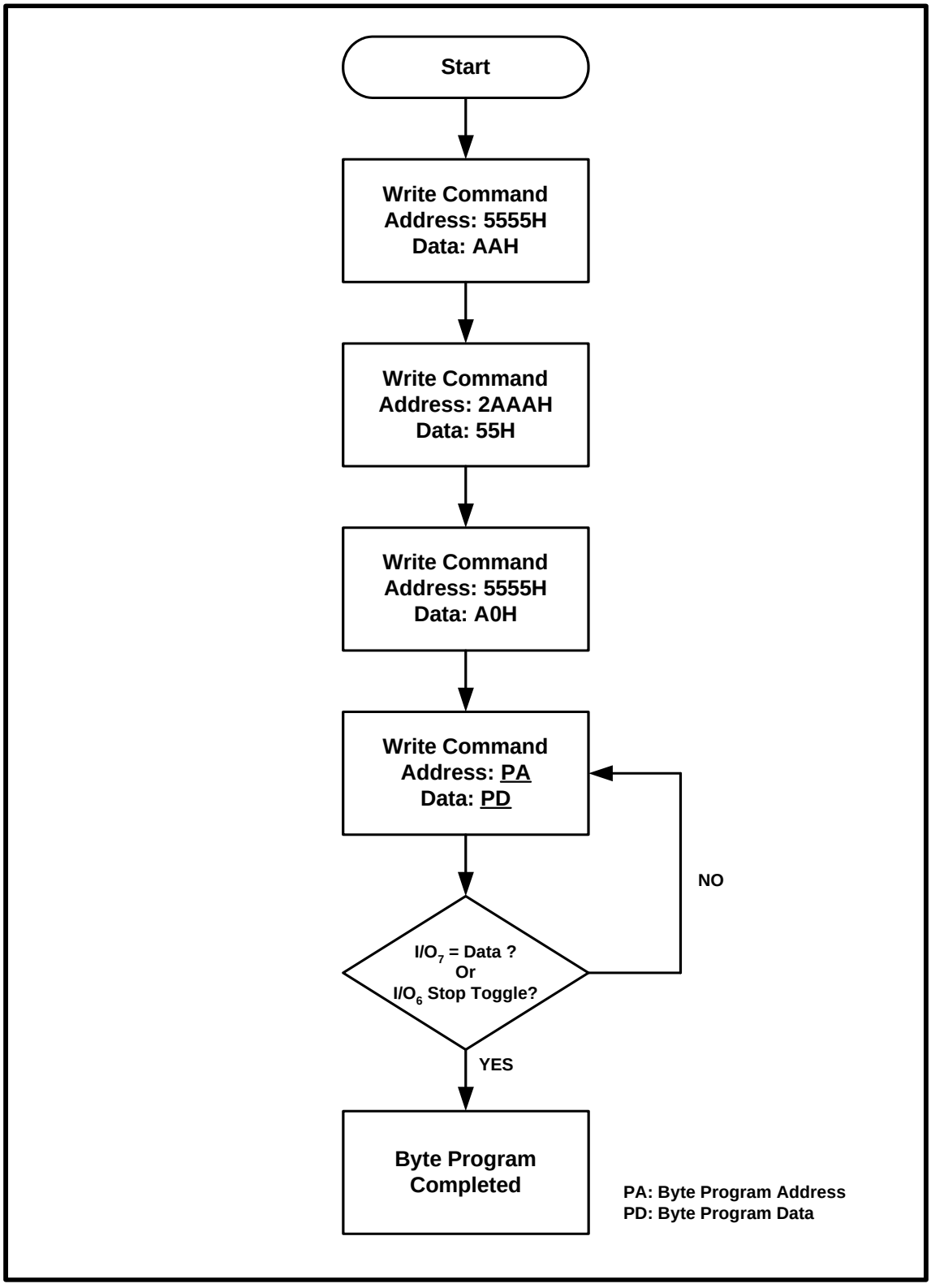


Figure 20: Automatic Block Erase Algorithm

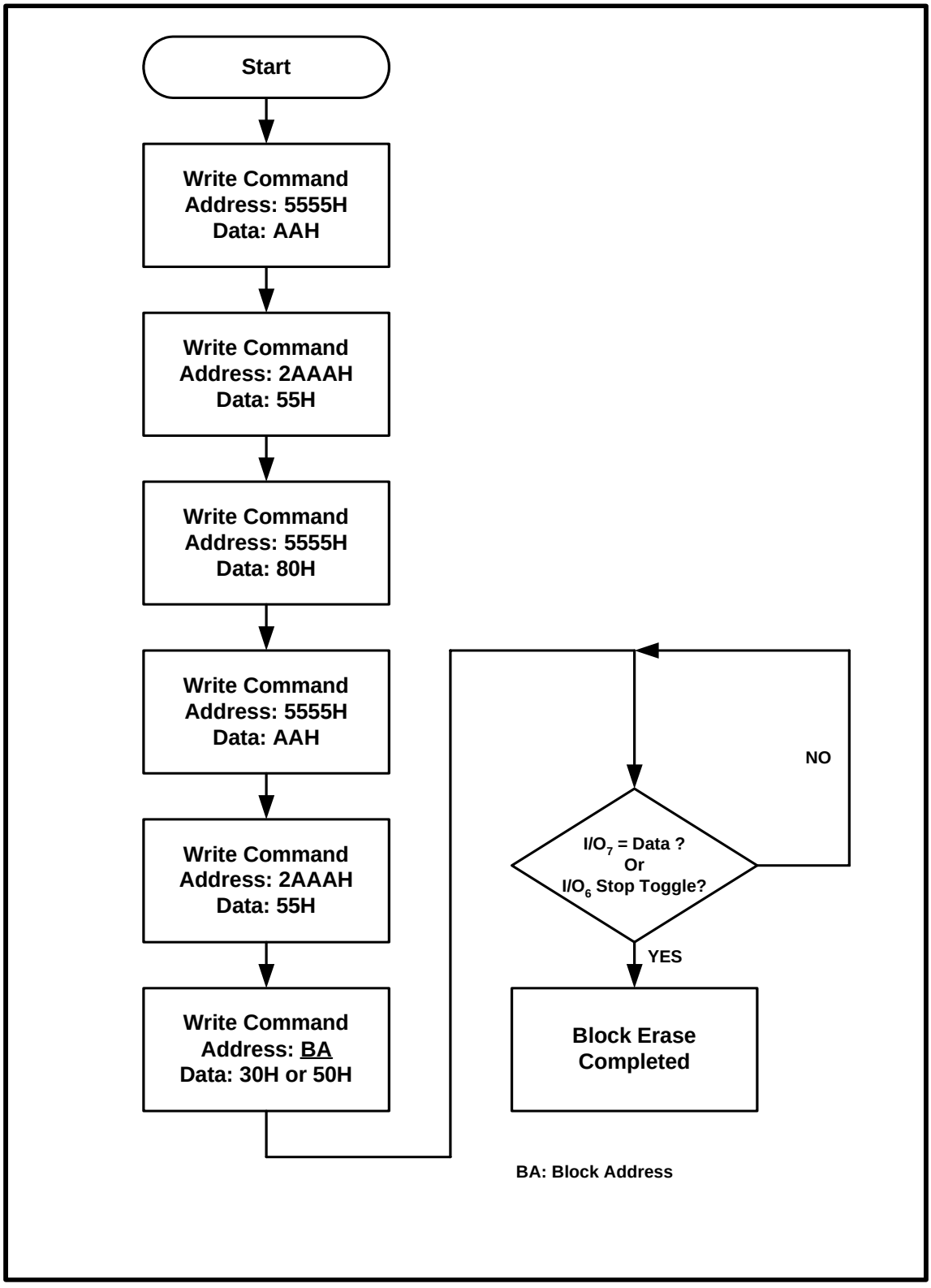


Figure 21: Automatic Chip Erase Algorithm

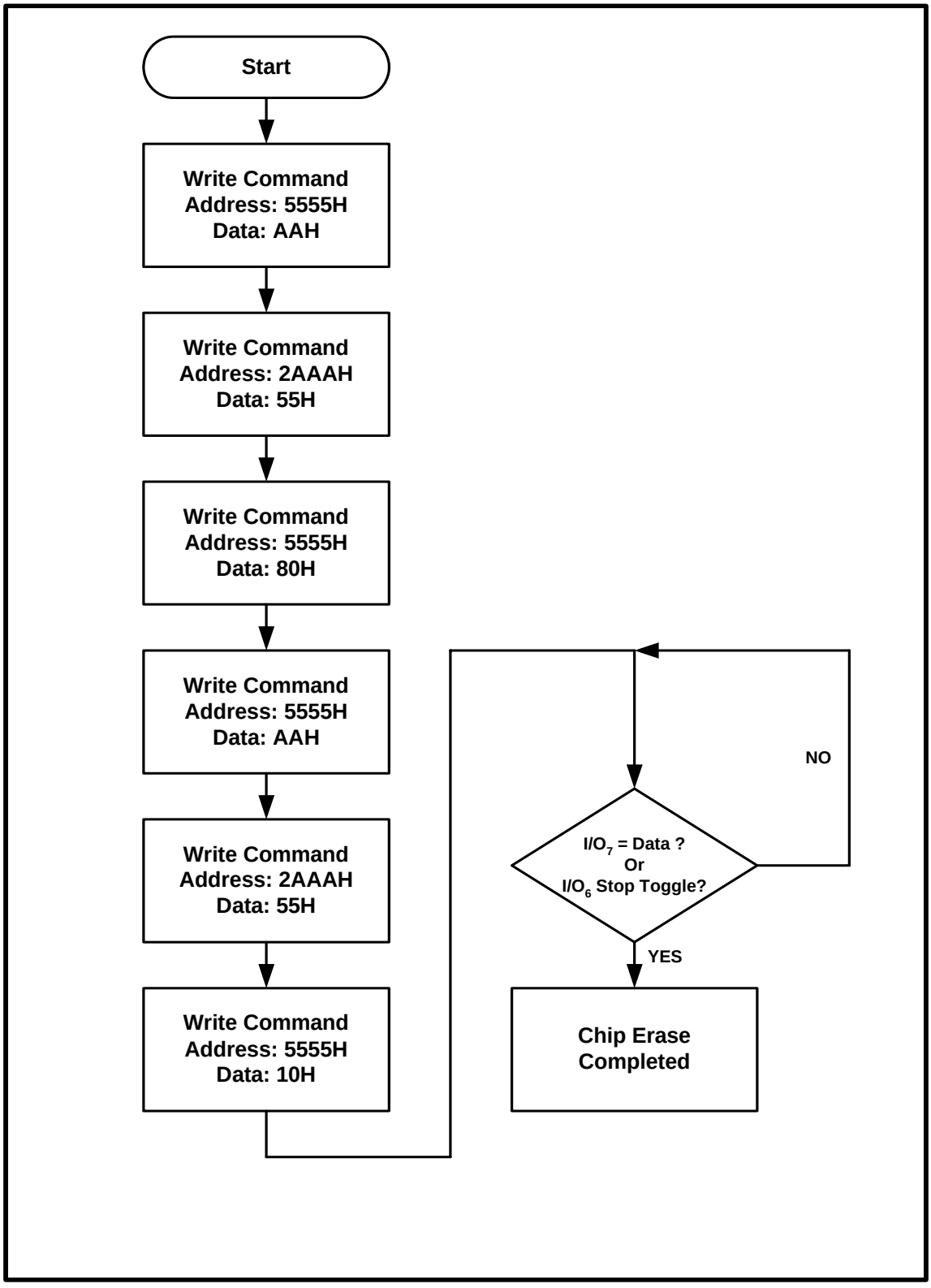
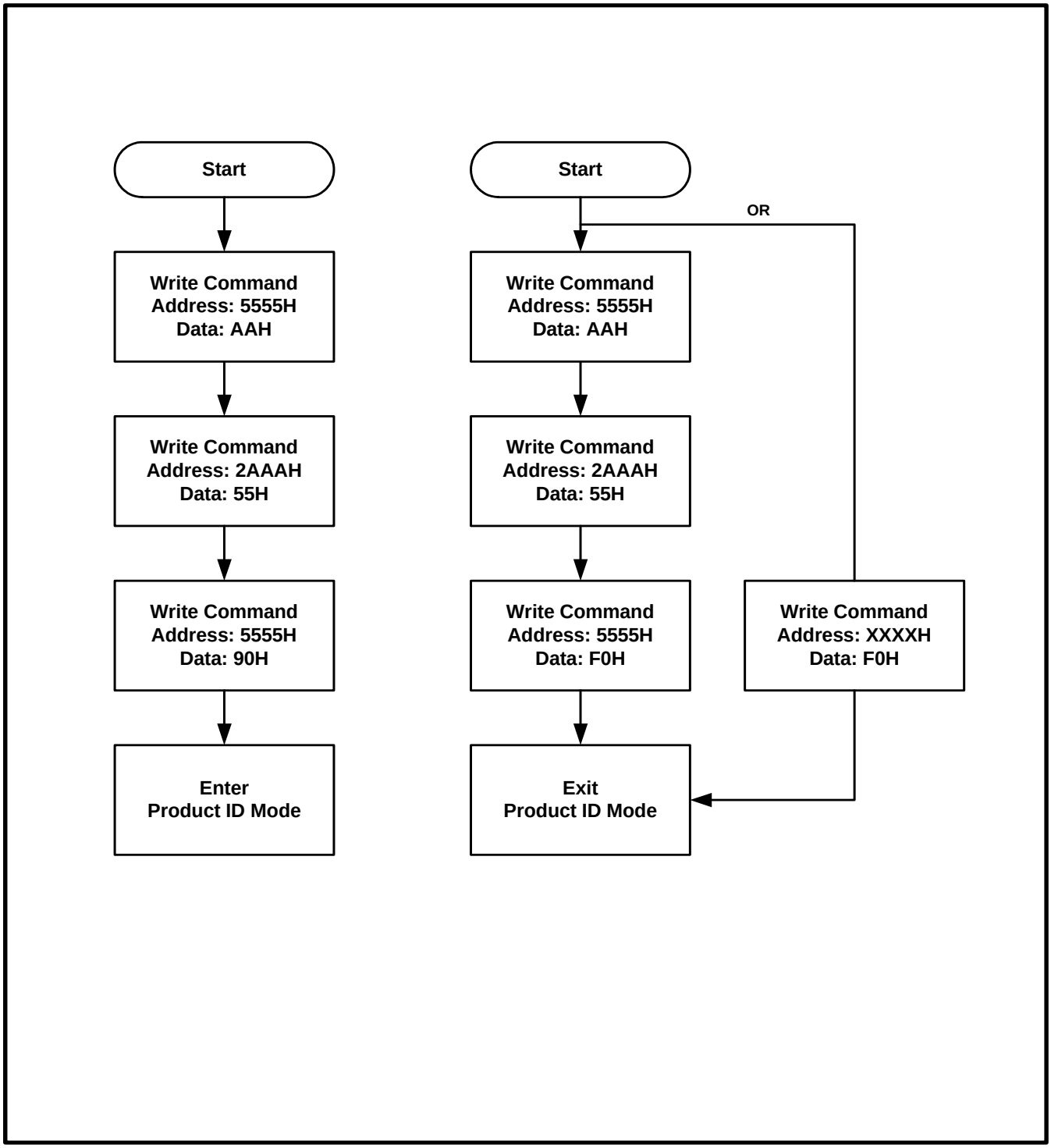
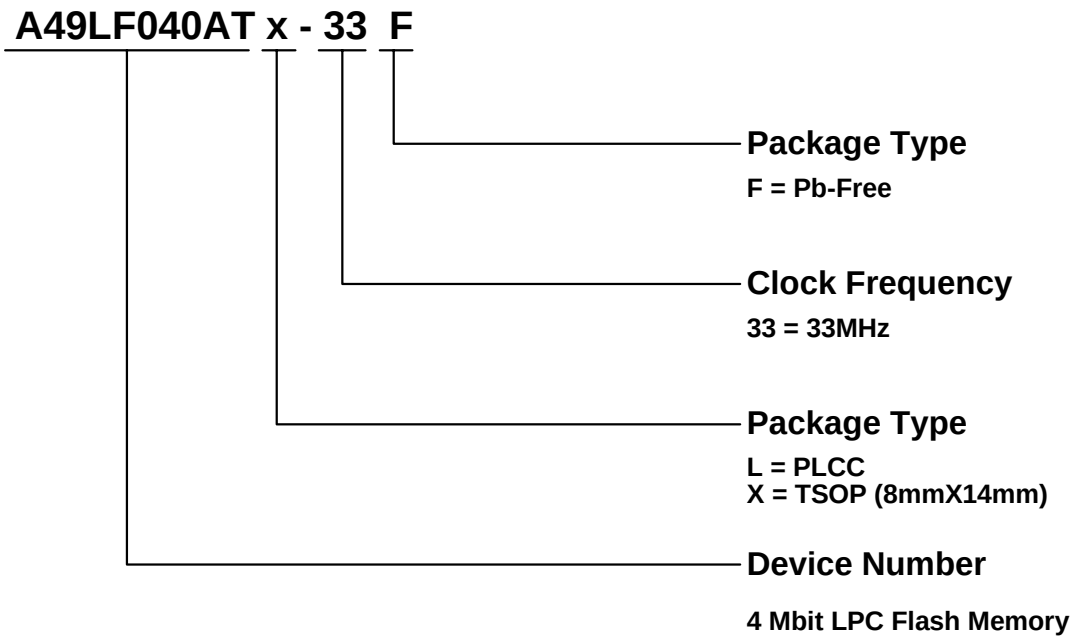


Figure 22: Product ID Command Flowchart



## Ordering Information

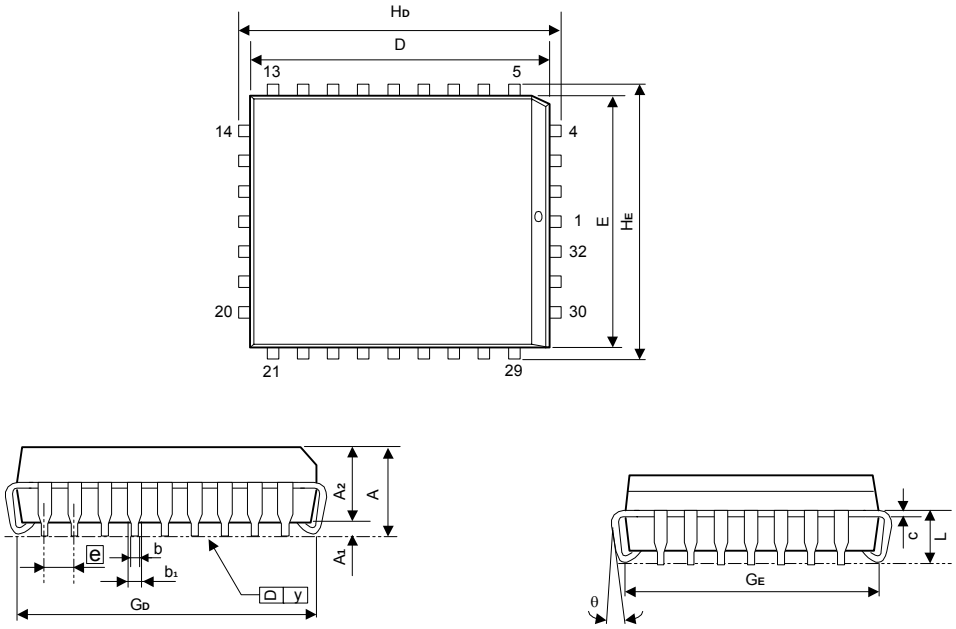



| Part No. | Clock Frequency (MHz) | Boot Block Location | Temperature Range | Package Type |
|---|---|---|---|---|
| A49LF040ATL-33 | 33 | Top | 0°C to +85°C | 32-pin PLCC |
| A49LF040ATL-33F | | Top | 0°C to +85°C | 32-pin Pb-Free PLCC |
| A49LF040ATX-33 | | Top | 0°C to +85°C | 32-pin TSOP (8mm X 14 mm) |
| A49LF040ATX-33F | | Top | 0°C to +85°C | 32-pin Pb-Free TSOP (8mm X 14 mm) |

## Package Information

### PLCC 32L Outline Dimension

unit: inches/mm

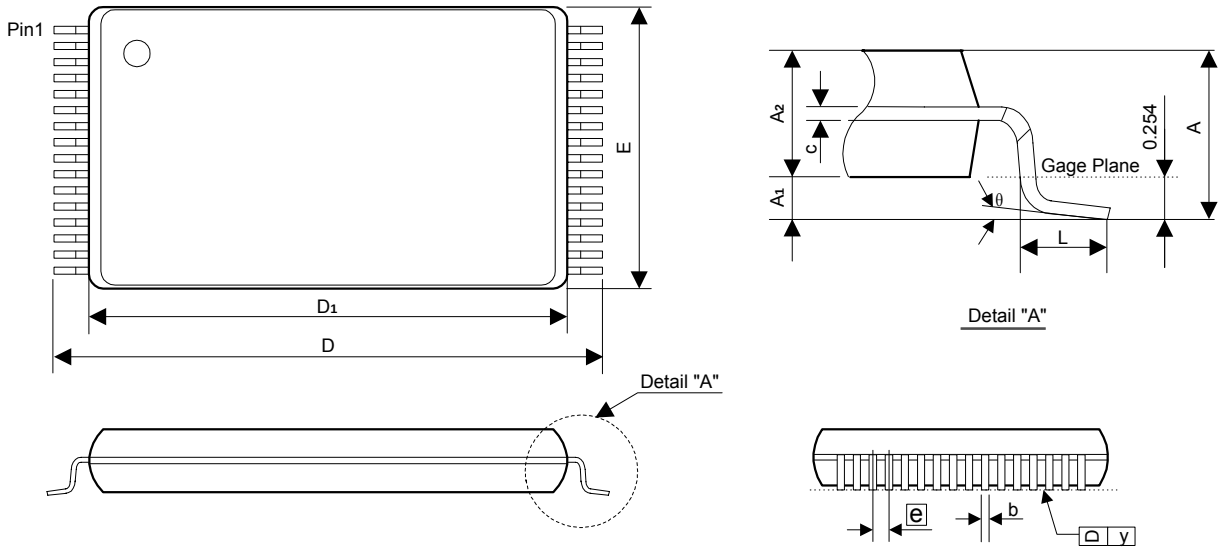



| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 0.134 | - | - | 3.40 |
| $A_1$ | 0.0185 | - | - | 0.47 | - | - |
| $A_2$ | 0.105 | 0.110 | 0.115 | 2.67 | 2.80 | 2.93 |
| $b_1$ | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| b | 0.016 | 0.018 | 0.021 | 0.41 | 0.46 | 0.54 |
| C | 0.008 | 0.010 | 0.014 | 0.20 | 0.254 | 0.35 |
| D | 0.547 | 0.550 | 0.553 | 13.89 | 13.97 | 14.05 |
| E | 0.447 | 0.450 | 0.453 | 11.35 | 11.43 | 11.51 |
| e | 0.044 | 0.050 | 0.056 | 1.12 | 1.27 | 1.42 |
| $G_D$ | 0.490 | 0.510 | 0.530 | 12.45 | 12.95 | 13.46 |
| $G_E$ | 0.390 | 0.410 | 0.430 | 9.91 | 10.41 | 10.92 |
| $H_D$ | 0.585 | 0.590 | 0.595 | 14.86 | 14.99 | 15.11 |
| $H_E$ | 0.485 | 0.490 | 0.495 | 12.32 | 12.45 | 12.57 |
| L | 0.075 | 0.090 | 0.095 | 1.91 | 2.29 | 2.41 |
| y | - | - | 0.003 | - | - | 0.075 |
| θ | 0° | - | 10° | 0° | - | 10° |

**Notes:**
1. Dimensions D and E do not include resin fins.
2. Dimensions $G_D$ & $G_E$ are for PC Board surface mount pad pitch design reference only.

## Package Information

**TSOP 32L TYPE I (8 X 14mm) Outline Dimensions** unit: inches/mm




| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 0.047 | - | - | 1.20 |
| $A_1$ | 0.002 | - | 0.006 | 0.05 | - | 0.15 |
| $A_2$ | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| b | 0.0067 | 0.0087 | 0.0106 | 0.17 | 0.22 | 0.27 |
| c | 0.004 | - | 0.0083 | 0.10 | - | 0.21 |
| E | 0.311 | 0.315 | 0.319 | 7.90 | 8.00 | 8.10 |
| e | - | 0.0197 | - | - | 0.50 | - |
| D | 0.543 | 0.551 | 0.559 | 13.80 | 14.00 | 14.20 |
| $D_1$ | 0.484 | 0.488 | 0.492 | 12.30 | 12.40 | 12.50 |
| L | 0.020 | 0.024 | 0.028 | 0.50 | 0.60 | 0.70 |
| y | 0.000 | - | 0.003 | 0.00 | - | 0.076 |
| θ | 0° | 3° | 5° | 0° | 3° | 5° |

**Notes:**
1. Dimension E does not include mold flash.
2. Dimension $D_1$ does not include interlead flash.
3. Dimension b does not include dambar protrusion.