1. General Description & Features

General Description

This device is Digital Image Signal Processor (ISP) for Security Camera System.
The main features are Adaptive Contrast Enhancer (ACE), External Line-Lock, 2D Noise Reduction, 2 Auto (AE, AWB) control, Y/C processor, OSD, Video Encoder and Embedded CPU are included to realize above features.

Features

Sensor Interface

- Resolution: 410/520K CCD (Sony, Sharp, Panasonic)
- S1S2 format 10-bit
- Interlace

Image Signal Processing

- High Resolution (700 TV line)
- External Line-Lock (w/o PLL control)
- Register control via COXITRON (Pelco)
- Digital Clamp (with Anti-smear)
- ACE(Digital WDR)
- De-Fog
- Auto Exposure Control (AE)
- Auto White Balance Control (AWB)
- Color Temperature Detection
- Enhanced Y/C Separator (De-Mosaic, De-Moiré)
- Linear Gamma Control (Input/out Gamma)
- HLC, BLC
- Hue controller (8-Way)
- Color Suppression (Edge, high/low light)
- OSD (Font, Line, Box on screen display)
- Defect Detection & Correction(256ea)
- Mirror function
- Edge Adaptive 2-D Digital Noise Reducer
- Smart IR LED controller(Auto dimming)
- Lens Shading correction
- Negative Image output
- Serial Key I/F
- CDS I/F

System feature

- Built-in AFE (Analog Front End)
- On-chip Encoder for CVBS
  - 1 channel on-chip DAC (9-bit)
- On-chip MCU (32-bit EISC core)
- External Serial Flash Memory

Power Management

- 3.3V I/O Power
- 3.3V Analog Power DAC
- 1.2V Internal Core Power and PLL

Operating Frequency

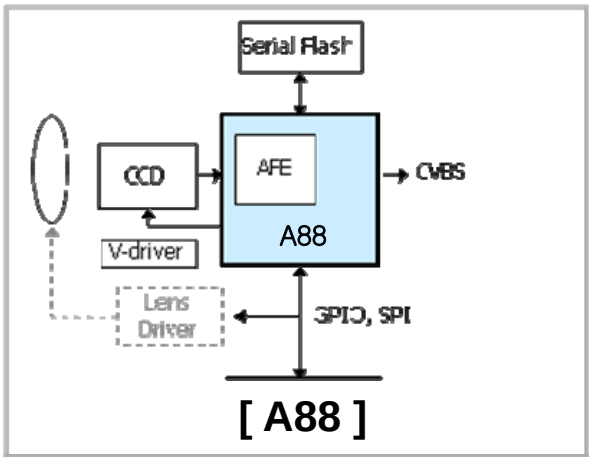
- Max.36MHz (core)

Operating Temperature

- -20˚C ~ +85˚C

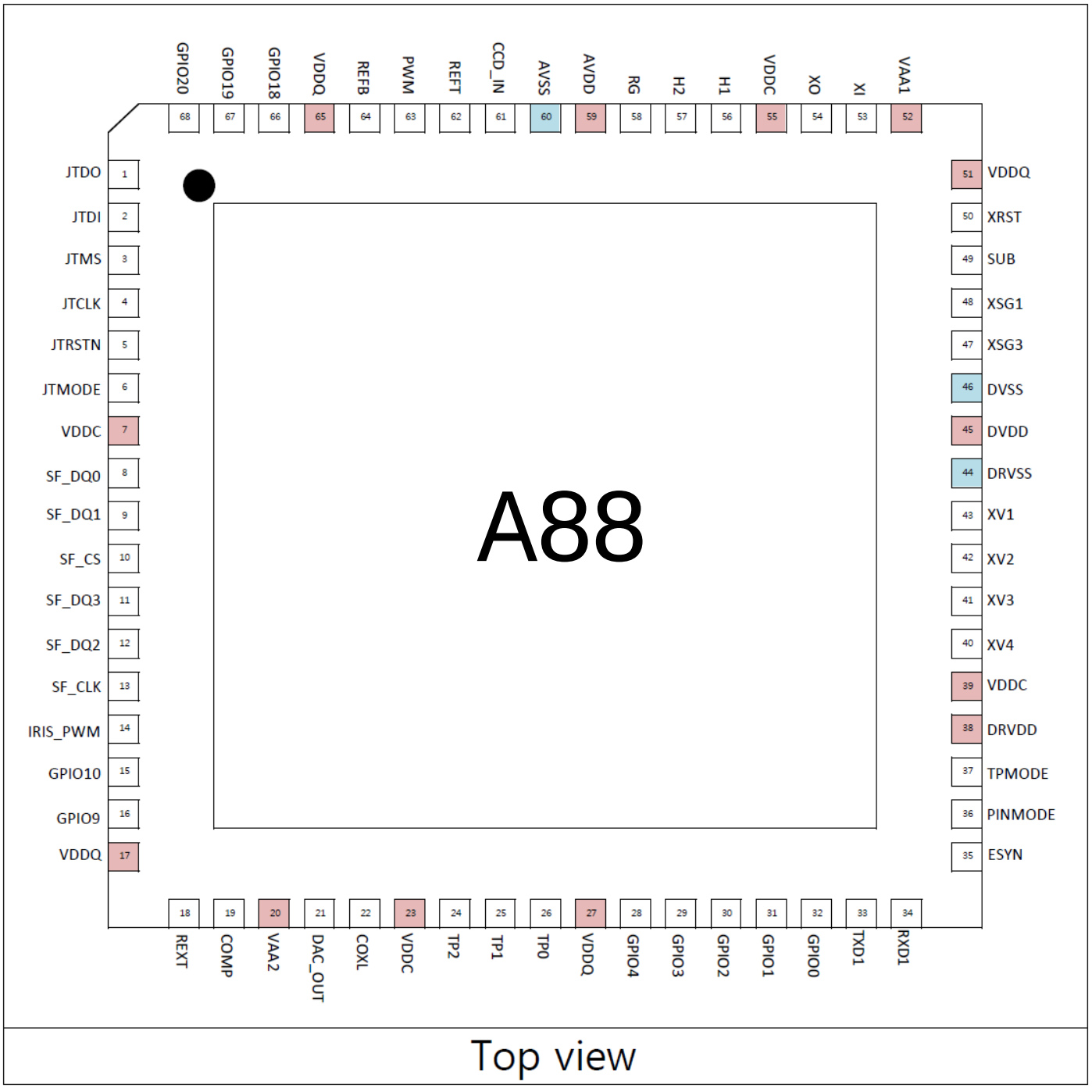
Package

- 0.4pitch: 8 X 8mm 68 Pin LGA



[A88]

2. Pin Diagram



Top view

3. I/O Information

SIDE	NO	PORT NAME	2'nd FUNC	3'rd FUNC	GPIO SPEC	Direction	VOLTAGE	설명	Note
LEFT	1	JTDO	SPDO	GPIO [14]	NORMAL GPIO	IO	VDDQ	Flash Download DO port	see table 1, PINMODE
	2	JTTDI	SPDI	GPIO [13]	NORMAL GPIO	I		Flash Download DI port	see table 1, PINMODE
	3	JTTMS	SPCS	GPIO [11]	NORMAL GPIO	I		Flash Download CS port	see table 1, PINMODE
	4	JTCLK	SPCK	GPIO [12]	NORMAL GPIO	I		Flash Download CLK port	see table 1, PINMODE
	5	JTRSTN				I		JTAG Reset port	"0" CPU sleep, "1" CPU working
	6	JTMODE				I		JTAG Mode sel port	"0" Flash download, "1" CPU working
	7	VDDC					1.2V	Core power	1.2V
	8	SF_DQ0				IO	VDDQ	Serial Flash DQ0 (DI)	External Flash I/F
	9	SF_DQ1				IO	VDDQ	Serial Flash DQ1 (DO)	External Flash I/F
	10	SFCSN				O	VDDQ	Serial Flash CS	External Flash I/F
	11	SF_DQ3				IO	VDDQ	Serial Flash DQ3 (HOLD#)	External Flash I/F
	12	SF_DQ2				IO	VDDQ	Serial Flash DQ2 (WP#)	External Flash I/F
	13	SF_CLK				O	VDDQ	Serial Flash clock	External Flash I/F
	14	IRIS_PWM	GPIO [21]			O	VDDQ	Logical PWM	
	15	GPIO [10]				IO	VDDQ	General purpose IO	
	16	GPIO [9]				IO	VDDQ	General purpose IO	
	17	VDDQ					3.3V	IO power	
BOTTOM	18	REXT						DAC external variable register pin. External 17.5kOhm connected.	
	19	COMP						DAC Compensation pin. External 10uF capacitor connected.	
	20	VAA2	DAC				3.3V	DAC Analog Power.	
	21	DAC_OUT				O	VAA2	DAC output. Connected with external 72 ohm register.	
	22	COXL				I		Pelco signal input port	
	23	VDDC					1.2V	Core power	
	24	TP2	GPIO [17]		CAP1	I		Test pin [2]	see table 2, TPMODE
	25	TP1	GPIO [16]		CAP0	I		Test pin [1]	see table 2, TPMODE
	26	TP0	GPIO [15]		NORMAL GPIO	I		Test pin [0]	see table 2, TPMODE
	27	VDDQ					3.3V	IO power	
	28	GPIO [4]			TSI_SCL	IO	VDDQ	General purpose IO	

	29	GPIO [3]			TWI_SDA	IO	VDDQ	General purpose IO	
	30	GPIO [2]			PWM2	IO	VDDQ	General purpose IO	
	31	GPIO [1]			PWM1	IO	VDDQ	General purpose IO	
	32	GPIO [0]			PWM0	IO	VDDQ	General purpose IO	
	33	TXD1				O	VDDQ	UART Transmitter	
	34	RXD1				I		UART Receiver	
RIGHT	35	ESYN				I		External sync signal input for line-lock	
	36	PINMODE				I		JTAG port function selection switch	see table 1
	37	TP_MODE				I		Test port function selection switch	see table 2
	38	DRVDD					3.3V	AFE digital output driver power	
	39	VDDC					1.2V	Core power	
	40	XV4				O	VDDQ	CCD vertical transfer pulse 4	
	41	XV3				O	VDDQ	CCD vertical transfer pulse 3	
	42	XV2				O	VDDQ	CCD vertical transfer pulse 2	
	43	XV1				O	VDDQ	CCD vertical transfer pulse 1	
	44	DRVSS						AFE digital output driver ground	
	45	DVDD					3.3V	AFE digital power	
	46	DVSS						AFE digital ground	
	47	XSG3				O	VDDQ	CCD sense gate pulse 3	
	48	XSG1				O	VDDQ	CCD sense gate pulse 1	
	49	XSUB				O	VDDQ	CCD sub pulse	
	50	XRST				I		A88 system reset signal	
	51	VDDQ					3.3V	IO power	
TOP	52	VAA1					1.2V	PLL analog power	
	53	XI	PLL			I		A88 X-tal clock input	
	54	XO				O		A88 X-tal clock output	
	55	VDDC					1.2V	Core power	
	56	H1				O	VDDT	CCD horizontal pulse	
	57	H2				O	VDDQ	CCD horizontal pulse	
	58	RG				O	VDDQ	CCD reset gate pulse	
	59	AVDD					3.3V	AFE analog power	
	60	AVSS						AFE analog ground	
	61	CCD_IN						Analog input from CCD	
	62	REFT						AFE top reference voltage decoupling	
	63	PWM				O	VDDQ	Random PWM for Smart IR	
	64	REFB						AFE bottom reference voltage decoupling	
	65	VDDQ					3.3V	IO power	
	66	GPIO [18]			CAP2	IO	VDDQ	General purpose IO	
	67	GPIO [19]			NORMAL GPIO	IO	VDDQ	General purpose IO	
	68	GPIO [20]			NORMAL GPIO	IO	VDDQ	General purpose IO	

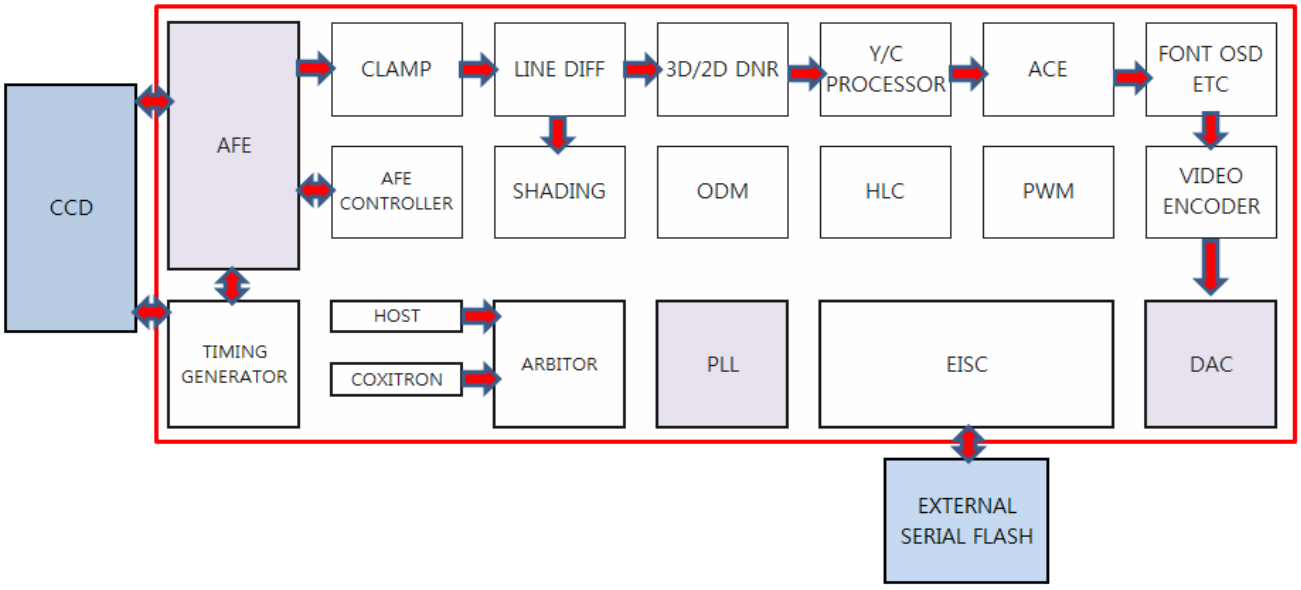
Table 1

PINMODE "1"		PINMODE “0”
comm_sel “1” ('default')	comm_sel “0”	
HD I	GPI13	JTTDI
HCS	GPI11	JTTMS
HCK	GPI12	JTTCLK
HDO	GPO14	JTTDO

Table 2

TPMODE "1"	TPMODE "0"
TP[2]	GPI [17]
TP[1]	GPI [16]
TP[0]	GPI [15]

4. Block Diagram



5. ELECTRICAL CHARATERISTICS

A. Absolute maximum rating

Symbol	Parameter	Rating		Unit
VDDC	DC supply voltage	1.08	1.32	V
VDDQ		3.0	3.63	
F_{max}	Max operating frequency	36 for 520K NTSC (36 for 520K PAL)		MHz
		28.6363 for 410K NTSC (28.375 for 410K PAL)		
T_{stg}	Storage temperature	-40 ~ 125		℃
T_{opr}	Operating temperature	-20 ~ 85		℃

Table 1

B. Recommended operation conditions

Symbol	Parameter	Rating	Unit
VDDC	DC supply voltage for Logic	1.2 ± 0.12	V
VDDQ	DC supply voltage for I/O	3.3 ± 0.33	
VAA1	DC supply voltage for PLL	1.2 ± 0.12	
VAA2	DC supply voltage for DAC	3.3 ± 0.33	
F_{typ}	Typical operating frequency	36	MHz

Table 2

C. Static characteristics

	Pin	Target	Unit
HBM (Human Body Model)	All	± 2000	V
MM (Machine Model)	All	± 200	V

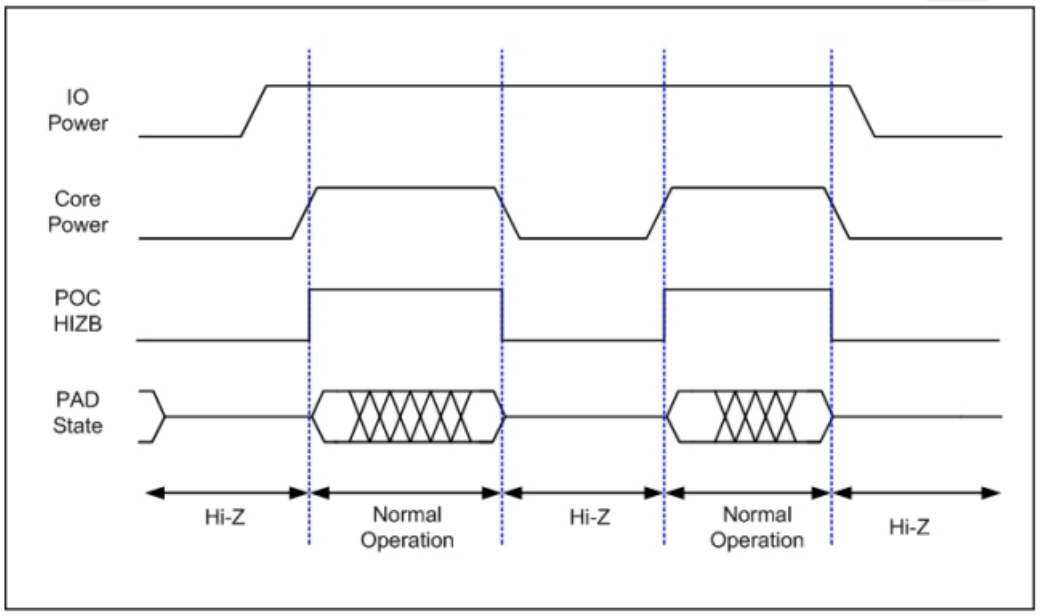
D. I/O DC Characteristic

PARAMETER		MIN	TYP	MAX	Unit
DVDD	3.3 IO supply voltage	3.0	3.3	3.6	V
T	Temperature	-40	25	125	C
VIL	Input low voltage	-0.3	-	0.3*DVDD	V
VIH	Input high voltage	0.7*DVDD	-	4	V
ΔV	Schmitt trigger hysteresis		0.1*DVDD		V
VOL	Output low voltage	-	-	0.2	V
VOH	Output high voltage	DVDD-0.2	-	-	V
IOL	Low level output current			-200	uA
IOH	High level output current	200			uA

E. I/O Pull-up Resistances

DVDD	Min	Typ	Max	Unit
3.3V IO Supply Voltage	30	45	73	KΩ

F. Power on sequence



Power on : High voltage in the order of (3.3V -> 1.2V) power on sequence

Power off : Low voltage in the order of (1.2V -> 3.3V) power off sequence

G. Power consumption

	Current	Voltage
Core Power (with PLL)	TBD	1.2 V
IO Power (with DAC)	TBD	3.3 V
AFE	TBD	3.3V
Wafer total	TBD	
Package total	TBD	

6. Function Description

A. TG BLOCK

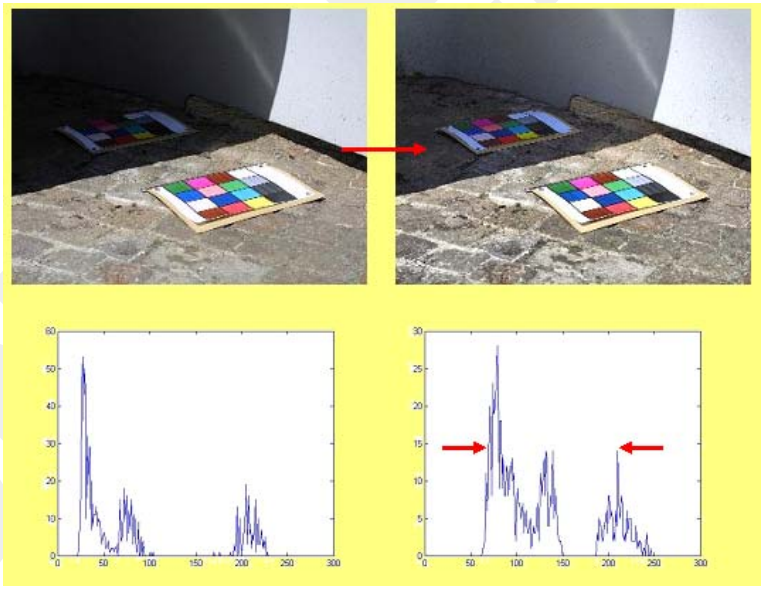
- 520K/410K (4-phase) signal for driving CCD and CDS/AGC stage of the input signal is generated.
- Supports NTSC/PAL
- Separate very high shutter interval is possible without fine tuning the entire length of exposure.
- Exposure of the 1H interval can be controlled up to 256 step intervals.

B. DIGITAL CLAMP BLOCK

- This function is to compensate for the instability of the CCD while following operating standards LEVEL.
- With reference to the CCD's OB BLANK section (interval), can adjust Image Data level Offset.
- CCD's SMEAR correction is possible.

C. ACE BLOCK

- In situation as shown, the dark areas of shadows/listings in large image are compensated as it has the ability to preserve the listings data.

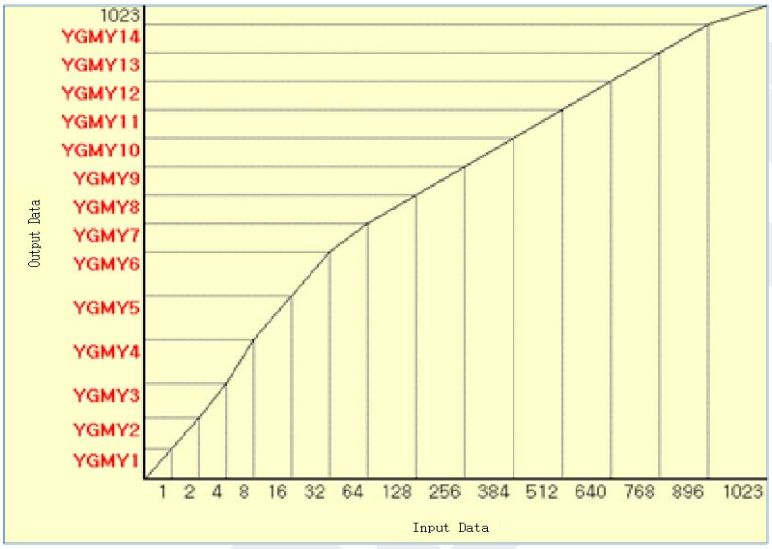


D. COLOR CORRECTION BLOCK

- When Cr/Cb and Y enter, this block generates RGB using the relation between Cr/Cb and Y.
- As the FULL BIT RESOLUTION input from CCD is used, the DATA loss is less.
- Built-in function to adjust the BLACK BALANCE.

E. GAMMA BLOCK

- If ISP input image is too dark, INPUT GAMMA exists for compensation.
- In order to compensate the GAMMA characteristics of the display device, OUTPUT GAMMA exists.
- Simple compensation of INPUT GAMMA is achieved through GAIN CONTROL.
- Compensation is achieved in a way that directly controls the conversion function with a 16-point OUTPUT GAMMA.

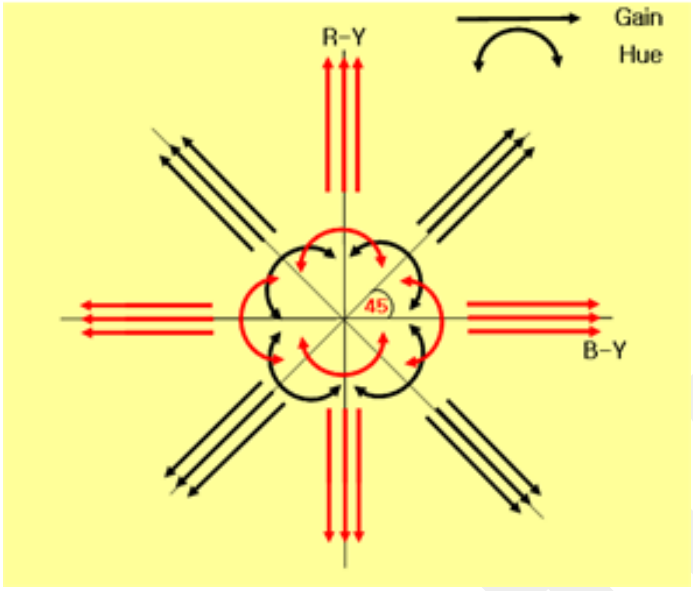


F. APERTURE BLOCK

- This block strengthens the composition of the image by increasing the image resolution.
- In order to prevent noise increase in low light, the differential of APERTURE GAIN shall be applied accordingly. THRESHOLD interval is divided according to the Y-level, GAIN settings may be different from one another.
- Adaptive Directional Filter improves vertical, horizontal edge components.

G. HUE CONTROL BLOCK

- As the R-Y, B-Y signals, output from CCD do not have ideal spectral characteristics, HUE CONTROL BLOCK provides Error Controls.
- Chrominance signal GAIN and HUE can be adjusted.
- GAIN, HUE configuration can be controlled in all 8 directions. Also, control area is divided into 4 sections of chrominance signals in order to control only certain areas of the chrominance signal.
- 8-way GAIN / 8-way HUE / 4 Area Control.



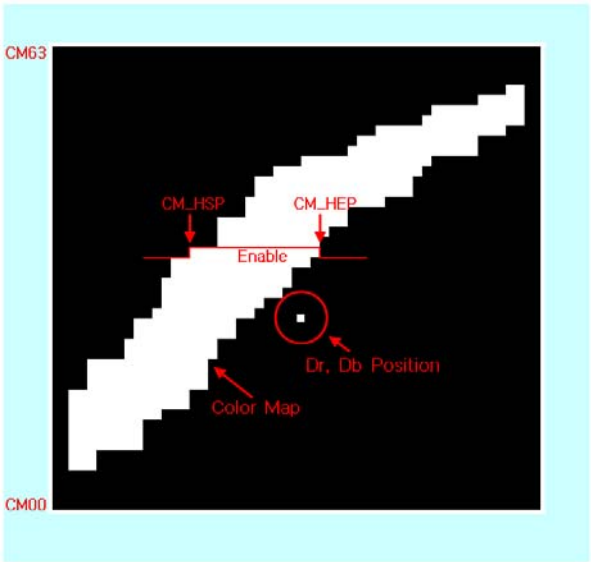
H. COLOR SUPPRESSION BLOCK

- Reduces the chrominance that is generated in EDGE components.
- Provides COLOR SUPPRESSION in areas of poor light conditions and saturated areas.

I. ODM BLOCK

Baseline data for AE/AWB is provided.

- If six AE windows have been provided, AE DATA for each window can be obtained. Histogram of only one WINDOW can be obtained.
- There is a COLOR MAP MASKING method for detecting white zone.



J. OSD BLOCK

- OSD (Output Screen Display) Output on screen is possible using the Font register.
- Address allocation for Font register is as follows.

Address	Name	R/W	Depth
	Font Control Register	R/W	
0x0600 ~ 0x07FF	Font ID Register	W Only	512 EA
0x0800 ~ 0x09FF	Font Attribute Register	W Only	512 EA
0x0A00 ~ 0x1BFF	Font Character Register	W Only	4608 Address

- **FONT ID:** Write to Display the ID of the Font. Area of one FONT ID Address occupies a position on one screen, values of register that correspond to write a value in the Point Font is imported. Font ID Memory pointed to by the memory Font Character imports the corresponding position in the Display Font Data User has saved here. Below is the MEMORY MAP of FONT ID.

Address	BIT[31:24]	BIT[23:16]	BIT[15:8]	BIT[7:0]
0x600	Reserved	Reserved	Reserved	0 Position
0x601	Reserved	Reserved	Reserved	1 Position
0x602	Reserved	Reserved	Reserved	2 Position
0x603	Reserved	Reserved	Reserved	3 Position
0x604	Reserved	Reserved	Reserved	4 Position
~	Reserved	Reserved	Reserved	~
0x61F	Reserved	Reserved	Reserved	31 Position
0x620	Reserved	Reserved	Reserved	32 Position
0x621	Reserved	Reserved	Reserved	33 Position
0x623	Reserved	Reserved	Reserved	34 Position
~	~	~	~	~
0x6CD	Reserved	Reserved	Reserved	205 Position
0x6CE	Reserved	Reserved	Reserved	206 Position
0x6CF	Reserved	Reserved	Reserved	207 Position
0x6D0	Reserved	Reserved	Reserved	208 Position
~	~	~	~	~
0x7FF	Reserved	Reserved	Reserved	511 Position

- **FONT ATTRIBUTE:** This memory specifies the attributes of the FONT. FONT ID is used to specify the color and background of the FONT. Following is the description of each bit of FONT ATTRIBUTE

속성 bit	Name	Feature
[23:16]	Y level	Font color selection
[15:8]	Cb level	
[7:0]	Cr level	

- **FONT CHARACTER:** User uses Bitmap Style by setting the FONT, which is stored to memory. One FONT is configured using 18 Address configurations. FONT stored start address of the memory will be increased by a factor of 18. The following is a memory for storing FONT MAP.

Address	BIT[31:28]	BIT[27:16]	BIT[15:12]	BIT[11:0]
0xa00	Reserved	Reserved	Reserved	Font 1 Line
0xa01	Reserved	Reserved	Reserved	Font 2 Line
0xa02	Reserved	Reserved	Reserved	Font 3 Line
0xa03	Reserved	Reserved	Reserved	Font 4 Line
0xa04	Reserved	Reserved	Reserved	Font 5 Line
0xa05	Reserved	Reserved	Reserved	Font 6 Line
0xa06	Reserved	Reserved	Reserved	Font 7 Line
0xa07	Reserved	Reserved	Reserved	Font 8 Line
0xa08	Reserved	Reserved	Reserved	Font 9 Line
0xa09	Reserved	Reserved	Reserved	Font 10 Line
0xa0a	Reserved	Reserved	Reserved	Font 11 Line
0xa0b	Reserved	Reserved	Reserved	Font 12 Line
0xa0c	Reserved	Reserved	Reserved	Font 13 Line
0xa0d	Reserved	Reserved	Reserved	Font 14 Line
0xa0e	Reserved	Reserved	Reserved	Font 15 Line
0xa0f	Reserved	Reserved	Reserved	Font 16 Line
0xa10	Reserved	Reserved	Reserved	Font 17 Line
0xa11	Reserved	Reserved	Reserved	Font 18 Line
0xa12	Reserved	Reserved	Reserved	Next font 1 line
0xa13	Reserved	Reserved	Reserved	Next font 2 line

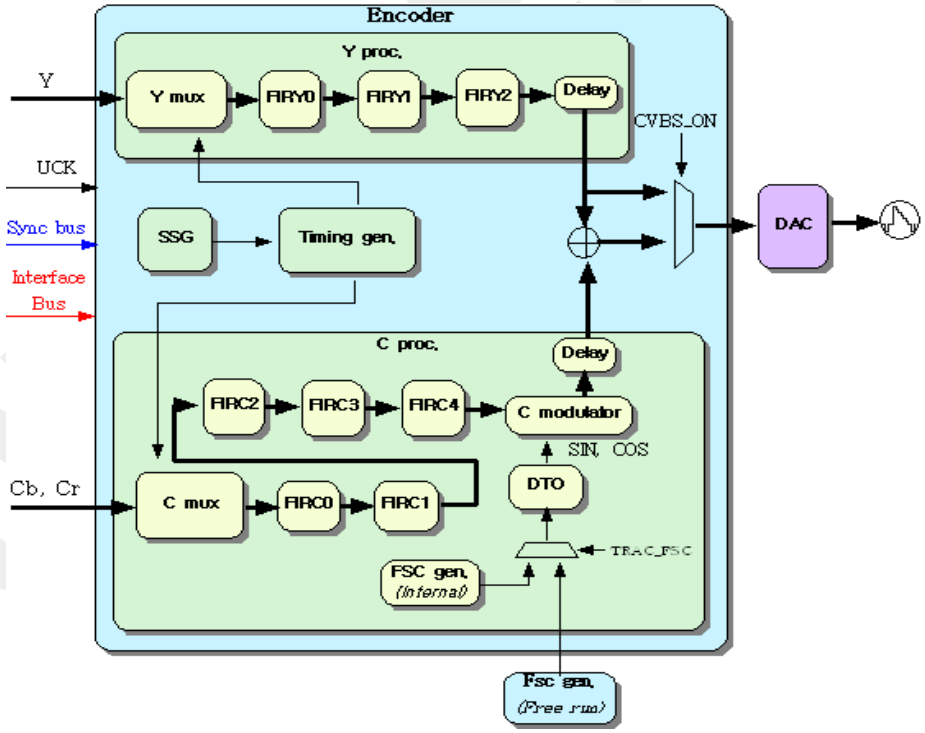
- As shown in the table above, the memory is set to see the figure in the next chapter, and at corresponding address User desired Font Bit Map can be written.

Line	11	10	9	8	7	6	5	4	3	2	1	0	Register Address / Bit
1	0	0	0	0	0	0	0	0	0	0	0	0	0x0a00 / BIT[11:0]
2	0	0	0	0	0	0	0	0	0	0	0	0	0x0a01 / BIT[11:0]
3	0	0	0	0	1	1	1	1	0	0	0	0	0x0a02 / BIT[11:0]
4	0	0	0	0	1	1	1	1	0	0	0	0	0x0a03 / BIT[11:0]
5	0	0	0	0	0	1	1	0	0	0	0	0	0x0a04 / BIT[11:0]
6	0	0	0	0	0	1	1	0	0	0	0	0	0x0a05 / BIT[11:0]
7	0	0	0	0	0	1	1	0	0	0	0	0	0x0a06 / BIT[11:0]
8	0	0	0	0	0	1	1	0	0	0	0	0	0x0a07 / BIT[11:0]
9	0	0	0	0	0	1	1	0	0	0	0	0	0x0a08 / BIT[11:0]
10	0	0	0	0	0	1	1	0	0	0	0	0	0x0a09 / BIT[11:0]
11	0	0	0	0	0	1	1	0	0	0	0	0	0x0a0a / BIT[11:0]
12	0	0	0	0	0	1	1	0	0	0	0	0	0x0a0b / BIT[11:0]
13	0	0	0	0	0	1	1	0	0	0	0	0	0x0a0c / BIT[11:0]
14	0	0	0	0	0	1	1	0	0	0	0	0	0x0a0d / BIT[11:0]
15	0	0	0	0	1	1	1	1	0	0	0	0	0x0a0e / BIT[11:0]
16	0	0	0	0	1	1	1	1	0	0	0	0	0x0a0f / BIT[11:0]
17	0	0	0	0	0	0	0	0	0	0	0	0	0x0a10 / BIT[11:0]
18	0	0	0	0	0	0	0	0	0	0	0	0	0x0a11 / BIT[11:0]

- The above example depicts the Memory Font one 0xa00 ~ 0xa11. Similarly, one of the characters can be represented in 0x812 ~ 0x823. In this way, you can store up to the end of the Font area.

K. Encoder block

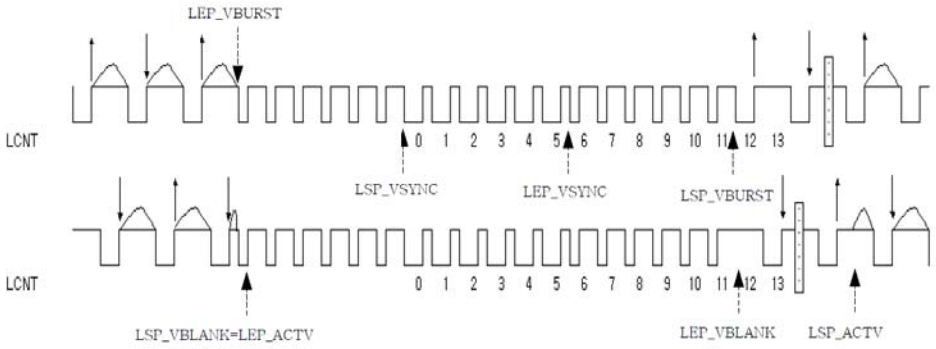
- Encoder block can be expressed as the following diagram.



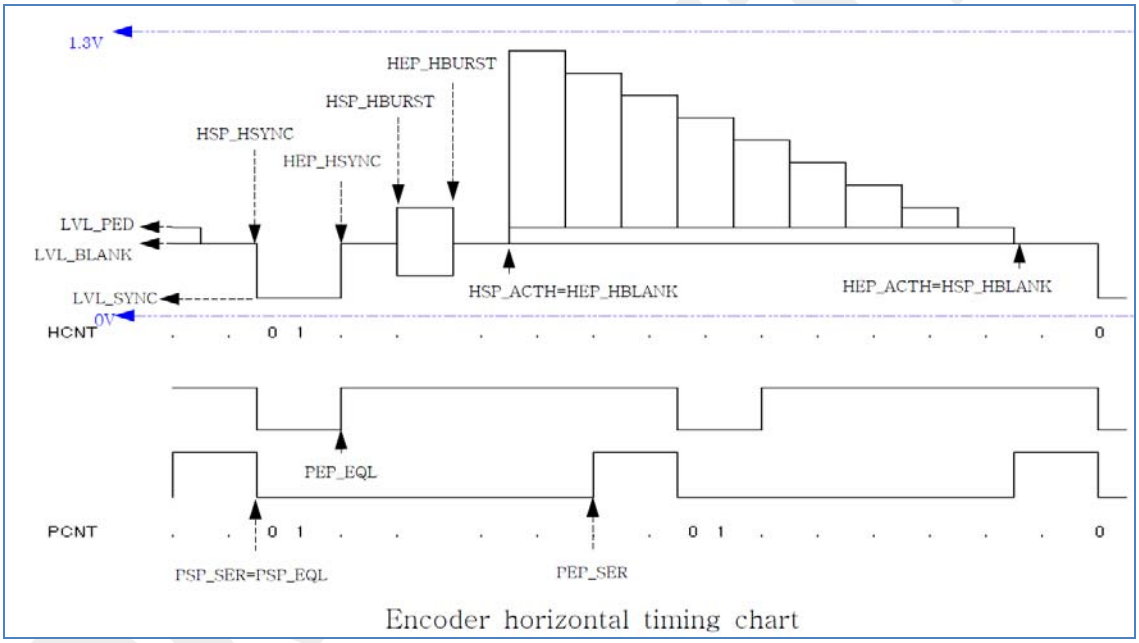
- SSG Block
  1. Starting from Sync bus, if EVD/EHD/EPD input is received, Encoder relevant registers can specify the value of the counter based on internal COUNTER generated BLOCK.

- Timing Generation Block

1. In CVBS signal format, to generate the internal timing, as part, Vertical blank/Horizontal blank/ Burst gate/Serration & Equalization and the actual Active video output interval are generated.
2. Timing diagram is shown below.

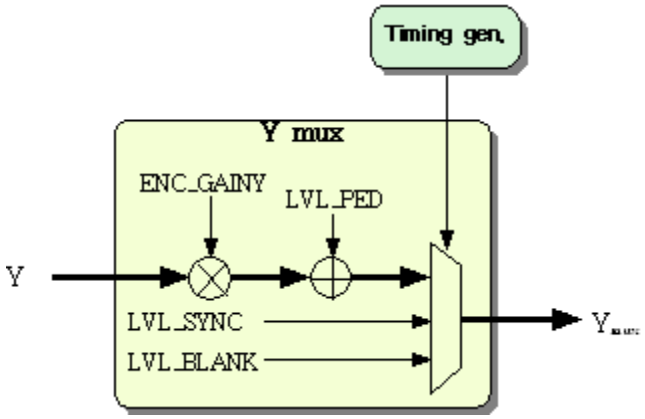


Encoder vertical timing chart



Encoder horizontal timing chart

- Y proc block
  1. Y mux block
     i. Timing generation block generates signals (Sync, Blank, Serration, Equalization, Video Active), according to output data selection and video output section, Y (luminance) is amplified by ENC_GAINY times and Pedestal level is added which is the final luminance output.



ii.Video segments from the output data is produced by the following equation.

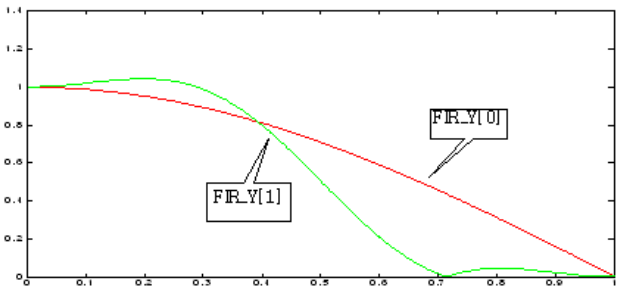
A. Ymax = Y x ENC_GAINY + LVL_PED

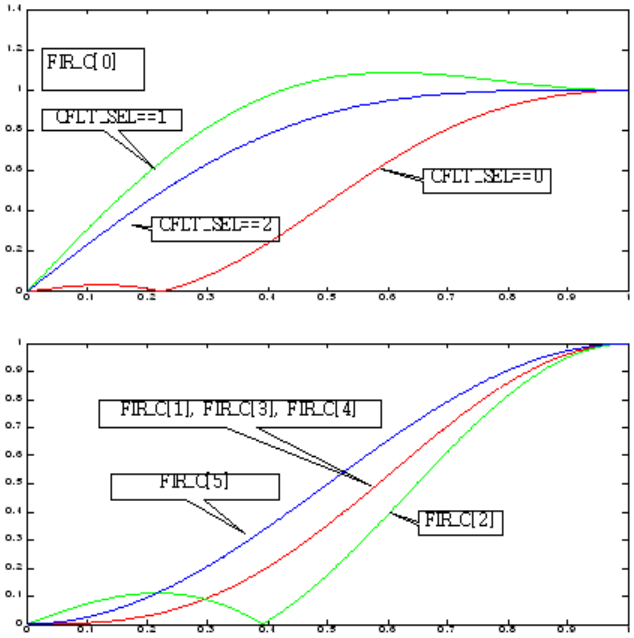
2. FIR (Finite Impulse Response) block

i.To perform the functions of moving average filter, by FIRY_ON, FIRC_ON filter on/off is possible.

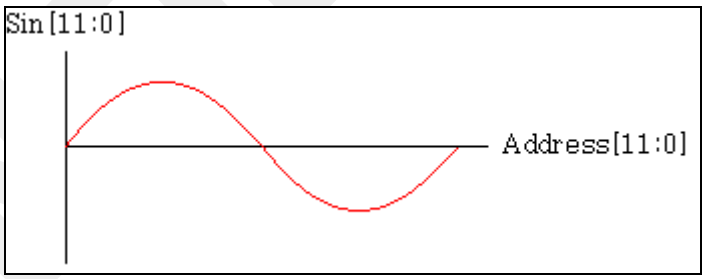
	Filter On/Off	Filter select	Filter Value
Y	FIRY_ON[0]	-	[1 1]
	FIRY_ON[1]	-	[-1 0 5 8 5 0 -1]
C	FIRC_ON[0]	CFLT_SEL==0	[-1 5 8 5 -1]
		CFLT_SEL==1	[-1 6 -1]
		CFLT_SEL==2	[-1 10 -1]
	FIRC_ON[1]	-	[1 2 1]
	FIRC_ON[2]	-	[1.5 1 1.5]
	FIRC_ON[3]	-	[1 2 1]
	FIRC_ON[4]	-	[1 2 1]
	FIRC_ON[5]	-	[1 1]

ii. The figure below shows characteristics of Y (Luminance) and C (Color) components for each of the filter coefficients.





- FSC generation block
  1. FSC gen block: Color composition (Cb, Cr) for the modulation of luminance signal, subcarrier needs to be generated. For this, Sine/Cosine table addresses are generated. The actual Sine/Cosine curve generated is fed to the DTO block.
  2. DTO (Discrete Time Oscillator): Address accredited by FSC gen block, block that generates Sine/Cosine curve has built-in sine table ROM of 512 and resolution is 12-bit.



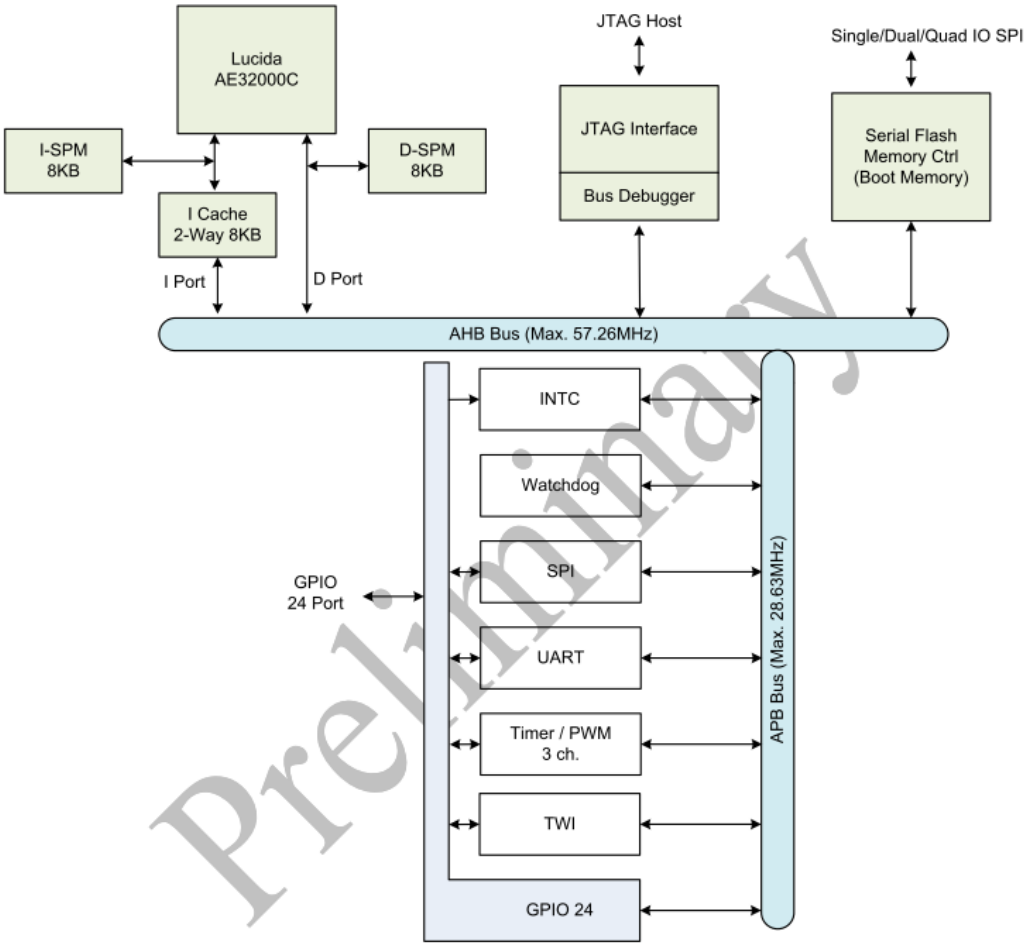
L. CPU BLOCK

- A 32-bit microcontroller operates a SINGLE / QUAD TYPE SERIAL FLASH mounted on the outside.
- Operation is set up to 57.26MHz.
- CPU's implementation has independent access to program memory and data memory (Harvard Architecture). Due to five stage pipeline structure of EISC, very fast command processing is performed.
- Through JTAG PROGRAMMING, download of program is faster than existing.
- 32BIT EISC ARCHITECTURE
  1. AE3200C
  2. Up to 58 MIPS throughout at 58MHz

3. 8KB 2-way instruction cache

- Embeded Memory
  1. 8Kbyte internal ISPM
  2. 8Kbyte internal DSPM
- Special Function
  1. Serial flash memory access
     i. SPI bus operation mode 0 (0,0) and mode 3 (1,1)
     ii. Support quad, single data access
- Peripherals
  1. 32 bit watch-dog timer
  2. 3 channel 16 bit timer/counter with 15 bit pre-scaler, capture, PWM
  3. 1 channel UART with 16 Byte FIFO, functionally compatible with the 16550
  4. 1 channel Master/Slave SPI with 8Byte FIFO
  5. Bus debugger with JTAG interface

- Block diagram



- For more information, refer to EISC manual ‘A88_CPU_datasheet_v0.0’

7. Register Map

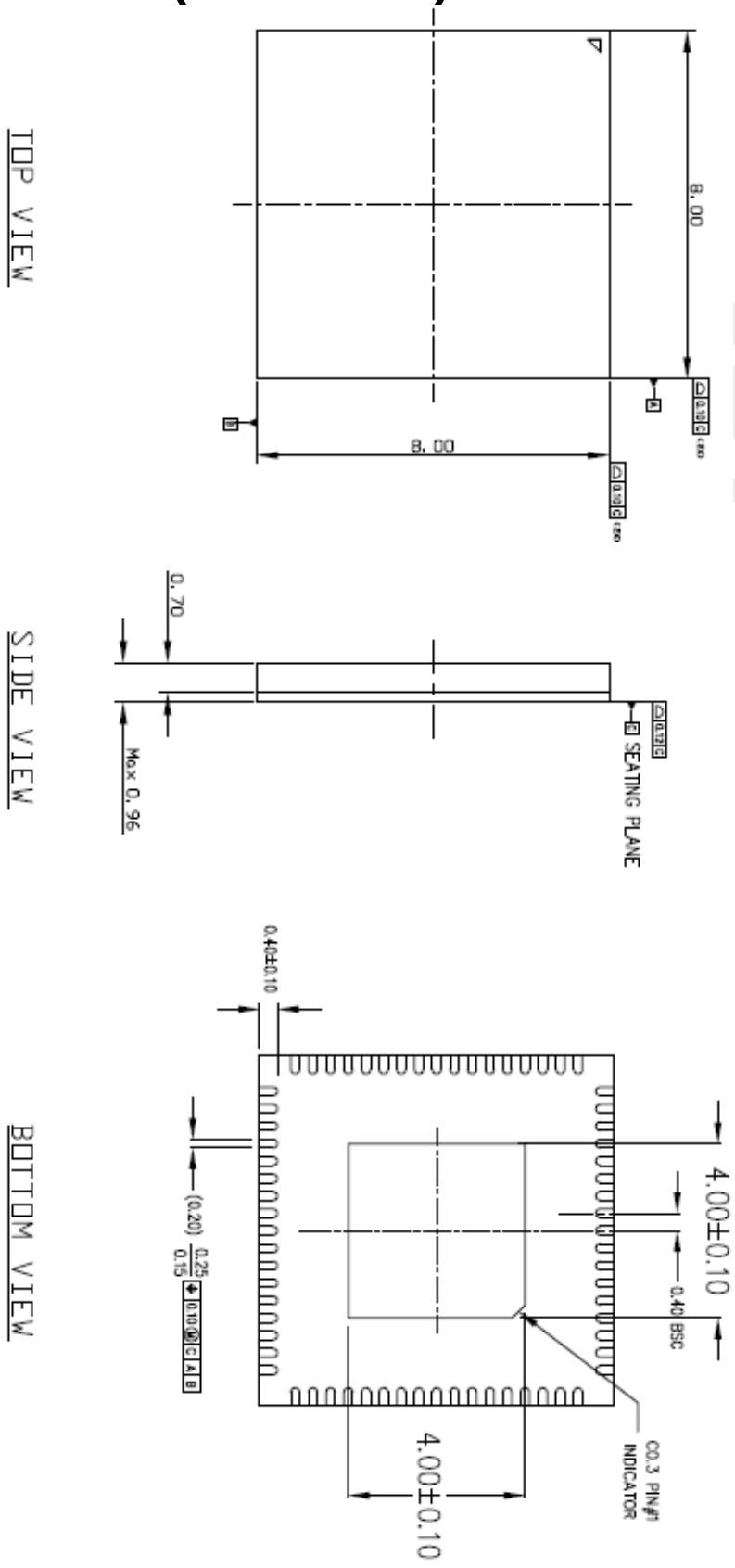
Register Address

Address	Module	R/W
0x0000 ~ 0x01FF	ISP, Special Function, ETC.	Read/Write
0x0200 ~ 0x02FF	ODM, Defect, ETC Read Register	Read Only
0x0300 ~ 0x03FF	Defect Position Register	Read/Write
0x0400 ~ 0x05FF	AWB Color Map Register	Write Only
0x0600 ~ 0x07FF	FONT ID Memory	Write Only
0x0800 ~ 0x09FF	FONT Attribute Memory	Write Only
0x0A00 ~ 0x1BFF	FONT Character Memory	Write Only
0x1C00 ~ 0x1CFF	Reserved	-
0x1D00 ~ 0x1DFF	SHADING Register	Write Only

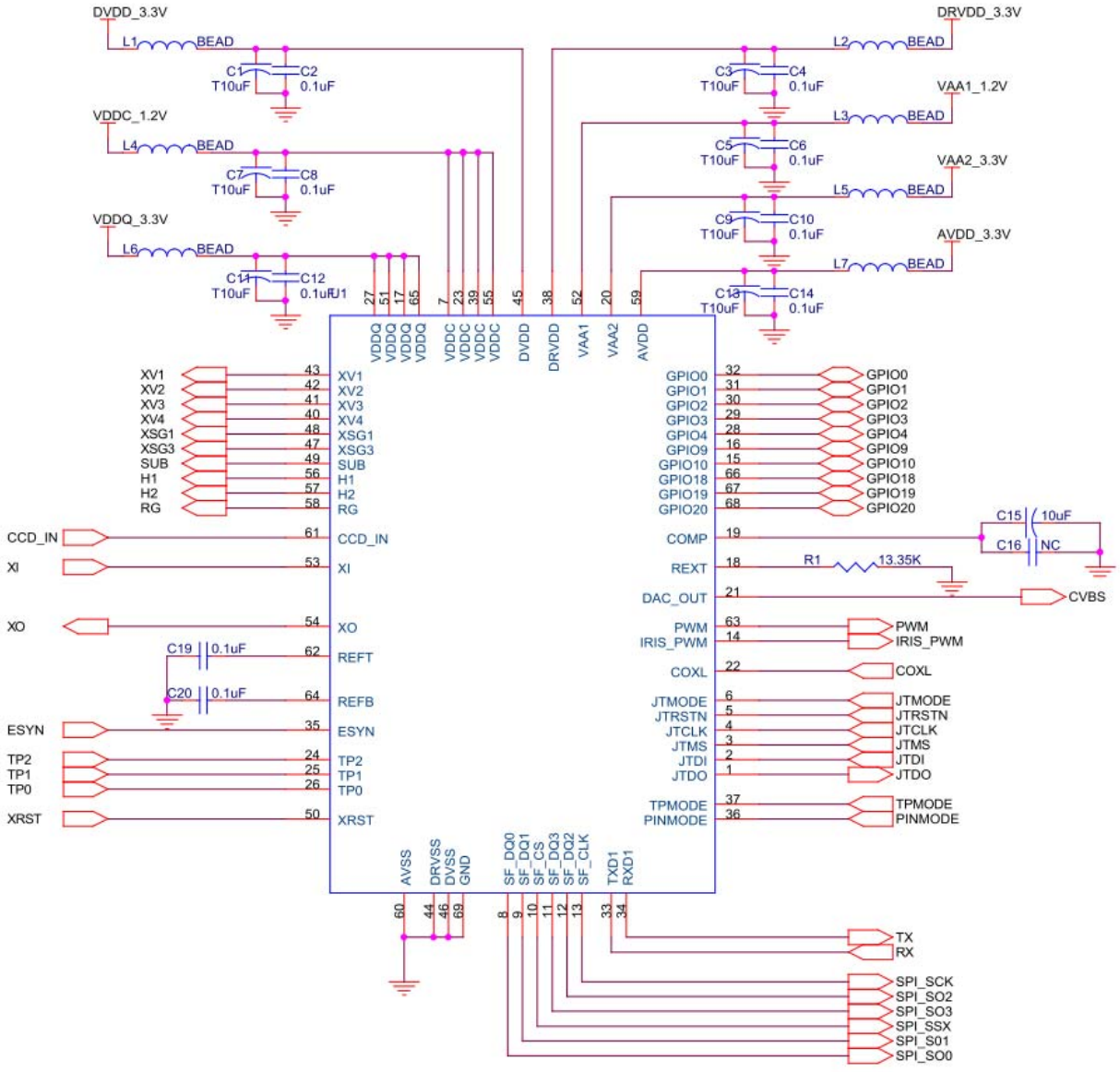
Table 3

- The above table is to control the A88 REGISTER ADDRESS MAP. In EISC, in order to control the DCP area, as it should be used, values of (ADDRESS * 4) can be controlled.
- Therefore, DCP ADDRESS that has to be controlled is obtained by 2-bit LEFT SHIFT of DCP ADDRESS.
- EISC CONTROL ADDRESS = (DCP_ADDRESS << 2)

8. Device Structure (PACKAGE)



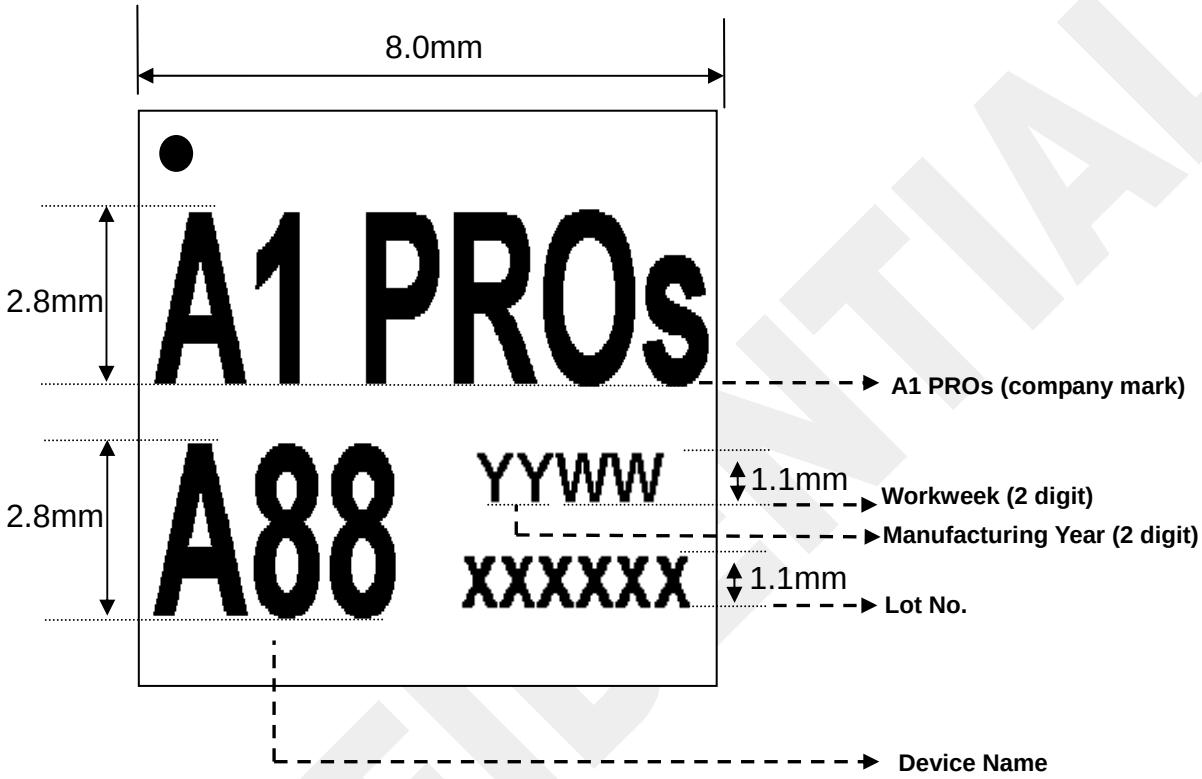
9. Application (SCHEMATIC)



10. Package Marking

Marking contents

(1) Product name : A88
(2) Company name : A1 PROs
(3) Country of origin : KOREA
(4) Data code :



Character Type : Arial
Marking Method : Laser
Line Space : 0.5mm
Marking Location : Center