

3.386

2.471

AA035P3-00

3.810

Value

-55°C to +90°C

-65°C to +150°C

7 V_{DC}

19 dBm

175°C

1.250

Features

- Single Bias Supply Operation (5 V)
- 19 dB Typical Small Signal Gain
- 17 dBm Typical P_{1 dB} Output Power at 35 GHz
- 0.25 µm Ti/Pd/Au Gates
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

Description

Alpha's three-stage reactively-matched Ka band GaAs MMIC driver amplifier has a typical P_{1 dB} of 17 dBm with 18 dB associated gain at 35 GHz. The chip uses Alpha's proven 0.25 µm MESFET technology, which is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate solder or epoxy die attach processes. The amplifier is a self-bias design requiring a single positive drain bias to one of any three bonding sites. All chips are screened for S-parameters prior to shipment for guaranteed performance. A broad range of applications exist in both the high reliability and commercial areas where high gain and power are required.

Electrical Specifications at 25°C (V_{DS} = 5 V)

Condition	Symbol	Min.	Typ. ³	Max.	Unit
					0
	I _{DS}		275	350	mA
= 31–35 GHz	G	15	19		dB
= 35 GHz	NF		10.5		dB
= 31–35 GHz	RL		-14	-10	dB
= 31–35 GHz	RL _O		-16	-10	dB
= 35 GHz	P _{1 dB}	15	17		dBm
= 35 GHz	P _{SAT}	16	19		dBm
	Θ _{JC}		66		°C/W
	= 31–35 GHz = 35 GHz = 31–35 GHz = 31–35 GHz = 35 GHz = 35 GHz	= 31–35 GHz G = 35 GHz NF = 31–35 GHz RLI = 31–35 GHz RLO = 35 GHz P1 dB = 35 GHz PSAT	= 31–35 GHz G 15 = 35 GHz NF 15 = 31–35 GHz RL _I 15 = 31–35 GHz RL _O 15 = 35 GHz P _{1 dB} 15 = 35 GHz P _{SAT} 16	BO BO F	Bit

Chip Outline

1.905

0.000

0.000

Chip thickness = 0.1 mm.

Dimensions indicated in mm.

Absolute Maximum Ratings

Characteristic

Operating Temperature (T_C)

Storage Temperature (T_{ST})

Junction Temperature (T_J)

Bias Voltage (V_D)

Power In (PIN)

.554

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All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.

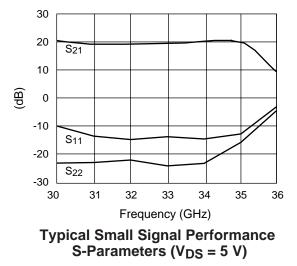
1. Not measured on a 100% basis.

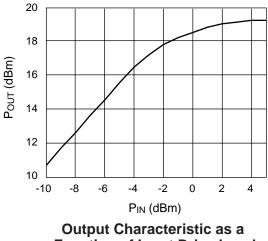
2. Calculated value based on measurement of discrete FET.

3. Typical represents the median parameter value across the specified

frequency range for the median chip.

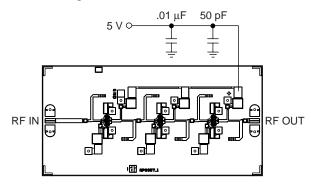
Typical Performance Data





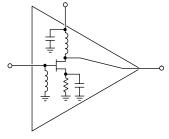
Function of Input Drive Level $(F = 35 \text{ GHz}, V_{DS} = 5 \text{ V})$

Bias Arrangement



For biasing on, adjust V_{DS} from zero to the desired value (4 V–6 V recommended). For biasing off, reverse the biasing on procedure.

Circuit Schematic



Detail A

