

37–40 GHz GaAs MMIC Driver Amplifier



AA038P2-00

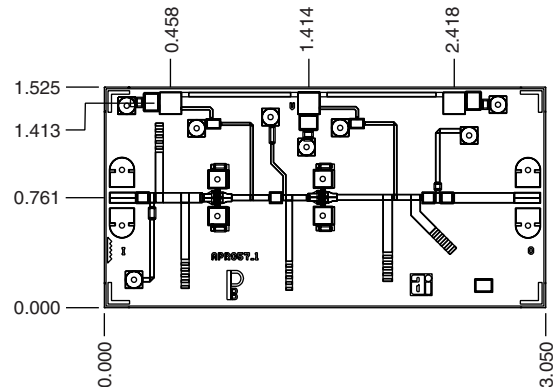
Features

- Single Bias Supply Operation (5 V)
- 13 dB Typical Small Signal Gain
- 14 dBm Typical $P_{1\text{ dB}}$ Output Power at 38 GHz
- 0.25 μm Ti/Pd/Au Gates
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

Description

Alpha's two-stage reactively-matched 37–40 GHz GaAs MMIC driver amplifier has typical small signal gain of 13 dB with a typical $P_{1\text{ dB}}$ of 14 dBm at 38 GHz. The chip uses Alpha's proven 0.25 μm MESFET technology, and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate a conductive epoxy die attach process. All chips are screened for gain, output power and S-parameters prior to shipment for guaranteed performance.

Chip Outline



Dimensions indicated in mm.
All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.
Chip thickness = 0.1 mm.

Absolute Maximum Ratings

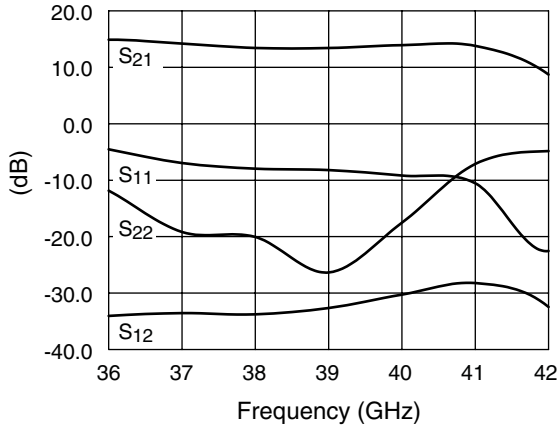
Characteristic	Value
Operating Temperature (T_C)	-55°C to +90°C
Storage Temperature (T_{ST})	-65°C to +150°C
Bias Voltage (V_D)	7 V_{DC}
Power In (P_{IN})	16 dBm
Junction Temperature (T_J)	175°C

Electrical Specifications at 25°C ($V_{DS} = 5\text{ V}$)

Parameter	Condition	Symbol	Min.	Typ. ²	Max.	Unit
Drain Current		I_{DS}		75	100	mA
Small Signal Gain	F = 37–40 GHz	G	11	13		dB
Input Return Loss	F = 37–40 GHz	RL_I		-9	-6	dB
Output Return Loss	F = 37–40 GHz	RL_O		-12	-10	dB
Output Power at 1 dB Gain Compression	F = 38 GHz	$P_{1\text{ dB}}$	13	14		dBm
Saturated Output Power	F = 38 GHz	P_{SAT}	15	16		dBm
Thermal Resistance ¹		θ_{JC}		199		°C/W

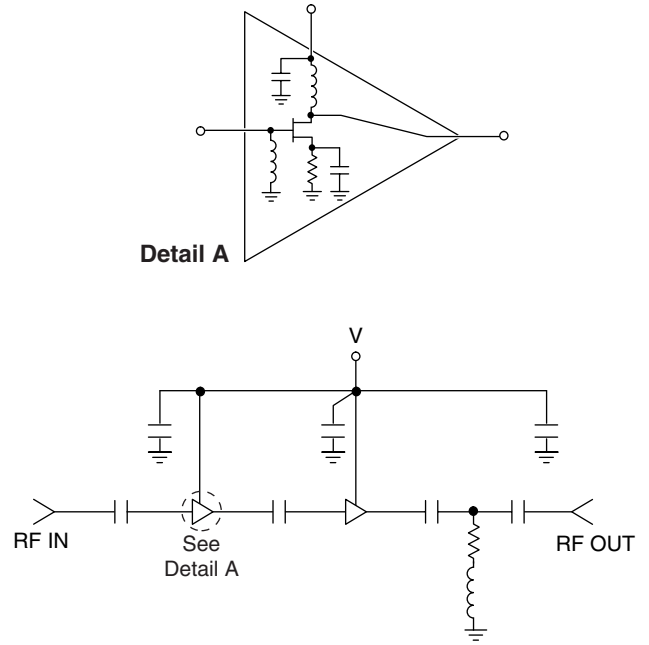
1. Calculated value based on measurement of discrete FET.
2. Typical represents the median parameter value across the specified frequency range for the median chip.

Typical Performance Data

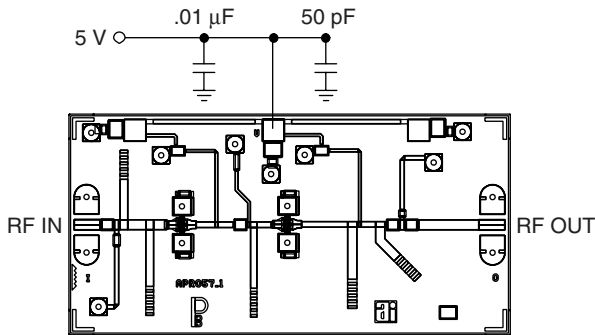


Typical Small Signal Performance S-Parameters (V_{DS} = 5 V)

Circuit Schematic



Bias Arrangement



For biasing on, adjust V_{DS} from zero to the desired value (5 V recommended). For biasing off, reverse the biasing on procedure.