ACE25AA400G

Serial NOR Flash Memory 4M bits 3.0V Quad I/O Serial Flash Memory with 4KB Uniform Sector

Description

The ACE25AA400G is 4M-bit Serial flash supports the standard Serial Peripheral Interface (SPI). and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 216Mbits/s and the Quad I/O & Quad output data is transferred with speed of 432Mbits/s.

Features

- 4M-bit Serial Flash
  512K-byte
  256 bytes per programmable page
- Standard, Dual, Quad SPI
  Standard SPI: SCLK, CS#, SI, SO, SO, WP#, HOLD#
  Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- Flexible Architecture
  Sector of 4K-byte
  Block of 32/64k-byte
- Package Options
  All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- Temperature Range & Moisture Sensitivity Level
  Industrial Level Temperature. (-40°C to +85°C), MSL3
- Low Power Consumption
  20mA maximum active current
  0.05uA maximum power down current
- Single Power Supply Voltage: Full voltage range:2.7~3.6V
- Minimum 100,000 Program/Erase Cycle
- High Speed Clock Frequency
  108MHz for fast read with 30PF load
  Dual I/O Data transfer up to 216Mbits/s
  Quad I/O Data transfer up to 432Mbits/s
- Program/Erase Speed
  Page Program time: 0.4ms typical
  Sector Erase time: 60ms typical
 Block Erase time: 0.15/0.25s typical
  Chip Erase time: 1.25s typical

- Software/Hardware Write Protection

  Write protect all/portion of memory via software

  Enable/Disable protection with WP# Pin

  Top or Bottom, Sector or Block selection

- Advanced security Features

  4*256-Byte Security Registers With OTP Lock

- Support SFDP & Unique ID

Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input /Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Packaging Type

SOP-8/SOP-8L   TSSOP-8   USON3*2-8
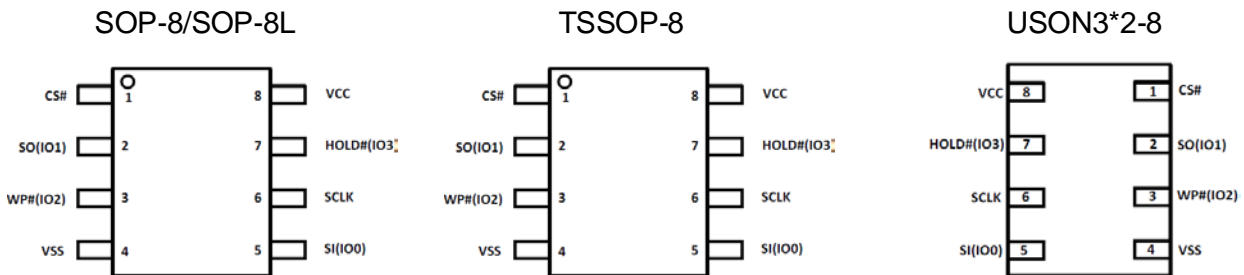
Pin Configurations

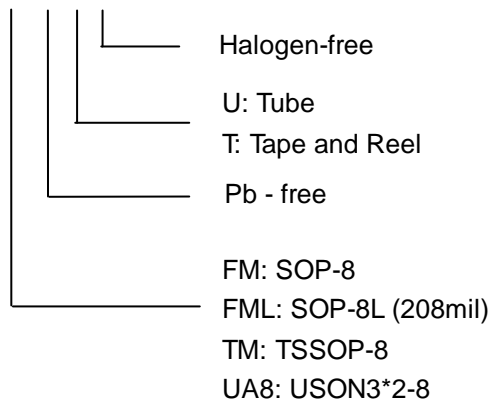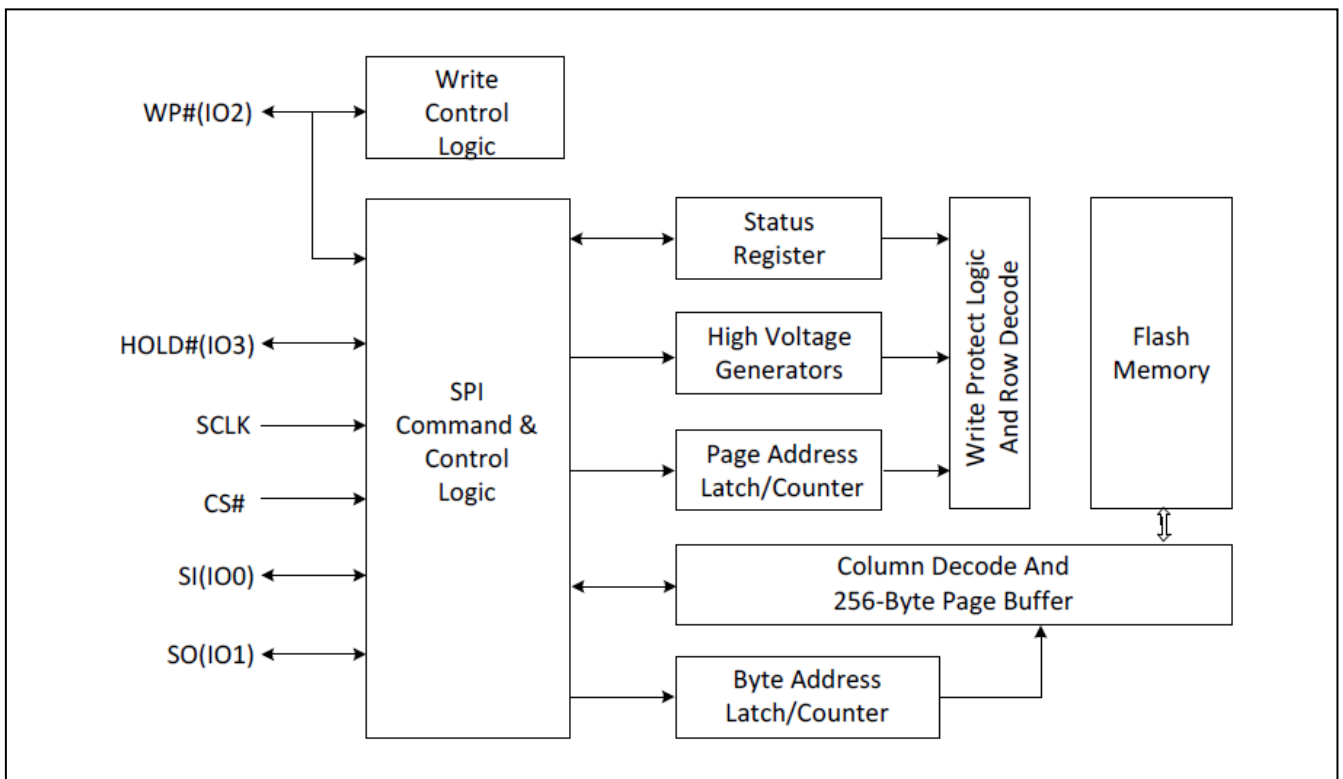| Pin Name	I/O	Functions
CS#	I	Chip Select Input
SO(IO1)	I/O	Data Output(Data Input Output 1)
WP#(IO2)	I/O	Write Protect Input (Data Input Output 2)
VSS		Ground
SI(IO0)	I/O	Data Input(Data Input Output 0)
SCLK	I	Serial Clock Input
HOLD#(IO3)	I/O	Hold Input (Data Input Output 3)
VCC		Power Supply

Ordering information

ACE25AA400G XX + X H

- Halogen-free

- U: Tube
- T: Tape and Reel

- Pb - free

- FM: SOP-8
- FML: SOP-8L (208mil)
- TM: TSSOP-8
- UA8: USON3*2-8

Block Diagram

Uniform Block Sector Architecture

ACE25AA400G 64K Bytes Block Sector Architecture

Block	Sector	Address Range	
7	127	07F000H	07FFFFH
	……	……	……
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	……	……	……
	96	060000H	060FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

Device Operation

The ACE25AA400G features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Note: "WP#" & "HOLD#" pin require external pull-up

Dual SPI

The ACE25AA400G supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Note: "WP#" & "HOLD#" pin require external pull-up

Quad SPI

The ACE25AA400G supports Quad SPI operation when using the "Quad Output Fast Read", "Quad I/O Fast Read", "Quad I/O Word Fast Read" (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set .

Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress .

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.
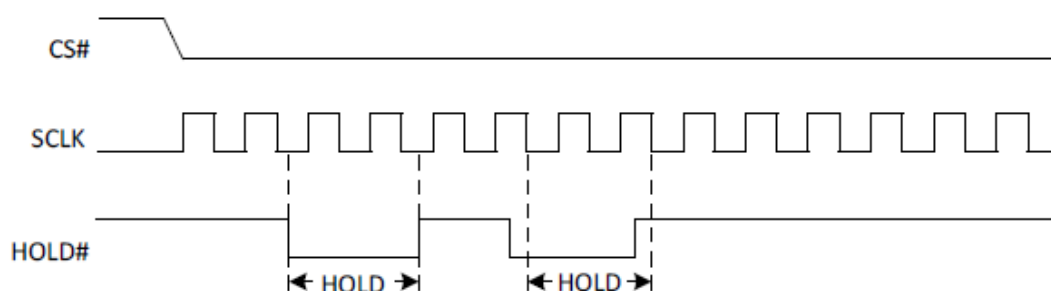
Data Protection

The ACE25AA400G provides the following data protection methods:

Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:

- Power-Up
- Write Disable (WRDI)
- Write Status Register (WRSR)
- Page Program (PP)
- Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)

Software Protection Mode:

- The Block Protect (BP3, BP2, BP1,BP0) bits define the section of the memory array that can be read but not change

Hardware Protection Mode:

- WP# going low to protected the BP0~BP3 bits and SRP bit

Deep Power-Down Mode:

- In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command

Table 1.ACE25AA400G Protected Area Sizes (CMP=0)

Status Register Contents				Protect Level	Protected Block
BP3	BP2	BP1	BP0		
0	0	0	0	0(none)	None
0	0	0	1	1(1 block)	Block 7
0	0	1	0	2(2 blocks)	Block 6-7
0	0	1	1	3(4 blocks)	Block 4-7
0	1	0	0	4(8 blocks)	protected all

Table 1.1ACE25AA400G Protected Area Sizes (CMP=1)

Status Register Contents				Protect Level	Protected Block
BP3	BP2	BP1	BP0		
0	0	0	0	0(none)	None
0	0	0	1	1(1 block)	Block 0
0	0	1	0	2(2 blocks)	Block 0-1
0	0	1	1	3(4 blocks)	Block 0-3
0	1	0	0	4(8 blocks)	Block 0-7

Status Register

S15	S14	S13	S12	S11	S10	S9	S8
Reserved	CMP	Reserved	Reserved	Reserved	LB	QE	Reserved

S7	S6	S5	S4	S3	S2	S1	S0
SRP	Reserved	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, the device is busy in program/erase/write status register progress, When WIP bit sets 0, means the device is not in program/ erase/ write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP3,BP2, BP1,BP0 bits.

The Block Protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP3, BP2, BP1, BP0) bits are all 0.

SRP bit.

The Status Register Protect (SRP) bit is a non-volatile Read/Write bit in the status register. The SRP bit controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP	WP#	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written until the next power-up.
1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written after a Write Enable command, WEL=1.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE bit is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

LB bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S10) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP3-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

Commands Description

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK. See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8)				(continuous)
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	Dummy(5)	(D7-D0)(3)			(continuous)
Quad I/O Word Fast Read	E7H	A23-A0 M7-M0(4)	Dummy(6)	(D7-D0)(3)			(continuous)
Continuous Read Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		
Quad I/O PP	38H	A23-A0 D7-D0	(D39-D8)	(Next byte)	(Next byte)		
Sector Erase	20H	A23-A16	A15-A8	A7-A0			

Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7- MID0)	(DID7-DID0)	(continuous)
Manufacturer/Device ID by Dual I/O	92H	A23-A8	A7-A0, M[7:0]	(M7-M0) (ID7-ID0)			(continuous)
Manufacturer/Device ID by Quad I/O	94H	A23-A0, M[7:0]	dummy	(M7-M0) (ID7-ID0)			
Read Serial Flash Discoverable Parameters	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Read Unique ID	5AH	00h	01h	94h	dummy	(D7-D0)	(continuous)
Read Identification	9FH	(MID7- MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Erase Security Register(8)	44H	A23-A16	A15-A8	A7-A0			
Program Security Register(8)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Read Security Register(8)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	
Enable Reset	66H						
Reset	99H						

Notes:

1. Dual Output data

    IO0 = (D6, D4, D2, D0) IO1 = (D7, D5, D3, D1)

2. Dual Input Address

    IO0 = A22, A20, A18, A16, A14, A12, A10, A8,A6, A4, A2, A0, M6, M4, M2, M0

    IO1 = A23, A21, A19, A17, A15, A13, A11, A9,A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

    IO0 = (D4, D0, …..)

    IO1 = (D5, D1, …..)

    IO2 = (D6, D2, …..)

    IO3 = (D7, D3, …..)

4. Quad Input Address

    IO0 = A20, A16, A12, A8, A4, A0, M4, M0

    IO1 = A21, A17, A13, A9, A5, A1, M5, M1

    IO2 = A22, A18, A14, A10, A6, A2, M6, M2

    IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Quad I/O Fast Read Data

    IO0 = (x, x, x, x, D4, D0,…)

    IO1 = (x, x, x, x, D5, D1,…)

    IO2 = (x, x, x, x, D6, D2,…)

    IO3 = (x, x, x, x, D7, D3,…)

6. Quad I/O Word Fast Read Data

    IO0 = (x, x, D4, D0,…)

    IO1 = (x, x, D5, D1,…)

    IO2 = (x, x, D6, D2,…)

    IO3 = (x, x, D7, D3,…)

7. Quad I/O Word Fast Read Data: the lowest address bit must be 0

8. Security Registers Address :

    Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;

    Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address;

    Security Register3: A23-A16=00H, A15-A8=03H, A7-A0= Byte Address.

ID Definitions

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0E	40	14
90H	0E		13
ABH			13

Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low, sending the Write Enable command, CS# goes high.
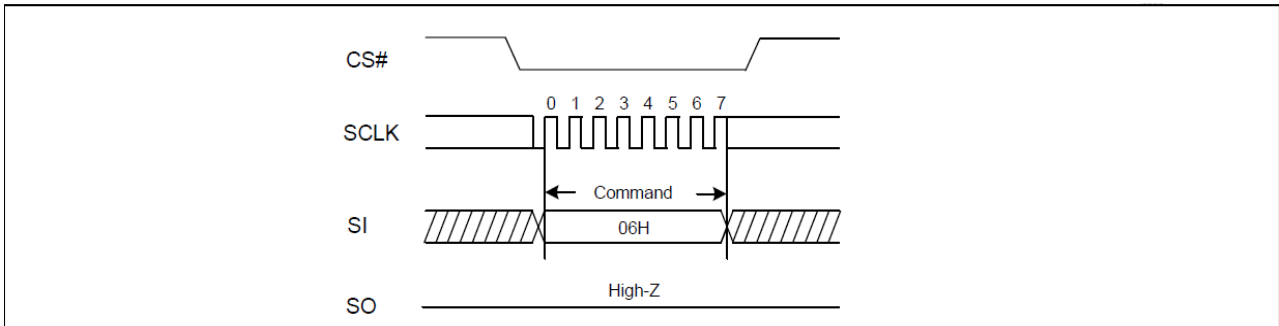

Figure1. Write Enable Sequence Diagram

Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.
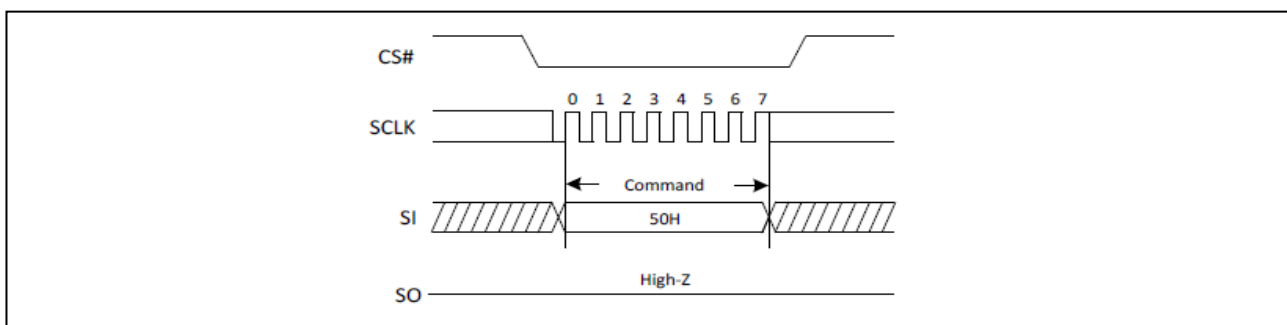
Figure2. Write Enable for Volatile Status Register Sequence Diagram

Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low Send Write Disable command CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.
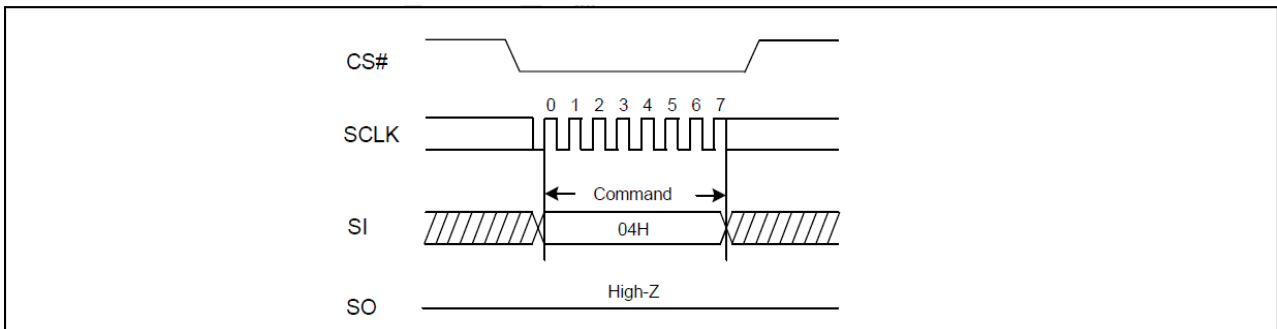

Figure3. Write Disable Sequence Diagram

Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H", the SO will output Status Register bits S7~S0. The command code "35H", the SO will output Status Register bits S15~S8.
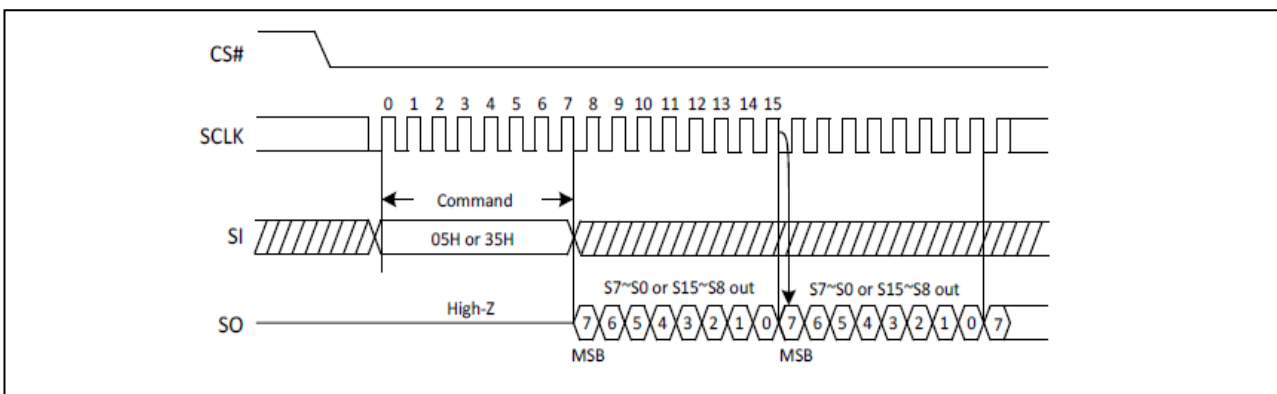
Figure4. Read Status Register Sequence Diagram

Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S1 and S0 of the Status Register.

CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE bit will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register can still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP3,BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.
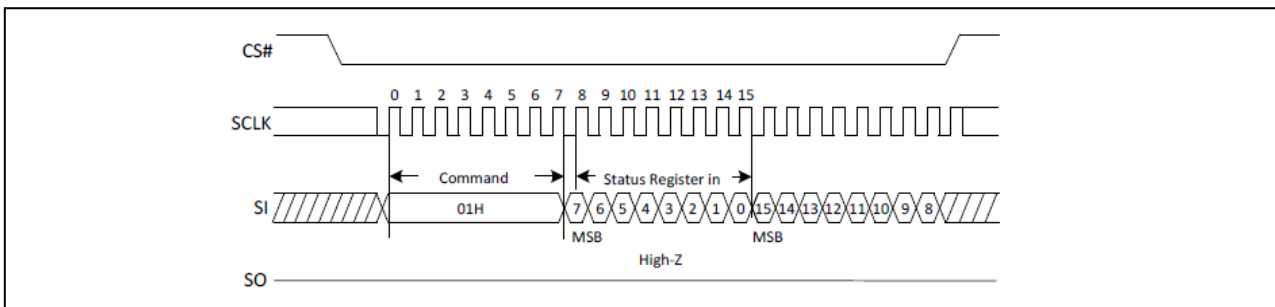

Figure5. Write Status Register Sequence Diagram

Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Therefore, the whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
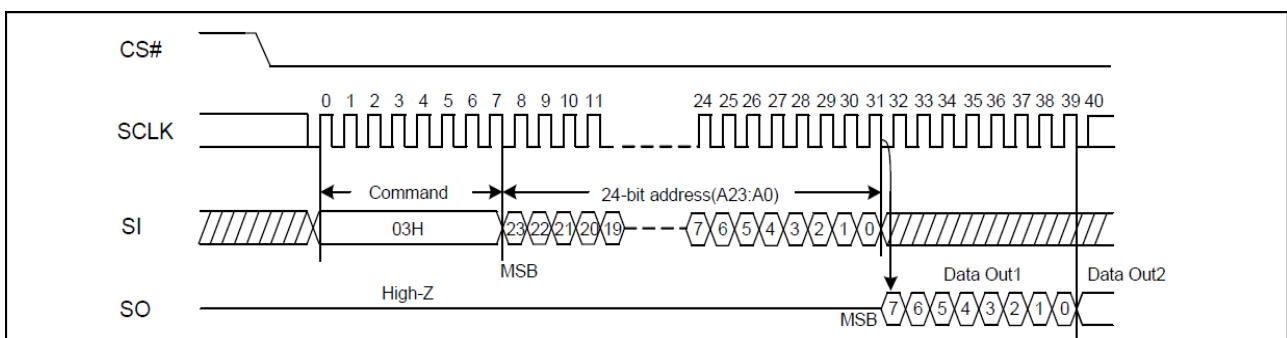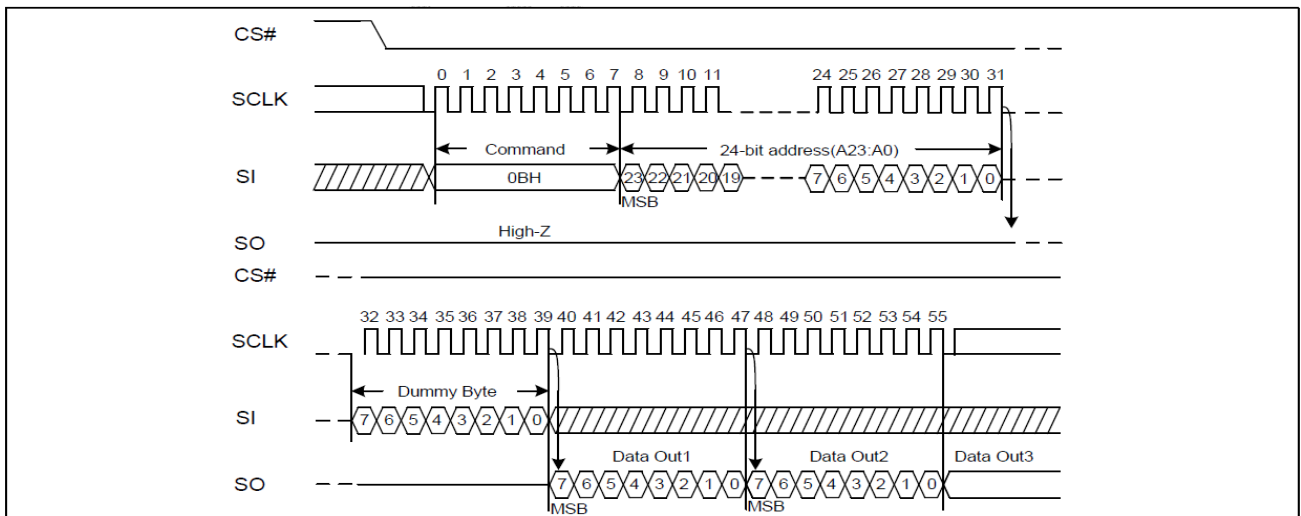

Figure6. Read Data Bytes Sequence Diagram

Read Data Bytes At Higher Speed (Fast Read)(0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.
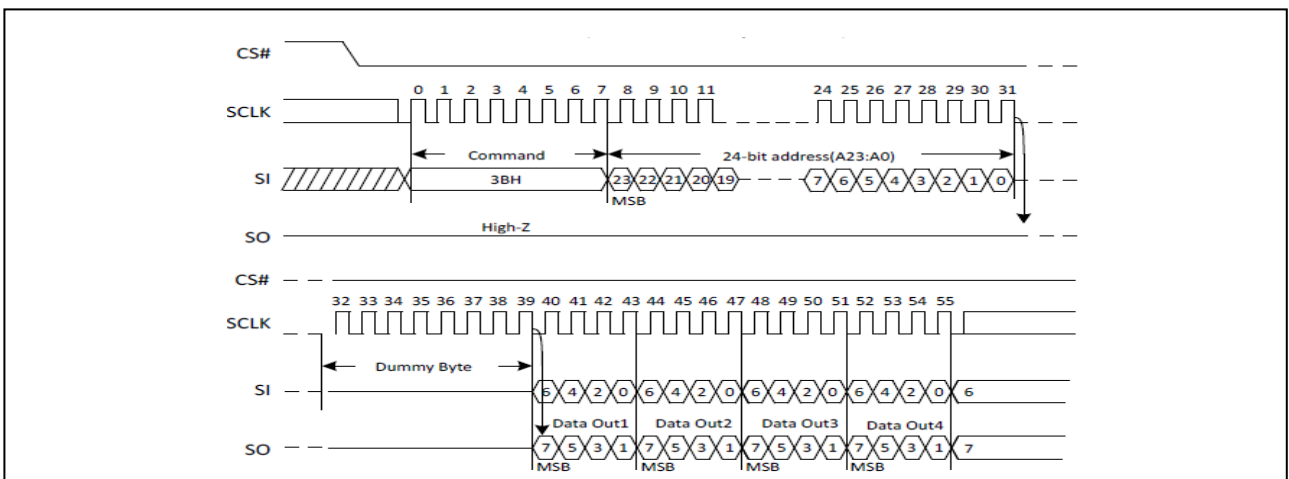

Figure7. Read Data Bytes at Higher Speed Sequence Diagram

Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.
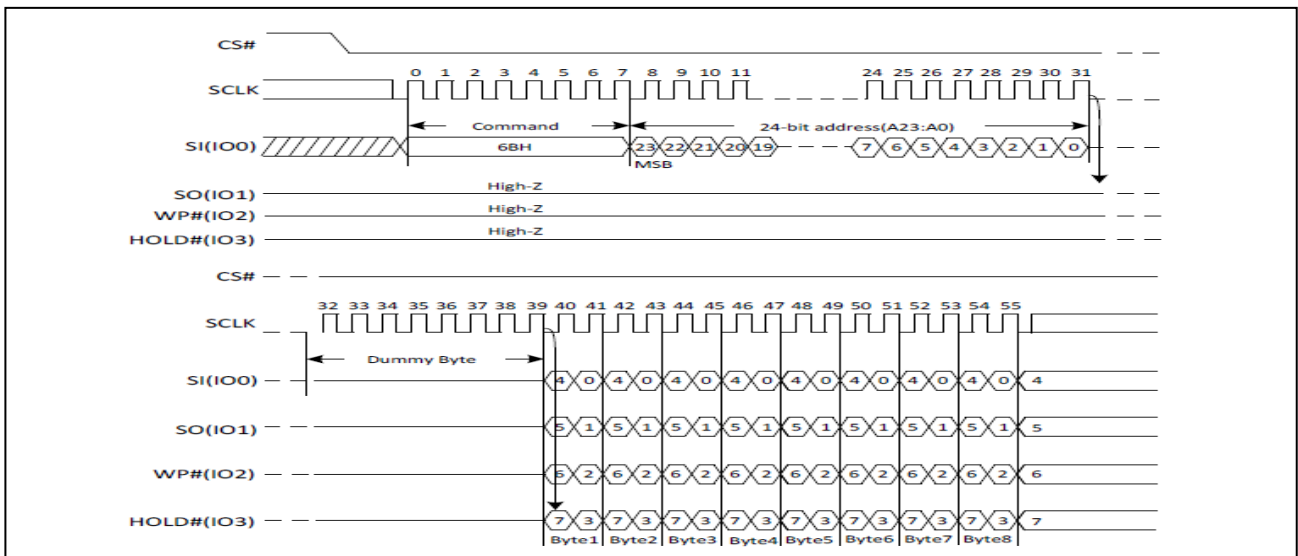

Figure8. Dual Output Fast Read Sequence Diagram

VER 1.3   15

Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure9. Quad Output Fast Read Sequence Diagram

Dual I/O Fast Read(BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7- 0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure 11. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.
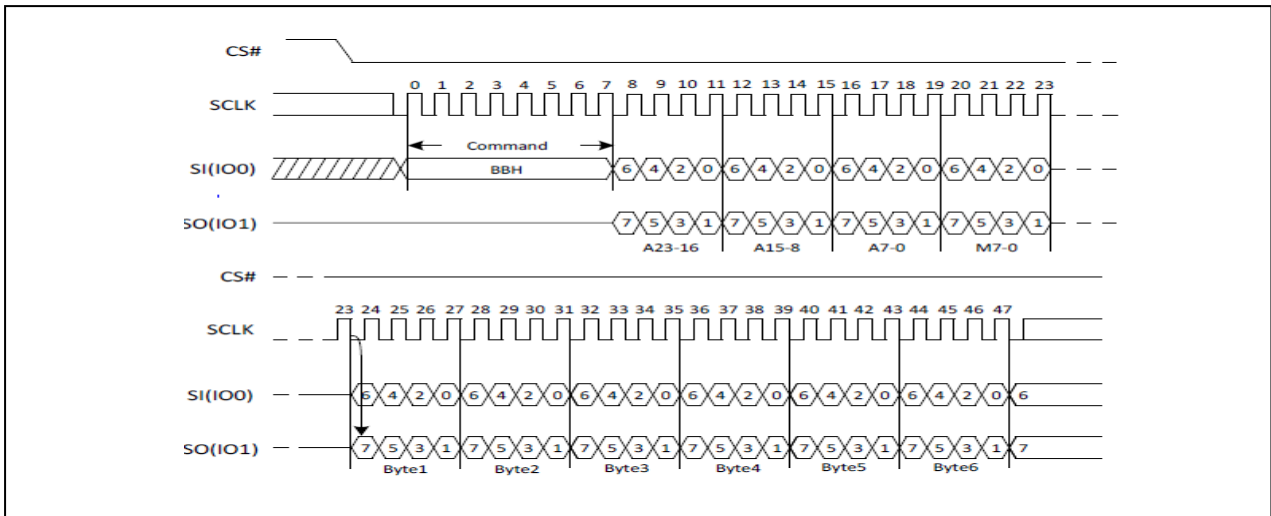
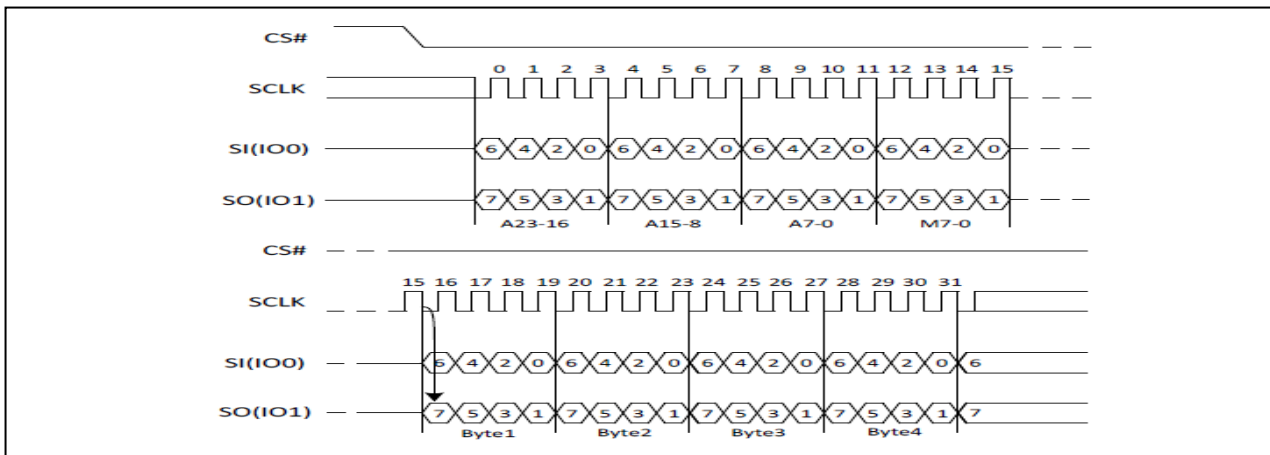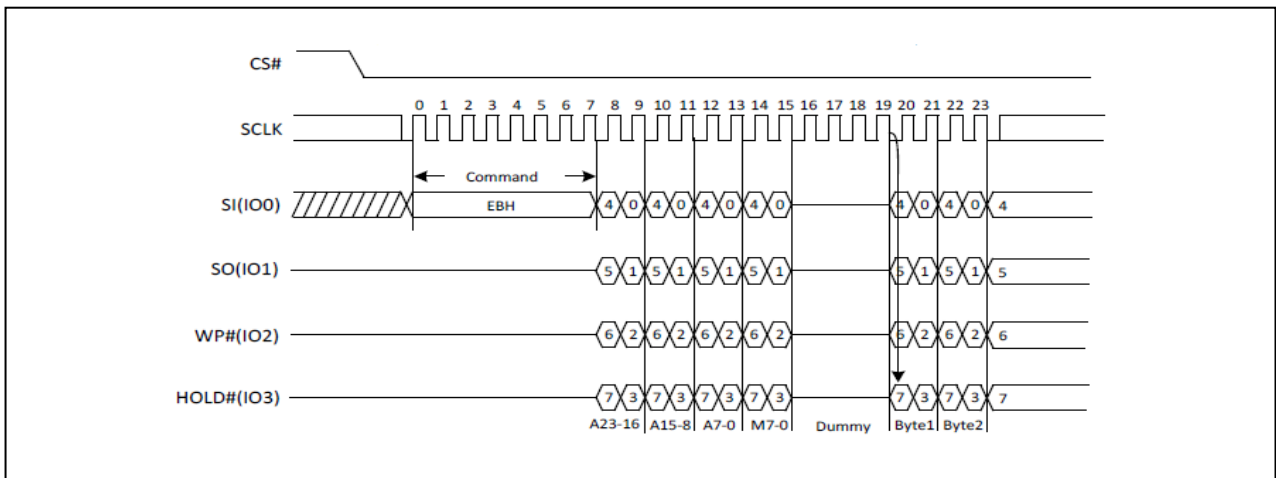Figure10. Dual I/O Fast Read Sequence Diagram (M5-4≠ (1, 0))

Figure11. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))

Quad I/O Fast Read(EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bits per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in Figure 12. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not re- quire the EBH command code. The command sequence is shown in Figure 13. If the "Continuous Read Mode" (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

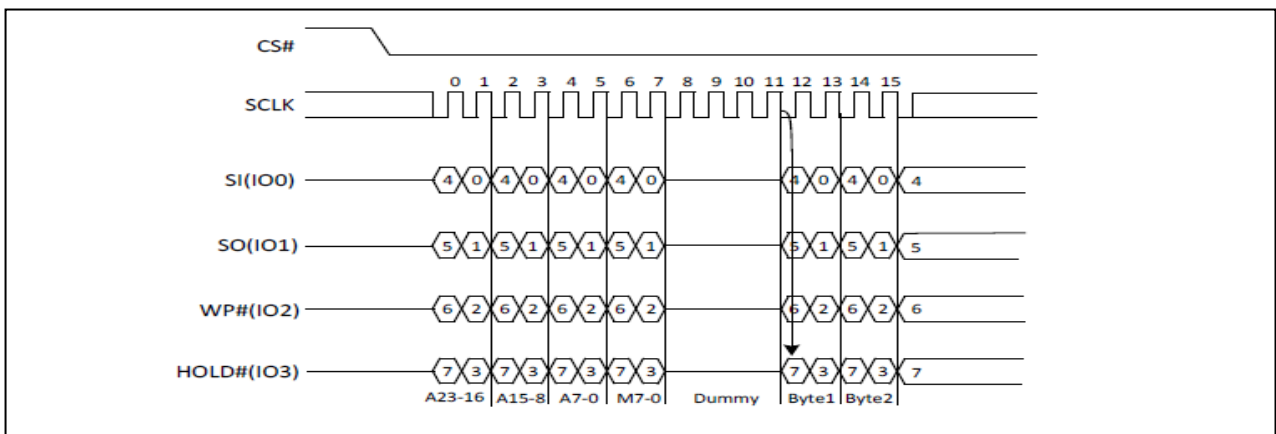Figure12.Quad I/O Fast Read Sequence Diagram (M5-4≠ (1, 0))

Figure13.Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0))

Quad I/O Word Fast Read(E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure 14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure 15. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.
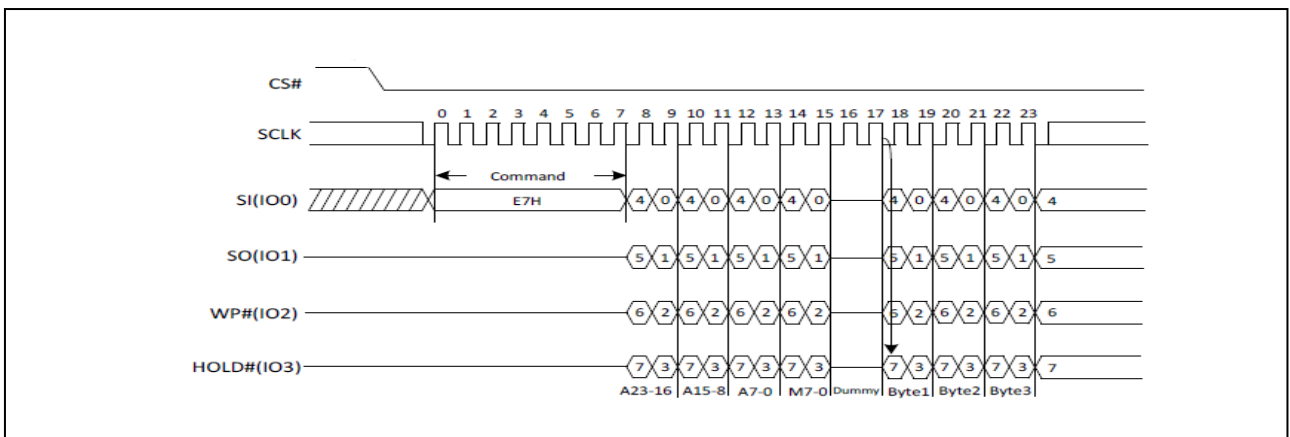

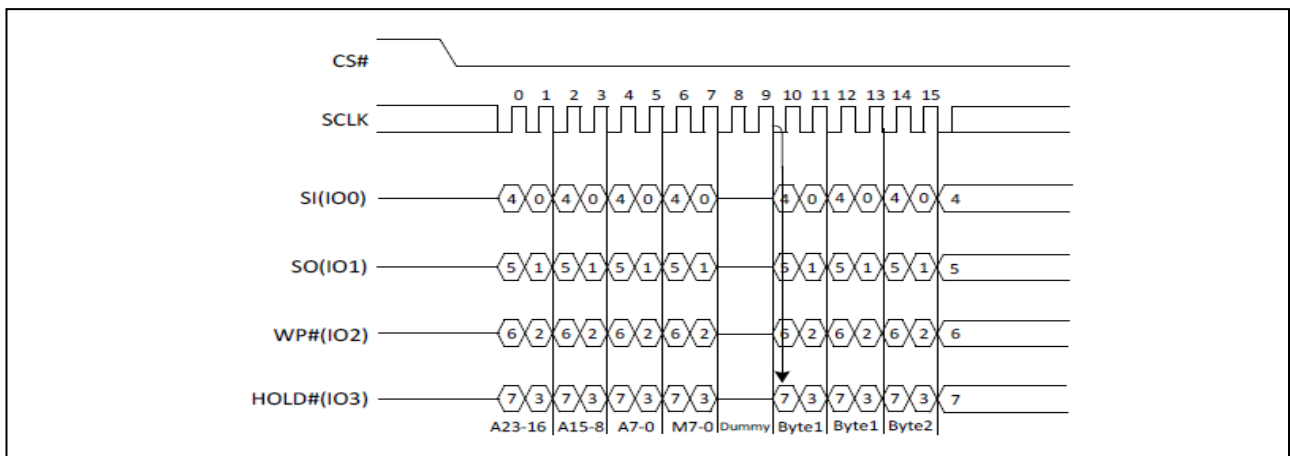Figure14.Quad I/O Word Fast Read Sequence Diagram (M5-4≠ (1, 0))

Figure15.Quad I/O Word Fast Read Sequence Diagram (M5-4= (1, 0))

Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low sending Page Program command 3-byte address on SI at least 1 byte data on SI CS# goes high. The command sequence is shown in Figure16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. As some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP3, BP2, BP1, BP0) is not executed.
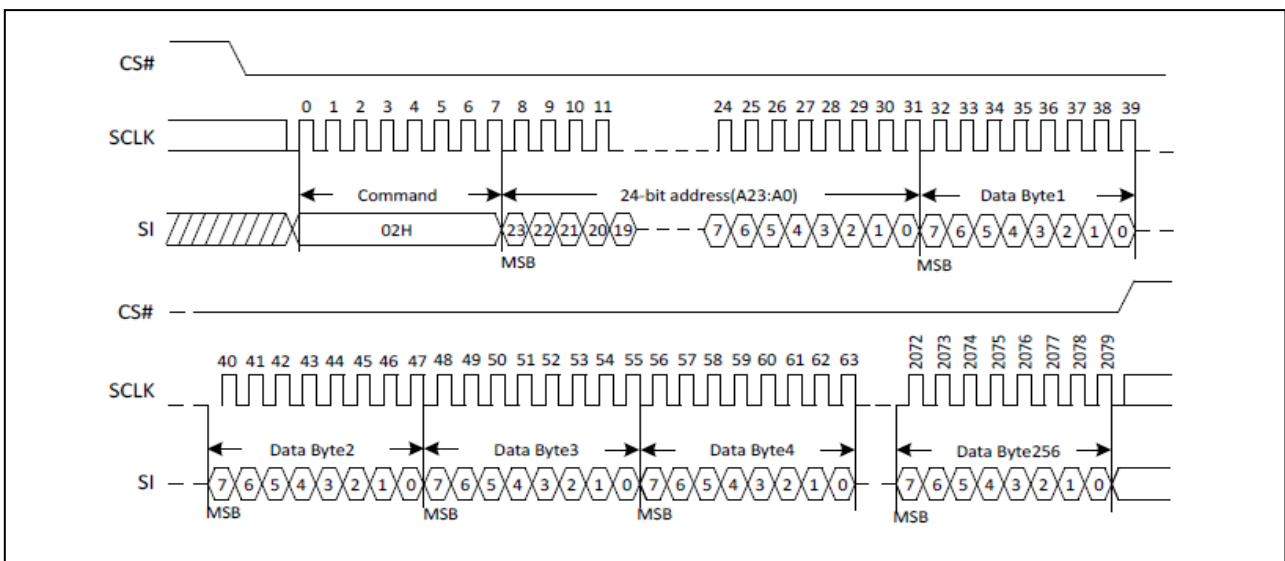

Figure16. Page Program Sequence Diagram

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Quad Page Program (QPP) (32H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure 17. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested ad- dresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP3, BP2, BP1, BP0) will not be executed.
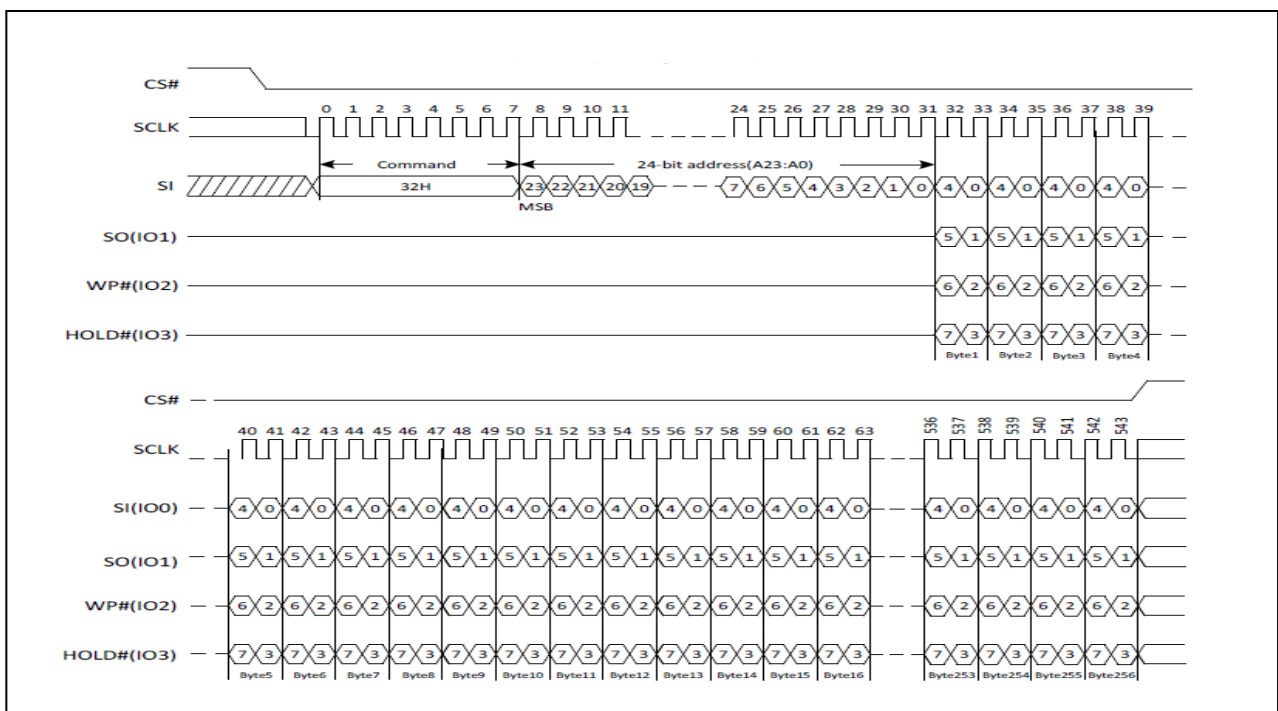

Figure17. Quad Page Program Sequence Diagram

4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of ap- plication. The 4PP operation frequency supports as fast as f4PP. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low → sending 4PP instruction code → 3-byte address on SIO[3:0] → at least 1-byte on data on SIO[3:0] → CS# goes high .
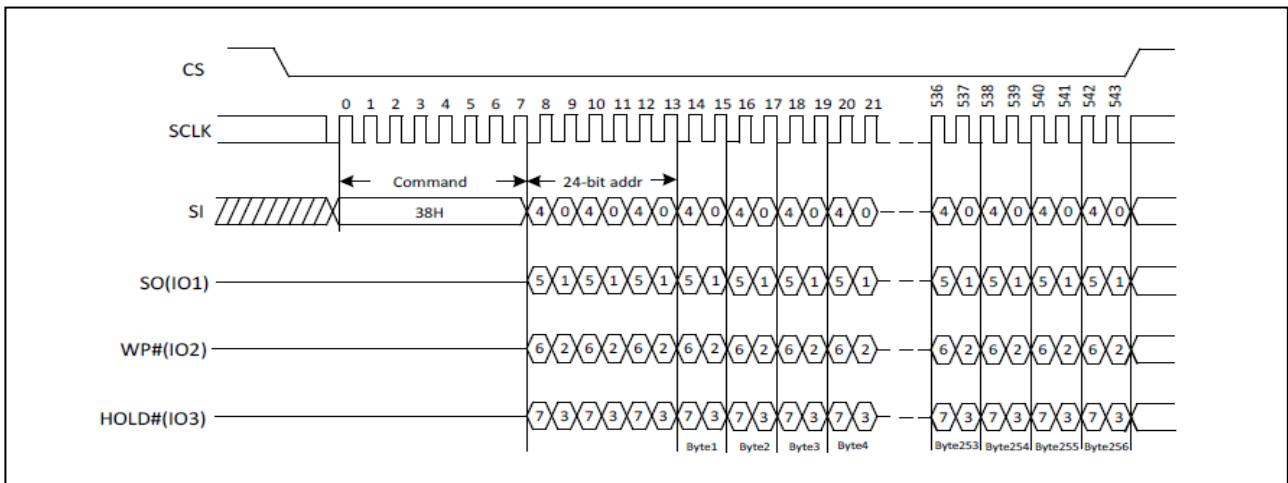

Figure18. Quad I/O Page Program Sequence Diagram

Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low sending Sector Erase command 3-byte address on SI CS# goes high. The command sequence is shown in Figure19. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed.

Write Enable Latch (WEL) bit is reset to 0 at the end of the Sector Erase cycle. Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP3,BP2, BP1, BP0) bit (see Table1 &1.1) will not be executed.
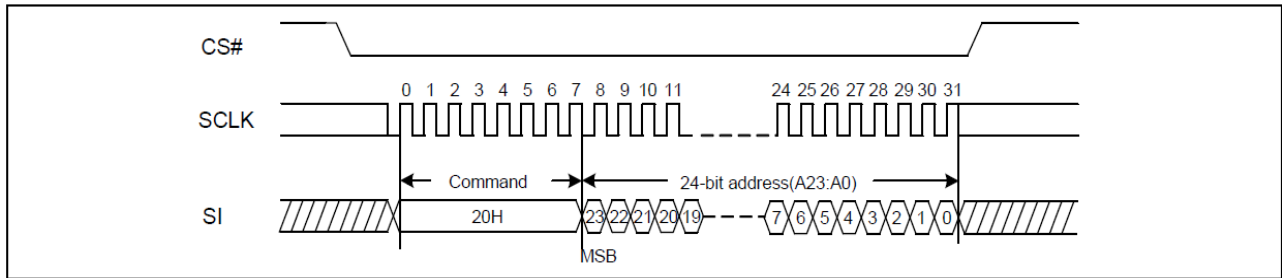

Figure19. Sector Erase Sequence Diagram

32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low sending 32KB Block Erase command 3-byte address on SI, CS# goes high. The command sequence is shown in Figure20. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP3, BP2, BP1, BP0) bits (see Table1 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.
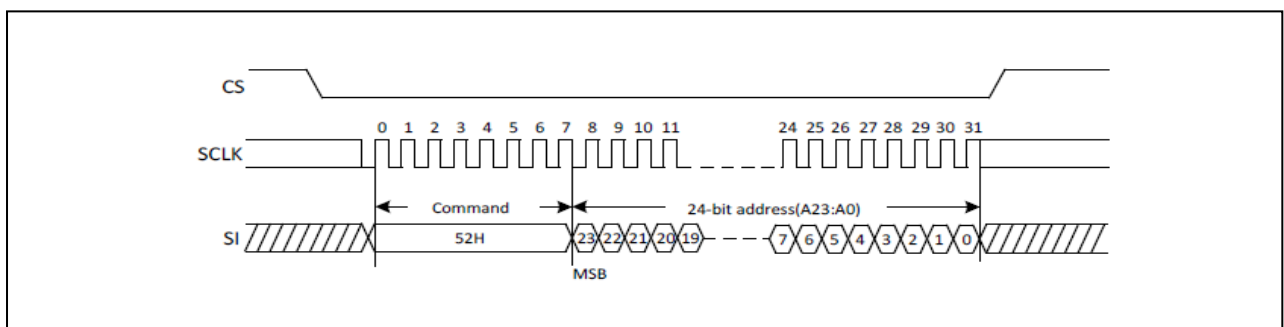

Figure20. 32KB Block Erase Sequence Diagram   VER 1.3   23

64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low sending 64KB Block Erase command 3-byte address on SI, CS# goes high. The command sequence is shown in Figure21. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. Write Enable Latch (WEL) bit is reset t. A 64KB Block Erase (BE) commands applied to a block which is protected by the Block Protect (BP3,BP2, BP1, BP0) bits (see Table1 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.
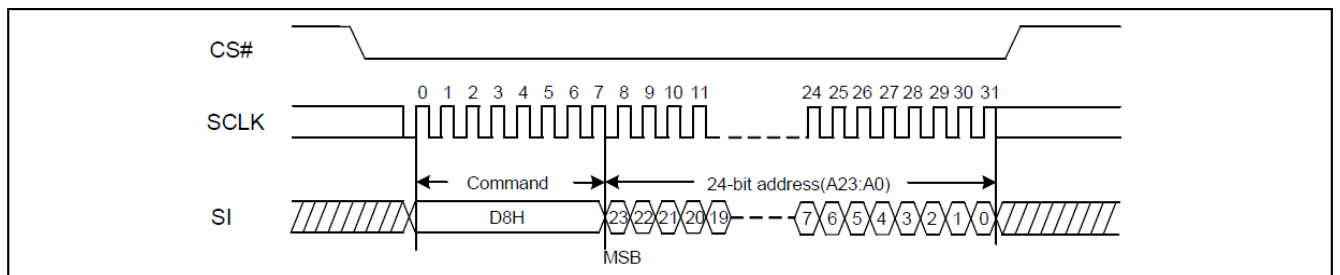

Figure21. 64KB Block Erase Sequence Diagram

Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low send Chip Erase command CS# goes high. The command sequence is shown in Figure22. CS# must be driven high after the eighth bit of the command code has been latch in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed.

At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block protected by (BP3, BP2, BP1, BP0) bits. The Chip Erase(CE) command is ignored if one or more sectors are protected.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.
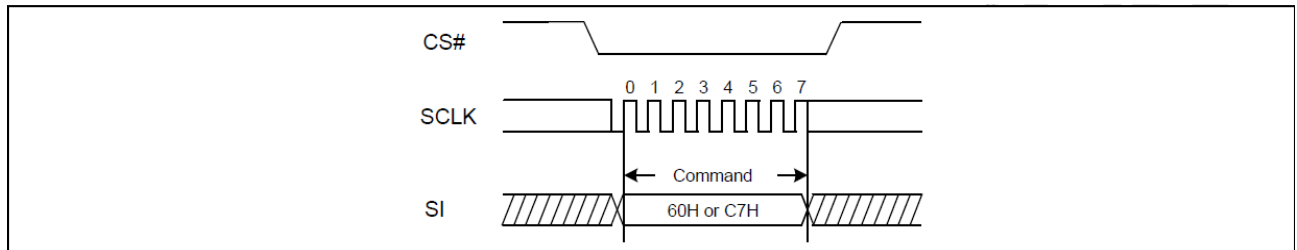

Figure22. Chip Erase Sequence Diagram

Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power- Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low, sending Deep Power-Down command, CS# goes high. The command sequence is shown in Figure 23. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power- Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
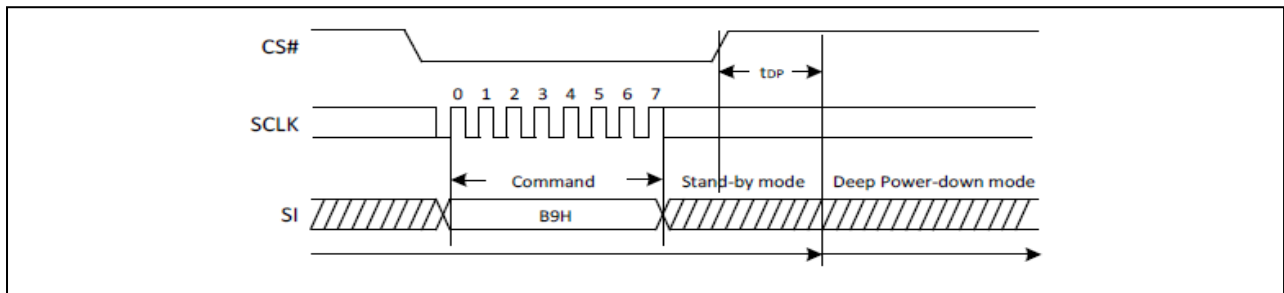
Figure23. Deep Power-Down Sequence Diagram

Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read/Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number. To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure24. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure25. The Device ID value for the ACE25AA400G is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 25, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not affects on the current cycle.
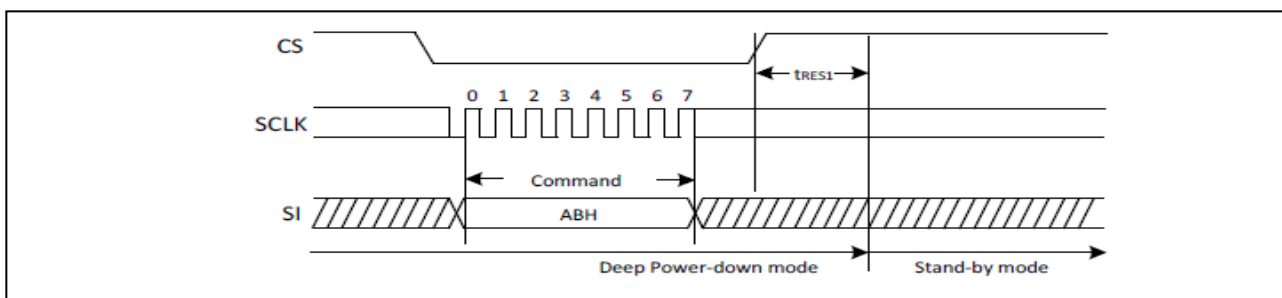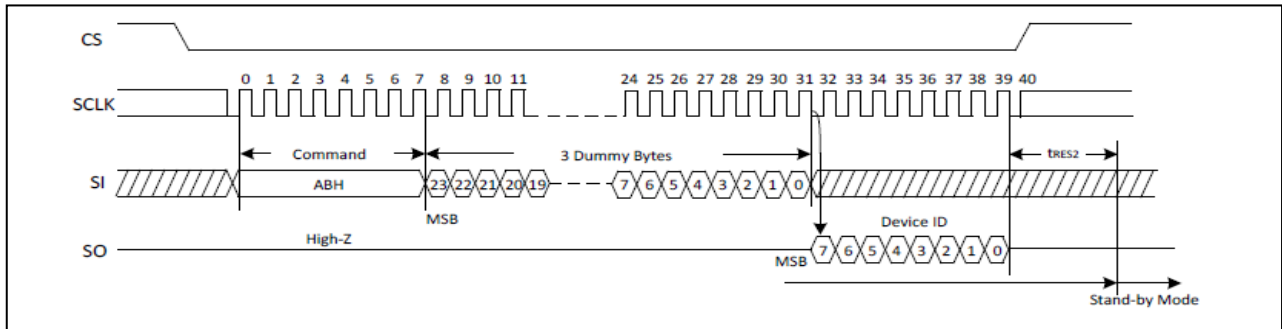

Figure24. Release Power-Down Sequence Diagram

Figure25. Release Power-Down /Read Device ID Sequence Diagram

Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID. The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 26. If the 24-bit address is initially set to 000001H, the Device ID will be read first.
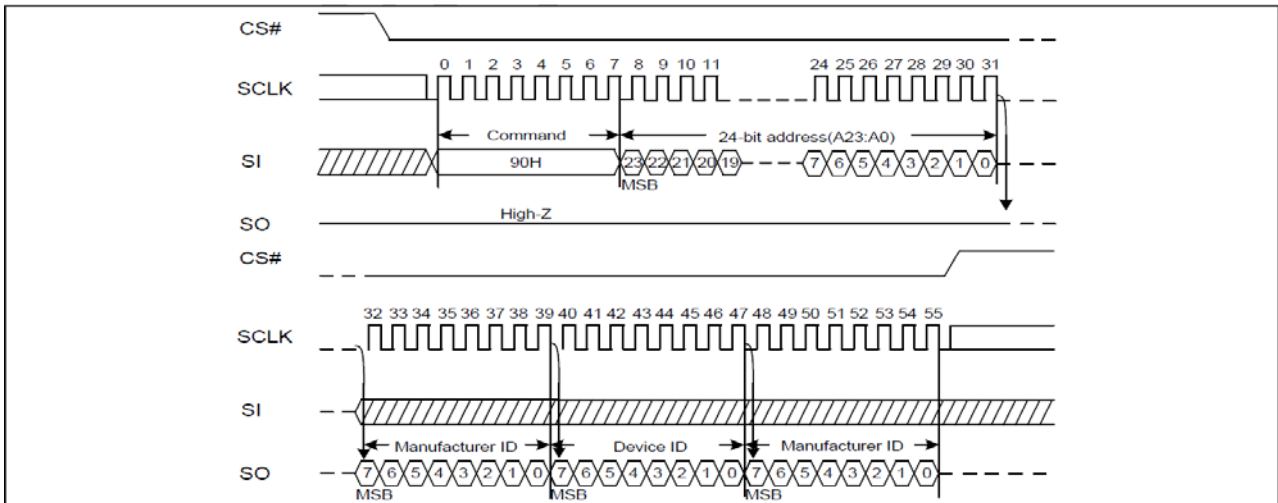
Figure26. Read ID Sequence Diagram

Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, "Continuous Read Mode" bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

Because the ACE25AA400G has no hardware reset pin, so if Continuous Read Mode bits are set to "AXH", the ACE25AA400G will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the "AXH" state and allow standard SPI command to be recognized. The command sequence is shown in Figure 27.
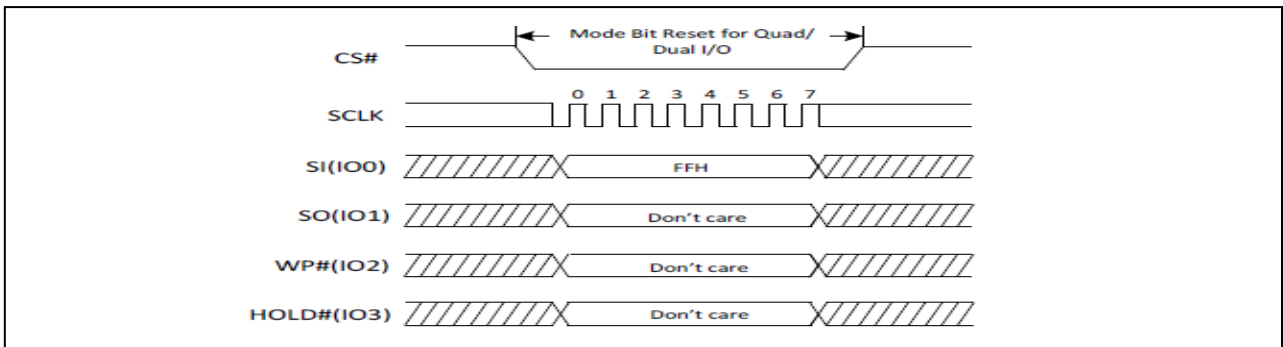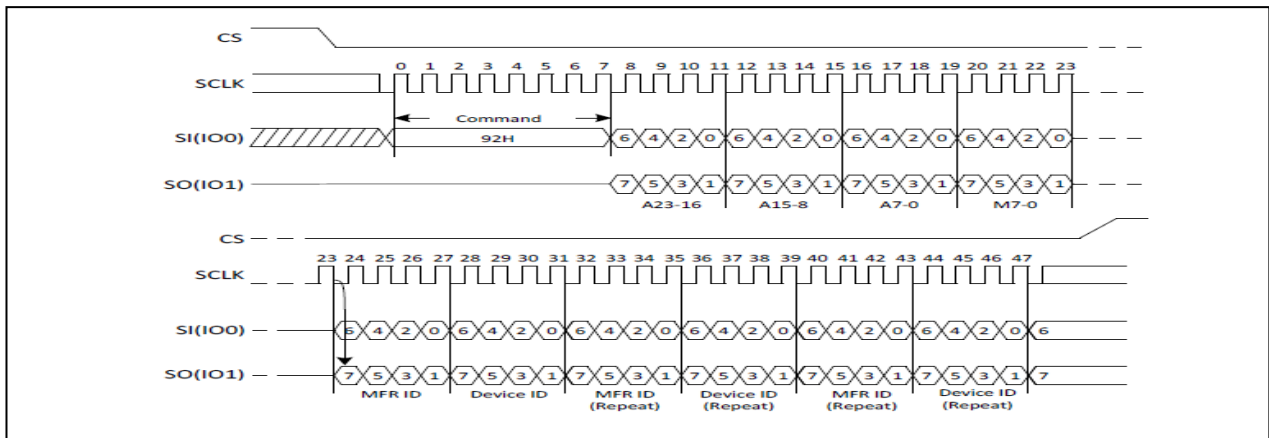
Figure27. Continuous Read Mode Reset Sequence Diagram

Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code "92H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 27.1 If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure27.1 Read Manufacture ID/ Device ID Dual I/O Sequence Diagram

Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The command is initiated by driving the CS# pin low and shifting the command code "94H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 28. If the 24-bit address is initially set to 000001H, the Device ID will be read first.
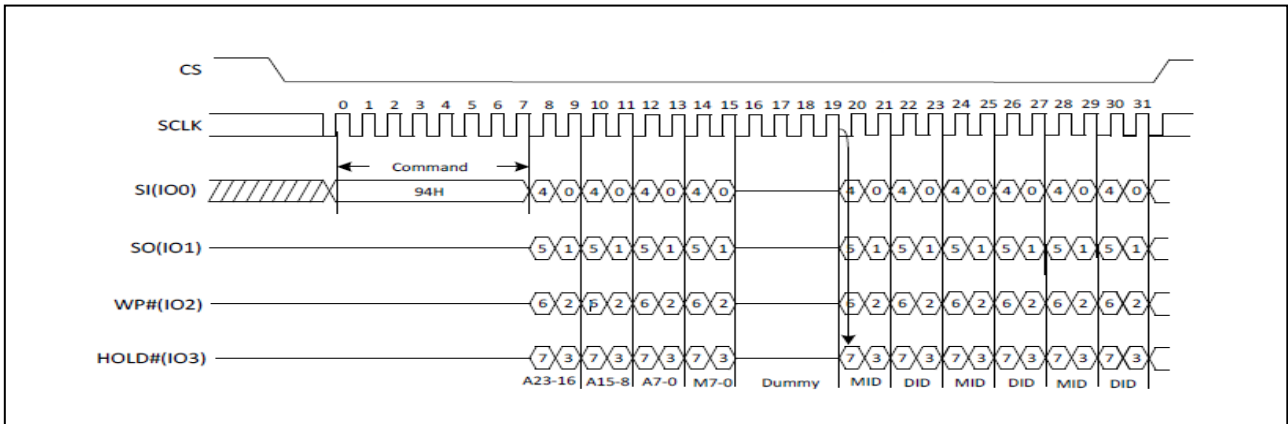
Figure28. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram

Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure29. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.
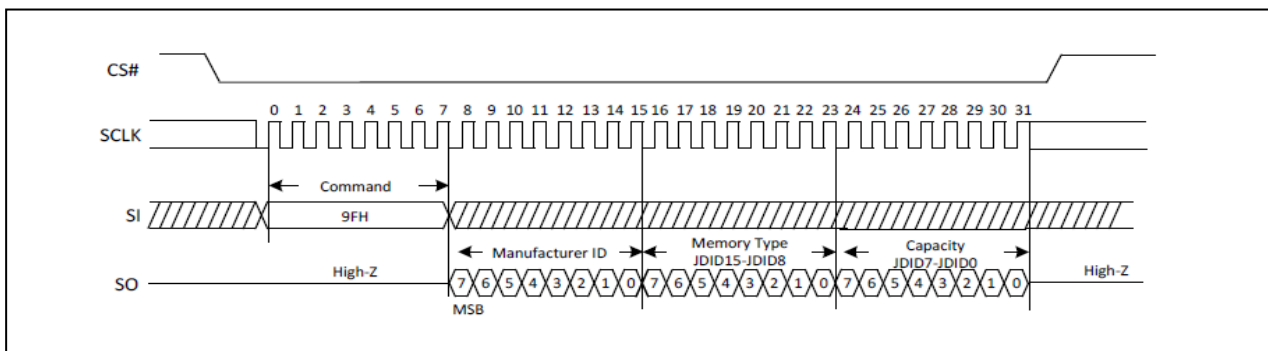

Figure29. Read Identification ID Sequence Diagram

Erase Security Registers (44H)

The ACE25AA400G provides four 256-byte Security Registers which only erased all at once but able to program individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low, sending Erase Security Registers Command, CS# goes high. The command sequence is shown in Figure 30. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

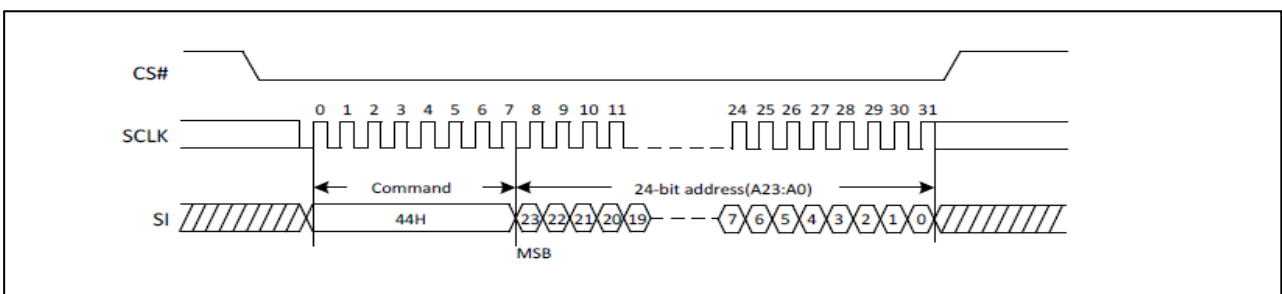| Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Don't Care

Figure30. Erase Security Registers command Sequence Diagram

Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

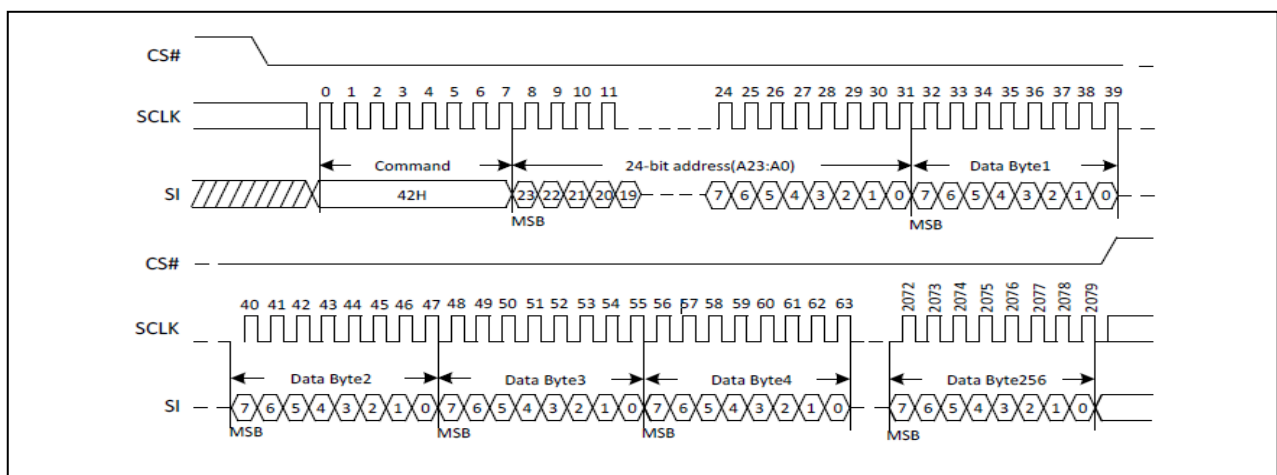| Address	A23-A16	A15-A8	A7-A0
Security Register0	00H	00H	Byte Address
Security Register1	00H	01H	Byte Address
Security Register2	00H	02H	Byte Address
Security Register3	00H	03H	Byte Address

Figure31. Program Security Registers command Sequence Diagram

Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3- byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically increment- ed to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

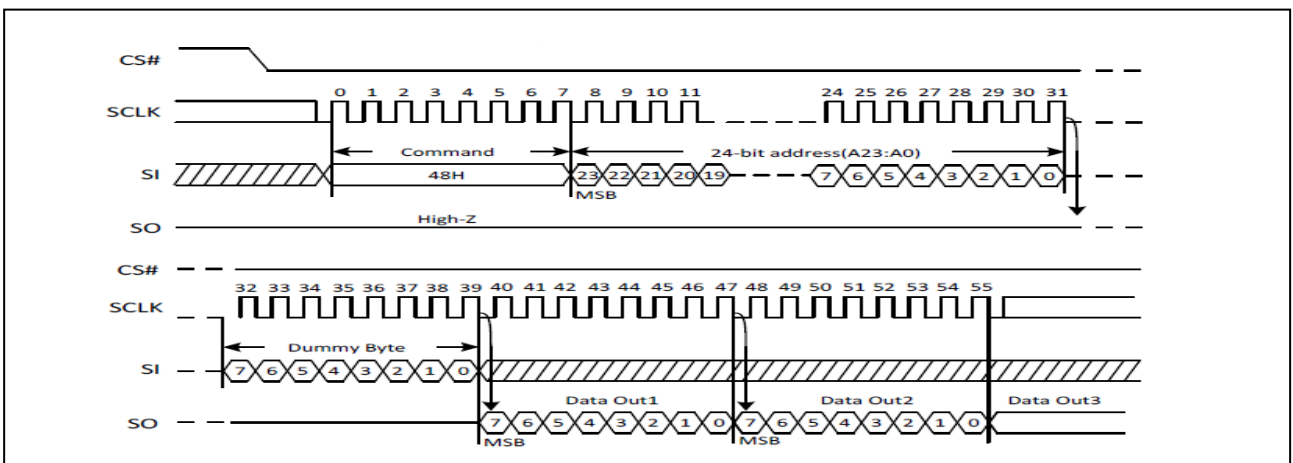| Address	A23-A16	A15-A10	A9-A0
Security Register	00000000	000000	Address

Figure32. Read Security Registers command Sequence Diagram

Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low Sending Enable Reset command CS# goes high CS# goes low Sending Reset command CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRSTR to reset. During this period, no command will be accepted. Data corruption may happy if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command sequence.
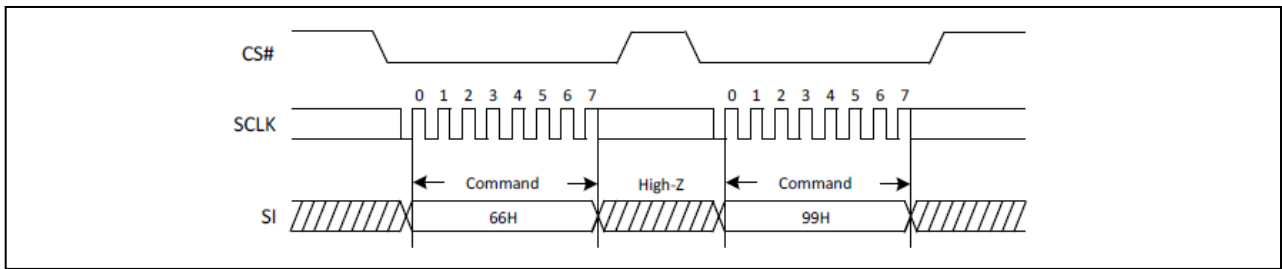
Figure33. Enable Reset and Reset command Sequence Diagram

Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.
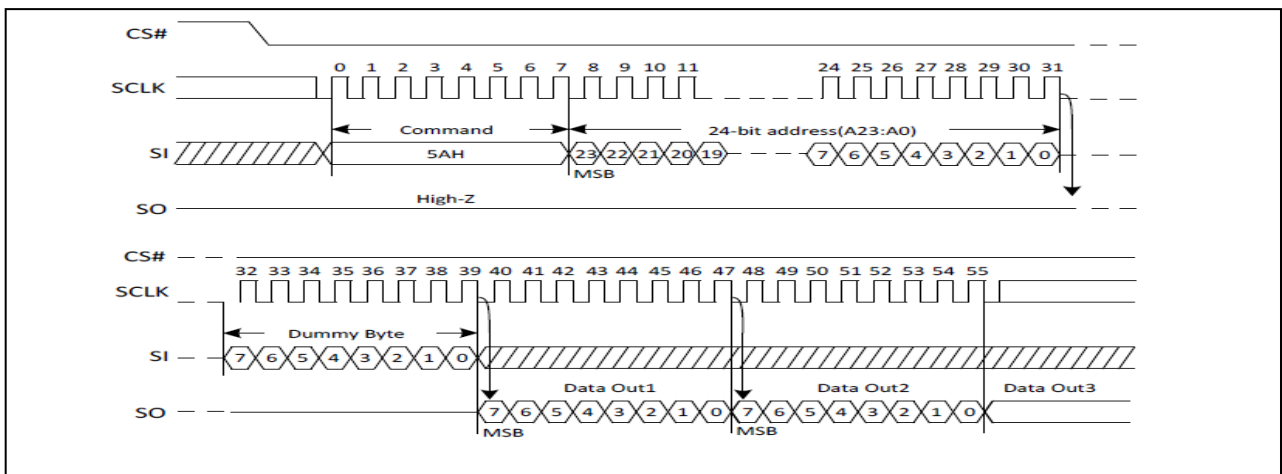

Figure34. Read Serial Flash Discoverable Parameter command Sequence Diagram

Read Unique ID (RUID)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each ACE25AA400G device. The Unique ID can be used in conjunction with user software methods to help prevent copy- ing or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →00H →01H→94H→ Dummy byte 128bit Unique ID Out → CS# goes high.

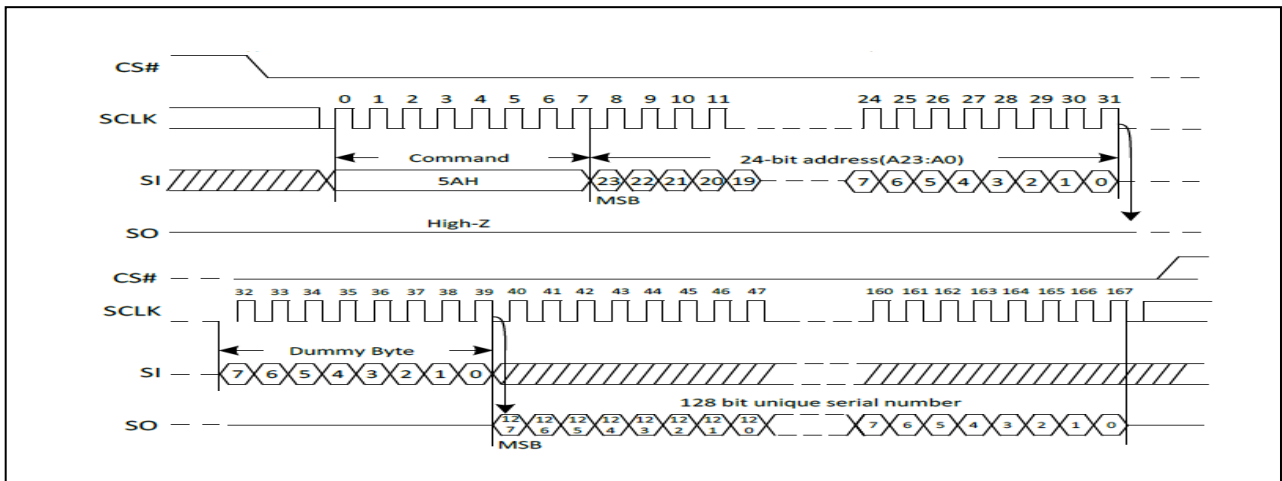The command sequence is show below.

Figure34.1 Read Unique ID (RUID) Sequence (Command 5AH)

Table 3. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDS in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number(ACE Manufacturer ID)	It is indicates ACE manufacturer ID	10H	07:00	0BH	0BH
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDS in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table 4. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	007FFFFFH	

(1-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states		3EH	20:16	00010b	42H
(1-2-2) Fast Read Number of Mode Bits			23:21	010b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH

(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

Table 5. Parameter Table (1): ACE Flash Parameter Tables

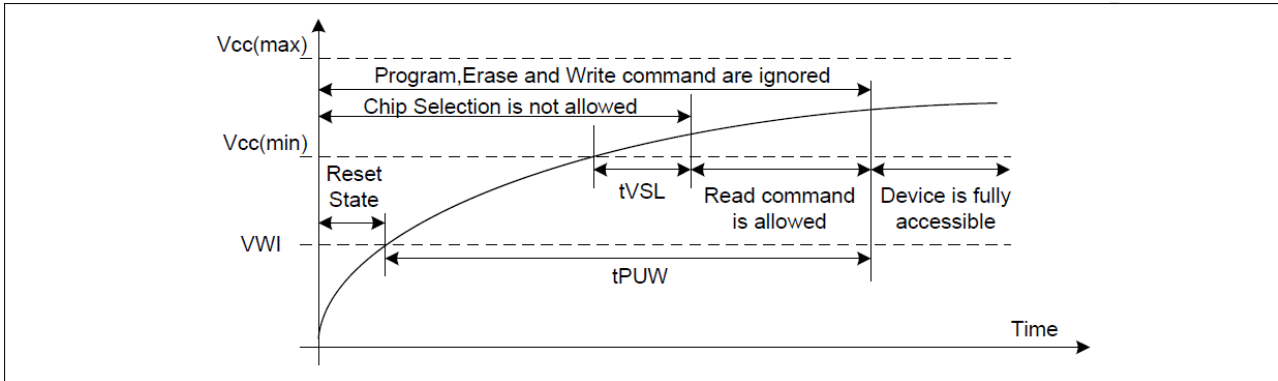| Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2300H=2.300V 2700H=2.700V	63H:62H	31:16	2700H	2700H
HW Reset# pin	0=not support 1=support		00	0b	
HW Hold# pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	0b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd	65H:64H	11:04	99H	7994H
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	0b	
Wrap-Around Read mode Opcode		66H	23:16	FFH	FFH
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support		00	0b	
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect	6BH:68H	10	0b	E3FCH
Secured OTP	0=not support 1=support		11	0b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

Electrical Characteristics
Power-On Timing

Table6. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	10		us
t_{PUW}	Time Delay Before Write Instruction	1	10	ms
V_{WI}	Write Inhibit Voltage	1	2.5	V

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

Data Retention and Endurance

Parameter	Typical	Unit
Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

Latch up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

Capacitance Measurement Condition

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			6	pF	VIN=0V
C_{OUT}	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Maximum Negative Overshoot Waveform
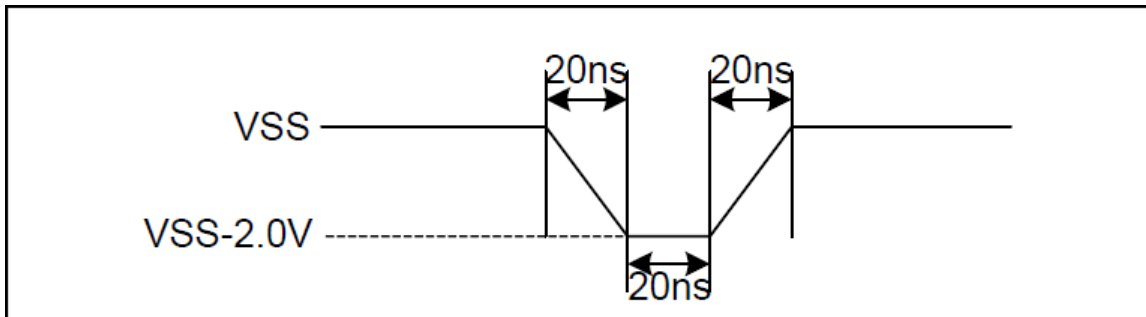
Maximum Positive Overshoot Waveform
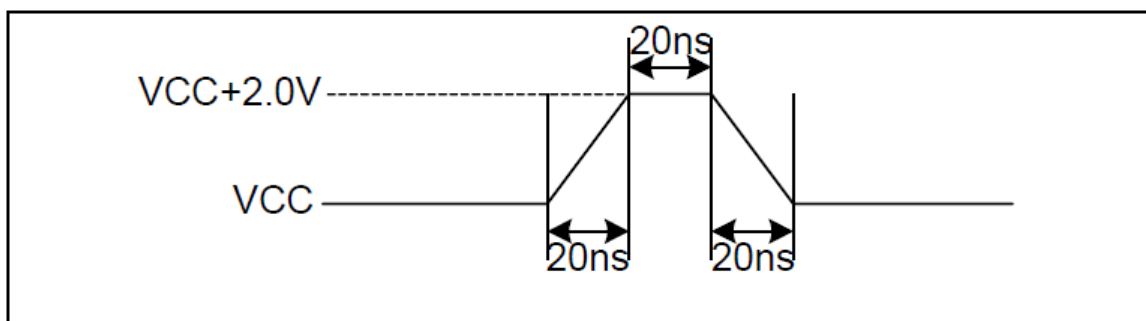
Figure35. Input Test Waveform and Measurement Level

DC Characteristics(T=-40℃~85℃,VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		12	20	µA
I_{CC2}	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		0.03	0.05	µA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 120MHz ,Q=Open(*1I/O)		15	20	mA
		CLK=0.1VCC/0.9VCC at 80MHz,Open(*1,*2,4I/O)		13	18	
		CLK=0.1VCC/0.9VCC at 50MHz ,Q=Open(*1I/O)		5	7	
I_{CC4}	Operating Current(PP)	CS#=VCC			20	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			20	mA
I_{CC6}	Operating Current(SE)	CS#=VCC			20	mA
I_{CC7}	Operating Current(BE)	CS#=VCC			20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100uA	VCC-0.2			V

AC Characteristics(T=-40℃~85℃,VCC=2.7~3.6V，C$_L$=30pf)

Symbol	Parameter	Min.	Typ	Max.	Unit
fC	Serial Clock Frequency For: Fast Read(0BH),Dual Output(3BH)			108	MHz
fC1	Serial Clock Frequency For: Dual I/O (BBH),Quad I/O(EBH),Quad Output(6BH)		80	108	MHz
fR	Serial Clock Frequency For: Read(03H)			80	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time(relative to Clock)	5			ns
tHHCH	Hold# High Setup Time(relative to Clock)	5			ns
tCHHL	Hold# High Hold Time(relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time(relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			6	ns
tHHQX	Hold# Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid			6.5	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			0.1	us
tRES1	CS# High To Standby Mode Without Electronic Signature Read			20	us
tRES2	CS# High To Standby Mode With Electronic Signature Read			20	us

tRST_R	CS# High To Next Command After Reset (from read)			20	us
tRST_P	CS# High To Next Command After Reset (from program)			20	us
tRST_E	CS# High To Next Command After Reset (from erase)			12	ms
tW	Write Status Register Cycle Time		60	500	ms
tPP	Page Programming Time		0.4	0.75	ms
tSE	Sector Erase Time		60	500	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.15/0.25	0.5/0.75	s
tCE	Chip Erase Time		1.25	5	s

Figure36. Serial Input Timing
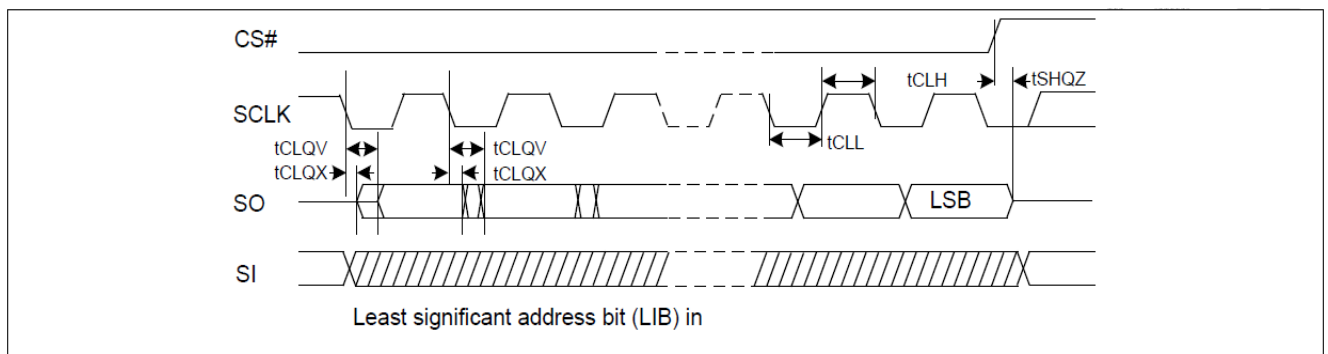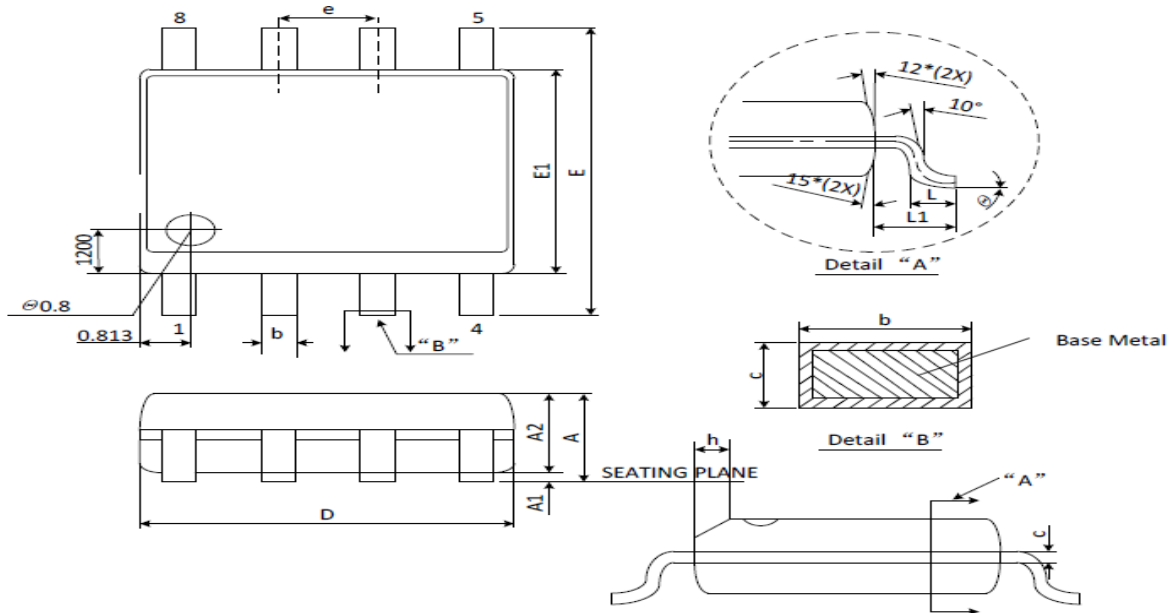
Figure37. Output Timing
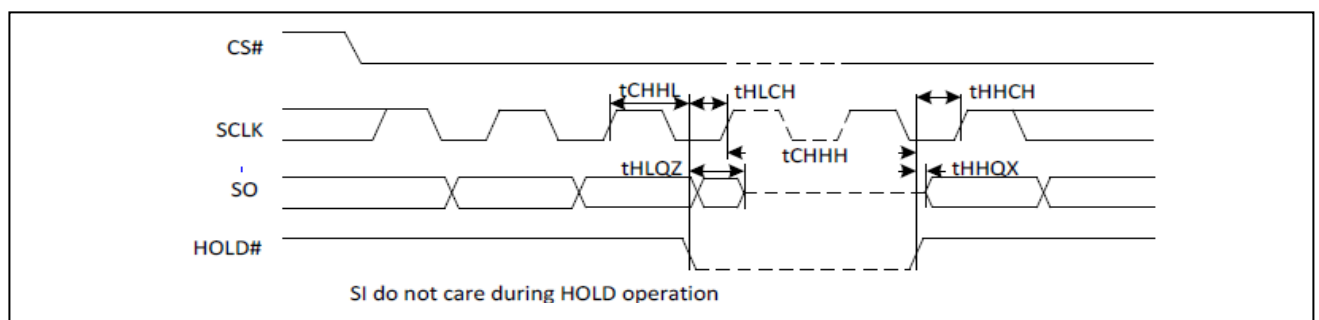
Figure38. Hold Timing

VER 1.3   44

Packaging information

SOP-8

Symbol	Dimensions In Millimeters		
	Min	Norm	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.300		1.500
b	0.330		0.510
c	0.190		0.250
D	4.700	4.900	5.000
E1	3.800	3.900	4.000
e		1.270	
E	5.800	6.000	6.200
h	0.250	0.350	0.500
L	0.508	0.635	0.762
L1	0.837	1.040	1.243
θ	0°		8°

Note:
1. Coplanarity: 0.1mm
2. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.
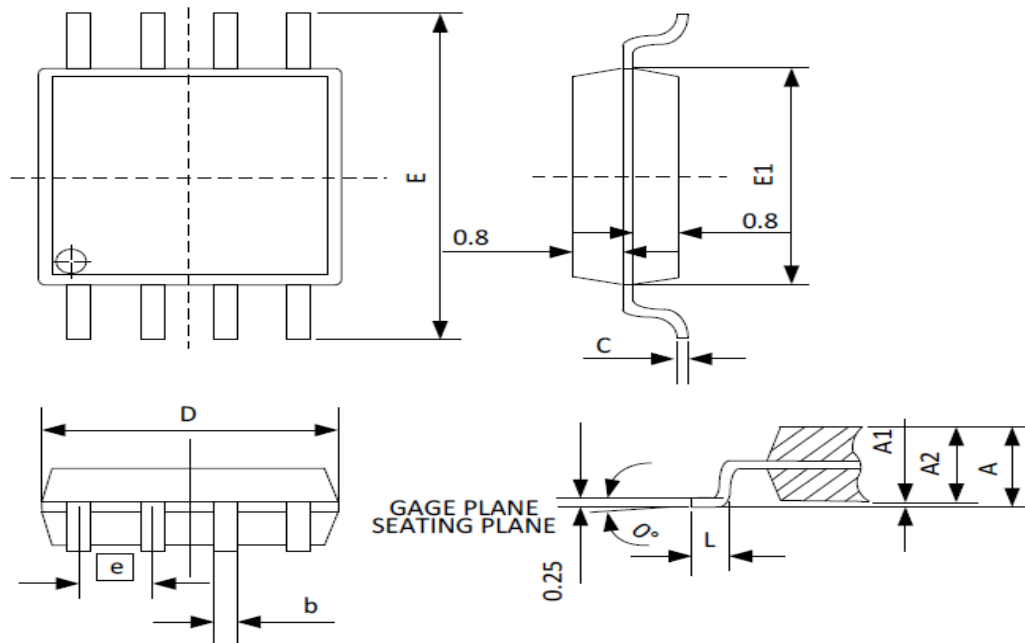3. All dimensions follow JEDEC MS-012 standard.

Packaging information

SOP-8L (208mil)

Symbol	Dimensions In Millimeters		
	Min	Norm	Max
A	1.750	1.950	2.160
A1	0.050	0.150	0.250
A2	1.700	1.800	1.910
b	0.350	0.420	0.480
c	0.190	0.200	0.250
D	5.130	5.230	5.330
E	7.700	7.900	8.100
E1	5.180	5.280	5.380
e	1.270 BSC		
L	0.500	0.650	0.800
θ	0°		8°

Note:
1. JEDEC Outline : N/A
2. Coplanarity: 0.1mm
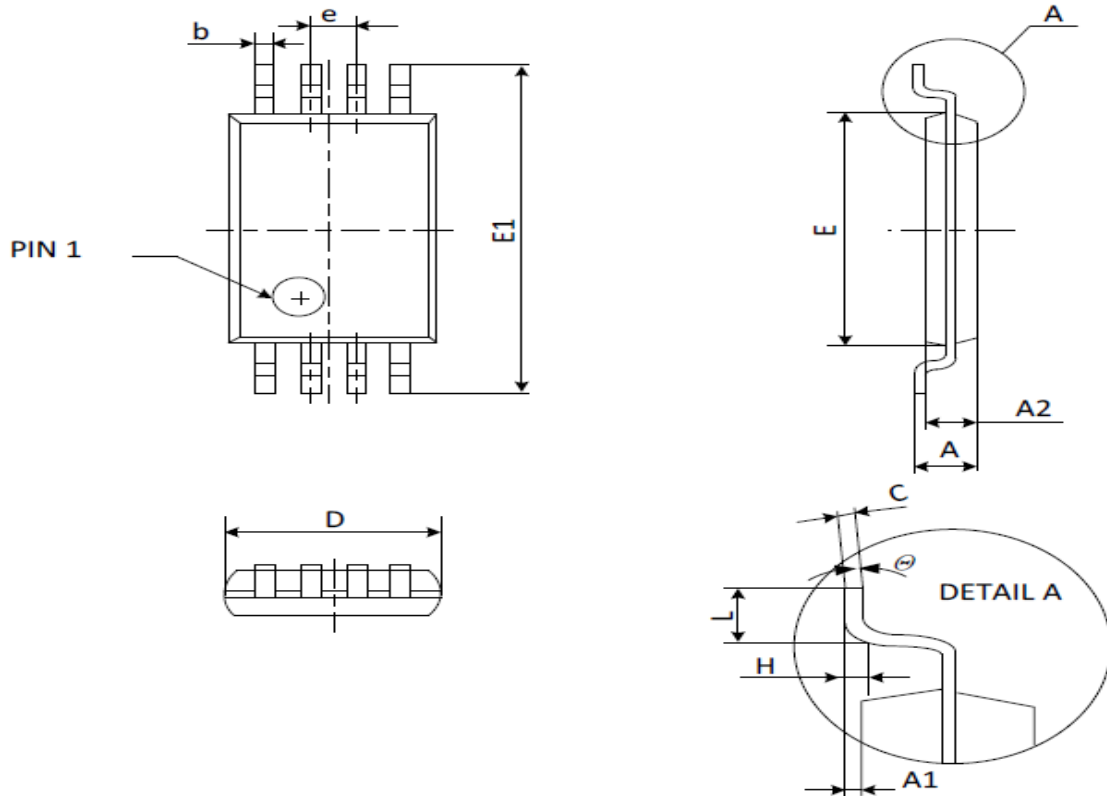3. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.

Packaging information

TSSOP-8

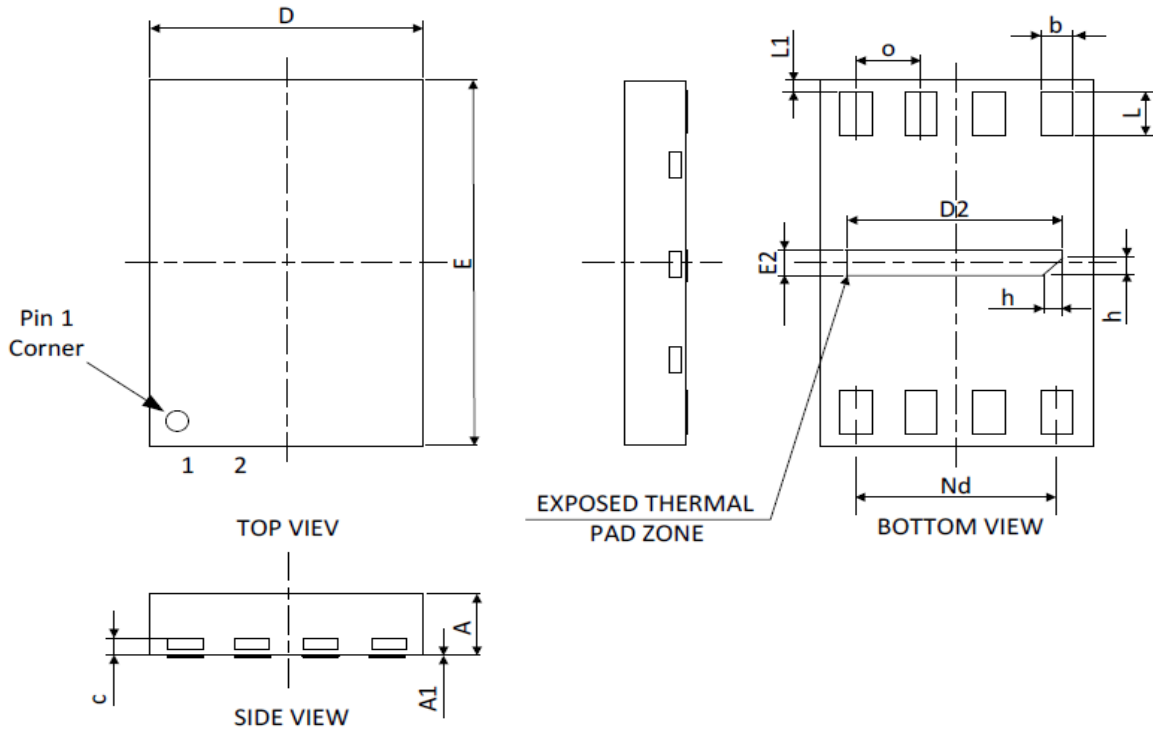| Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

Packaging information

USON3*2-8

Symbol	Dimensions In Millimeters		
	Min	Norm	Max
A	0.500	0.550	0.600
A1	0.000	0.020	0.050
b	0.180	0.250	0.030
c	0.100	0.150	0.200
D	1.900	2.000	2.100
D2	1.500	1.600	1.700
e	0.500BSC		
Nd	1.500BSC		
E	2.900	3.000	3.100
E2	0.100	0.200	0.300
L	0.300	0.350	0.400
L1	0.050	0.100	0.150
h	0.050	0.150	0.250

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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