ACE25C800G

Uniform SECTOR Dual and Quad Serial Flash

Description

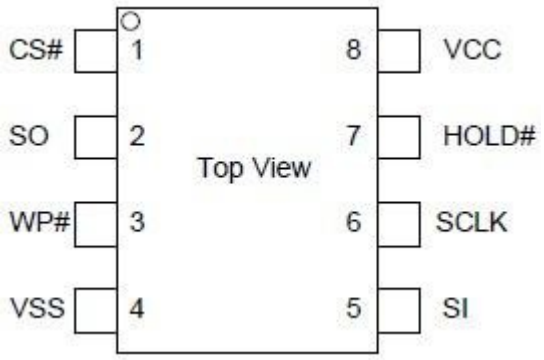
The ACE25C800G (8M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI),I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 240Mbits/s and the Quad I/O & Quad output data is transferred with speed of 432Mbits/s.

Features

- 8M-bit Serial Flash
  - -1024K-byte
  - -256 bytes per programmable page
- Standard, Dual, Quad SPI
  - -Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - -Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - -Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- High Speed Clock Frequency
  - -108MHz for fast read with load
  - -Dual I/O Data transfer up to 216Mbits/s
  - -Quad I/O Data transfer up to 432Mbits/s
- Software/Hardware Write Protection
  - -Write protect all/portion of memory via software
  - -Enable/Disable protection with WP# Pin
  - -Top or Bottom, Sector or Block selection
- Minimum 100,000 Program/Erase Cycles
- Program/Erase Speed
  - -Page Program time: 0.7ms typical
  - -Sector Erase time: 100ms typical
  - -Block Erase time: 0.2/0.4s typical
  - -Chip Erase time: 7s typical
- Flexible Architecture
  - -Sector of 4K-byte
  - -Block of 32/64k-byte
- Low Power Consumption
  - -20mA maximum active current
  - -5uA maximum power down current
- Advanced security Features(1)
  - -3*256-Byte Security Registers With OTP Lock
- Voltage, Temperature Range
  - -Full voltage range: 2.7~3.6V
  - -40℃ to 85℃ operating range

Packaging Type

DIP-8 / SOP-8 / SOP-8 (208mil)



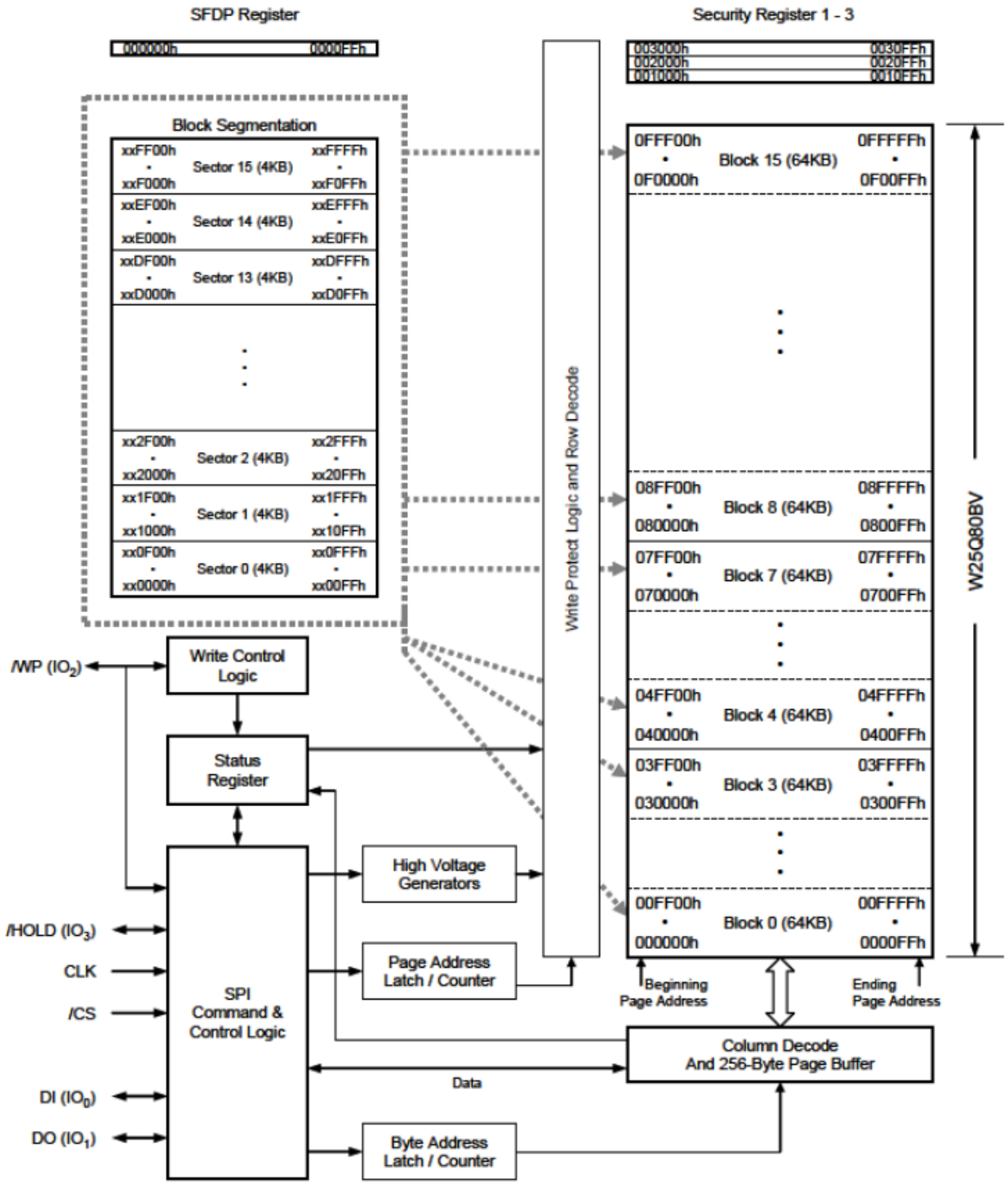
Pin Configurations

Pin No	Pin Name	I/O	Function
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
8	VCC		Power Supply

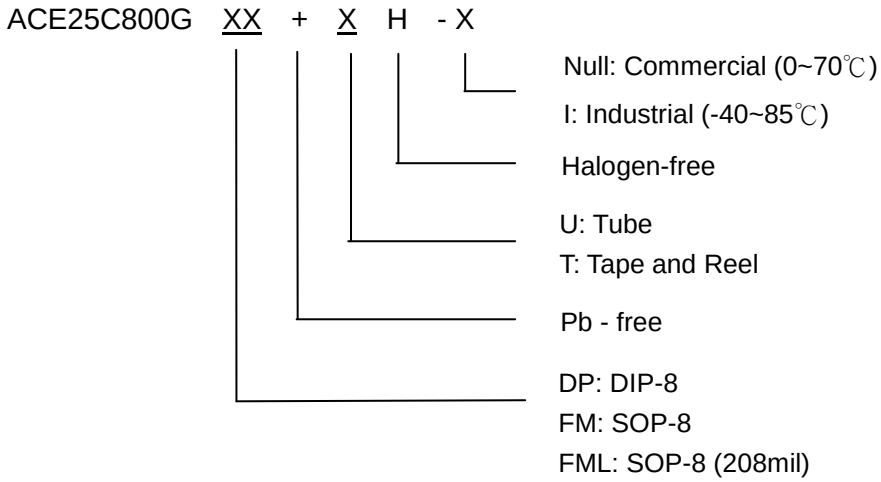
Memory Organization

Each device has	Each block has	Each sector has	Each page has	
1M	64/32K	4K	256	bytes
4K	256/128K	16	-	pages
256	16/8	-	-	sectors
16/32	-	-	-	blocks

Block Diagram



Ordering information



Uniform Block Sector Architecture

ACE25C800G 64K Bytes Block Sector Architecture

Block	Sector	Address range	
15	255	0FF000H	0FFFFFH
	….	….	….
	240	0F0000H	0F0FFFH
14	239	0EF000H	0EFFFFH
	….	….	….
	224	0E0000H	0E0FFFH
….	….	….	….
	….	….	….
….	….	….	….
	….	….	….
	….	….	….
2	47	02F000H	02FFFFH
	….	….	….
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	….	….	….
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	….	….	….
	0	000000H	000FFFH

Device Operation

SPI Mode

Standard SPI

The ACE25C800G features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The ACE25C800G supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The ACE25C800G supports Quad SPI operation when using the “Quad Output Fast Read”,” Quad I/O Fast Read”, “Quad I/O Word Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

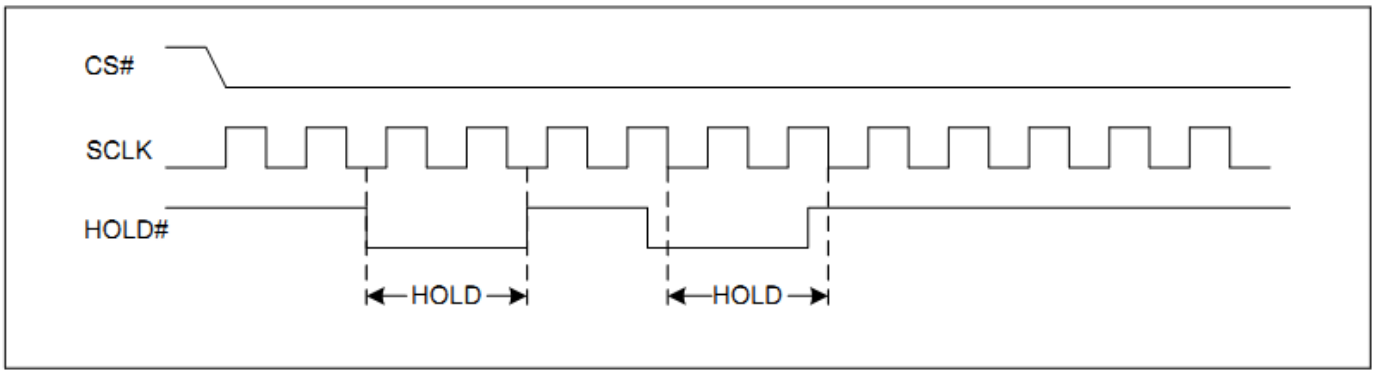


Figure1. Hold Condition

Data Protection

The ACE25C800G provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up
  -Write Disable (WRDI)
  -Write Status Register(WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect (SEC, TB, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~SEC bits and SRP0~1 bits.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from deep Power-Down Mode command.

Table1.0 ACE25C800G Protected area size (CMP=0)

Status Register Content					Memory Content			
SEC	**TB**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000H-0FFFFFH	64KB	Upper 1/16
0	0	0	1	0	14 to 15	0E0000H-0FFFFFH	128KB	Upper 1/8
0	0	0	1	1	12 to 15	0C0000H-0FFFFFH	256KB	Upper 1/4
0	0	1	0	0	8 to 15	080000H-0FFFFFH	512KB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/16
0	1	0	1	0	0 to 1	000000H-01FFFFH	128KB	Lower 1/8
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/4
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/2
0	X	1	0	1	0 to 15	000000H-0FFFFFH	1M	ALL
X	X	1	1	X	0 to15	000000H-0FFFFFH	1M	ALL
1	0	0	0	1	15	0FF000H-0FFFFFH	4KB	Top Block
1	0	0	1	0	15	0FE000H-0FFFFFH	8KB	Top Block
1	0	0	1	1	15	0FC000H-0FFFFFH	16KB	Top Block
1	0	1	0	X	15	0F8000H-0FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block

Table1.1 ACE25C800G Protected area size (CMP=1)

Status Register Content					Memory Content			
SEC	TB	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 15	000000H-1FFFFFH	1M	ALL
0	0	0	0	1	0 to 14	000000H-0EFFFFH	960KB	Lower 15/16
0	0	0	1	0	0 to 13	000000H-0DFFFFH	896KB	Lower 17/8
0	0	0	1	1	0 to 11	000000H-1BFFFFH	768KB	Lower 3/4
0	0	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/2
0	1	0	0	1	1 to 15	010000H-0FFFFFH	960KB	Upper 15/16
0	1	0	1	0	2 to 15	020000H-0FFFFFH	896KB	Upper 7/8
0	1	0	1	1	4 to 15	040000H-0FFFFFH	768KB	Upper 3/4
0	1	1	0	0	8 to 15	080000H-0FFFFFH	512KB	Upper 1/2
0	X	1	0	1	NONE	NONE	NONE	NONE
X	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 15	000000H-0FEFFFH	1020KB	L-255/256
1	0	0	1	0	0 to 15	000000H-0FDFFFH	1016KB	L-127/128
1	0	0	1	1	0 to 15	000000H-0FBFFFH	1008KB	L-63/64
1	0	1	0	X	0 to 15	000000H-0F7FFFH	992KB	L-31/32
1	1	0	0	1	0 to 15	001000H-0FFFFFH	1020KB	U-255/256
1	1	0	1	0	0 to 15	002000H-0FFFFFH	1016KB	U-127/128
1	1	0	1	1	0 to 15	004000H-0FFFFFH	1008KB	U-63/64
1	1	1	0	X	0 to 15	008000H-0FFFFFH	992KB	U-31/32

Status Register

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	LB3	LB2	LB1	Reserved	QE	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	SEC	TB	BP2	BP1	BP0	WEL	W1P

The status and control bits of the Status Register are as follows:

WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

SEC, TB, BP2, BP1, BP0 bits

The Block Protect (SEC, TB, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (SEC, TB, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (SEC, TB, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, BP0) bits are “000” when CMP=0, or “110/111” when CMP=1.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	#WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and can not be written to
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1
1	0	X	Power Supply Lock- Down(1)	Status Register is protected and can not be written to again until the next Power-Down, Power-Up cycle
1	1	X	One Time Program (2)	Status Register is permanently protected and can not be written to

Note:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0,0) state.
2. 2The One time Program feature is available upon special order. Please contact ACE for details.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground)

LB3/LB2/LB1 bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S10) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it’s set to 1, the Security Registers will become read-only permanently. LB0 is reserved, LB3/2/1 for Security Registers 3:1.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the SEC-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

SUS bit

The SUS bit is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75H) command. The SUS bit is cleared to 0 by Erase/Program Resume (7AH) command as well as a power-down, power-up cycle.

Commands Description

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Enable for Volatile Status Register	50H						
Write Status Register	01H	(S7-S0)					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	Dummy(5)	(D7-D0)(3)			(continuous)
Continuous Read Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Program/Erase Suspend	75H						
Program/ Erase Resume	7AH						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/Device ID	90H	dummy	dummy	00H	(M7-M0)	(ID7-ID0)	(continuous)
Read Identification	9FH	(M7-M0)	(ID15-ID8)	(ID7-ID0)			(continuous)
Erase Security Registers (8)	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers (8)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	
Read Security Registers (8)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	

Note:

1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
2. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
3. Quad Output Data
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3,…..)
4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
5. Fast Read Quad I/O Data
   IO0 = (x, x, x, x, D4, D0,…)
   IO1 = (x, x, x, x, D5, D1,…)
   IO2 = (x, x, x, x, D6, D2,…)
   IO3 = (x, x, x, x, D7, D3,…)
6. Security Registers Address:
   Security Register: A23-A16=00000000b, A15-A10=0000b, A9-A0= Address;

Table of ID Definitions

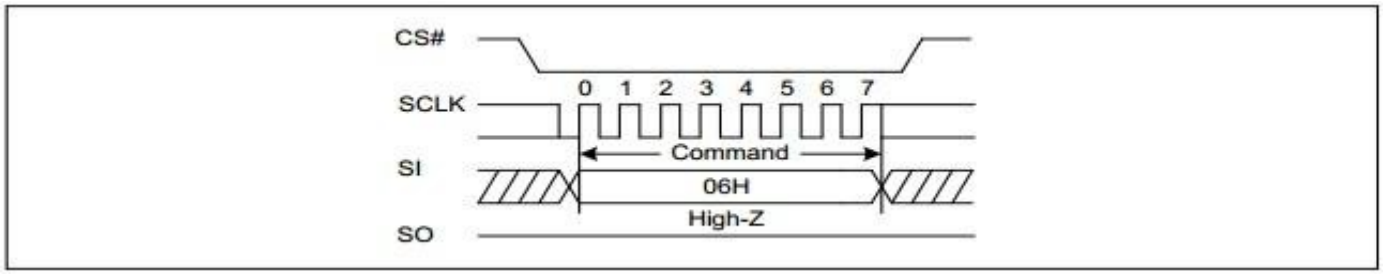
ACE25C800G

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	E0	40	14
90H	E0		13
ABH			13

Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low sending the Write Enable command CS# goes high.

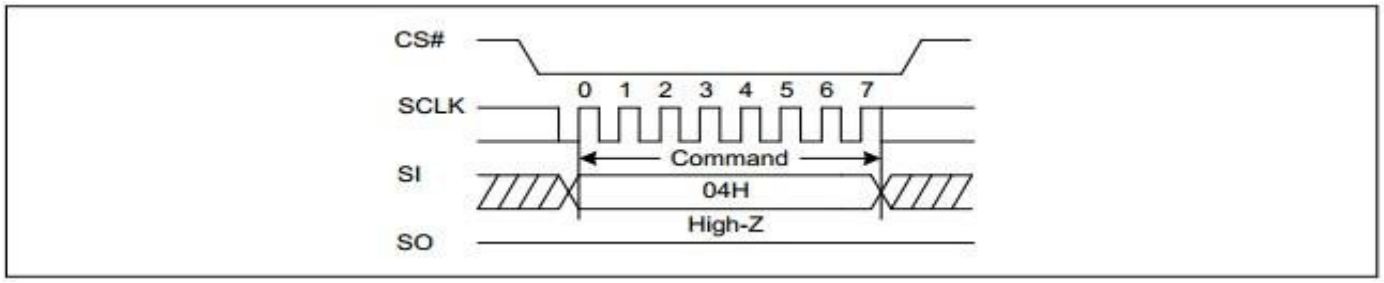
Figure2. Write Enable Sequence Diagram



Write Disable (WRDI)(04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low Sending the Write Disable command CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

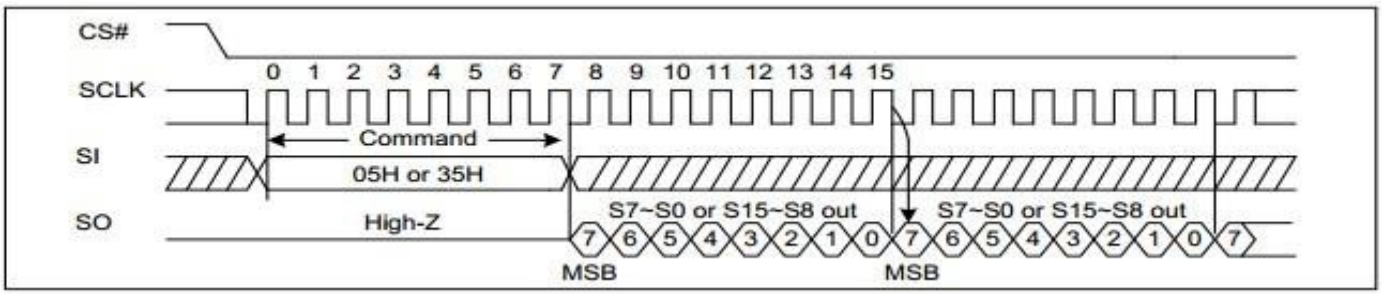
Figure3. Write Disable Sequence Diagram



Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

Figure4. Read Status Register Sequence Diagram



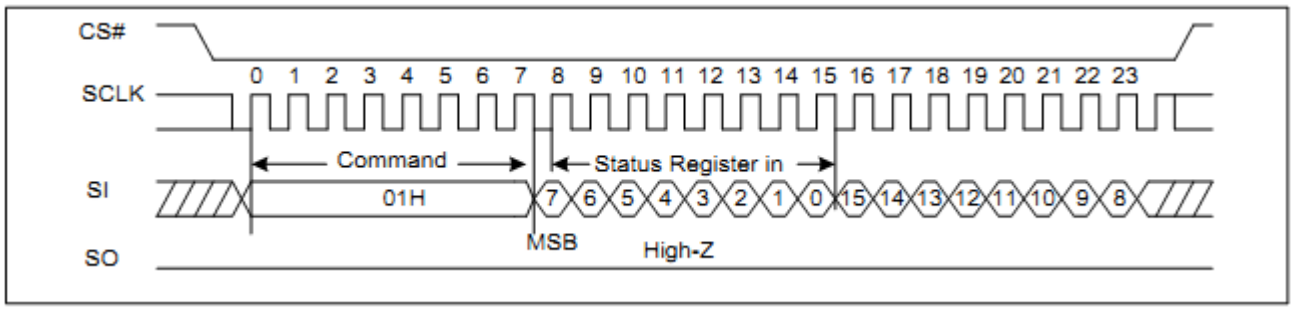
Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE and SRP1 bits will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (SEC, TB, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

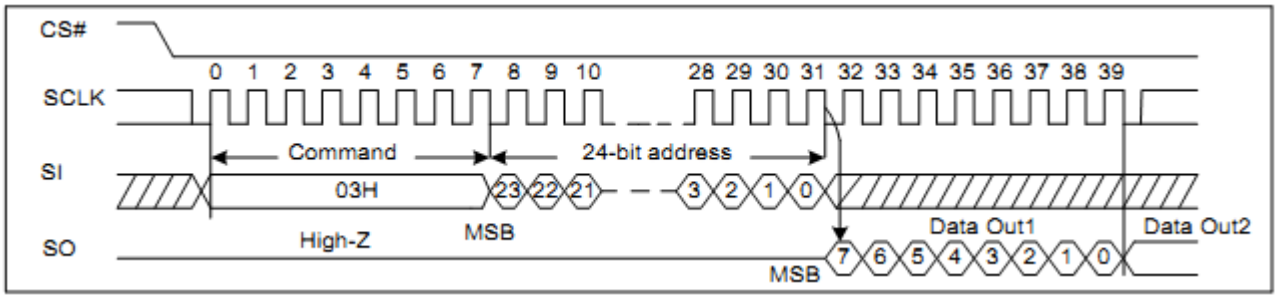
Figure5. Write Status Register Sequence Diagram



Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

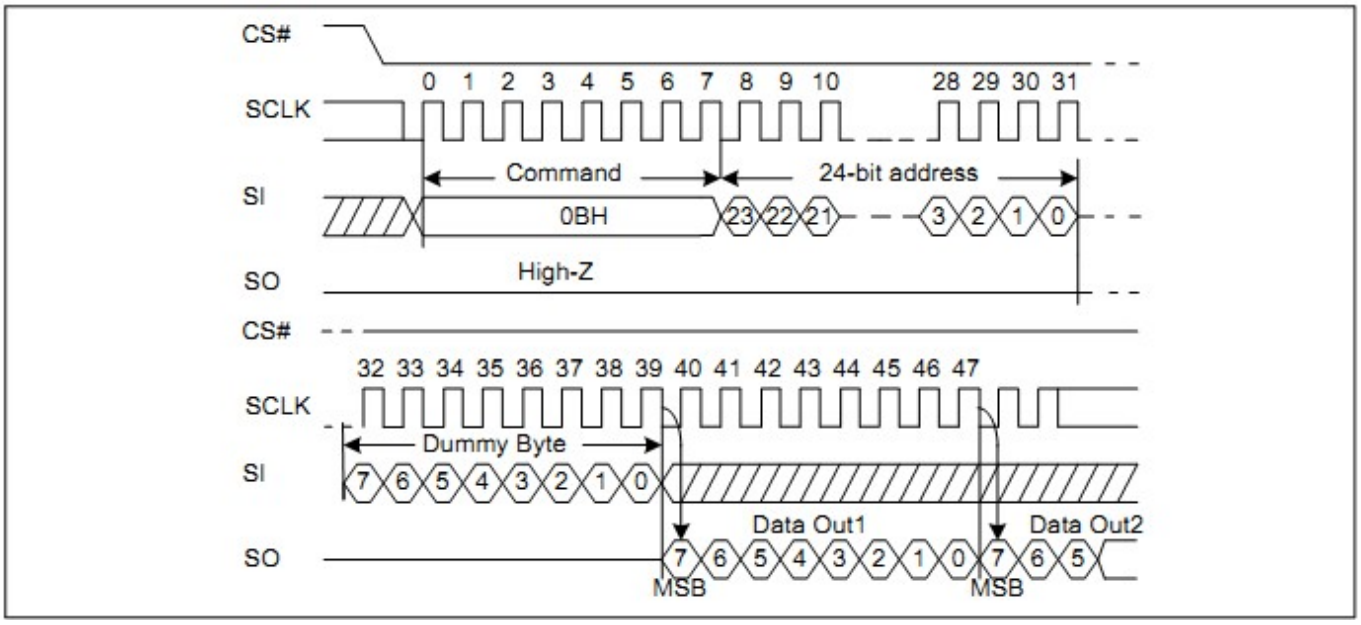
Figure6. Read Data Bytes Sequence Diagram



Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3- byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

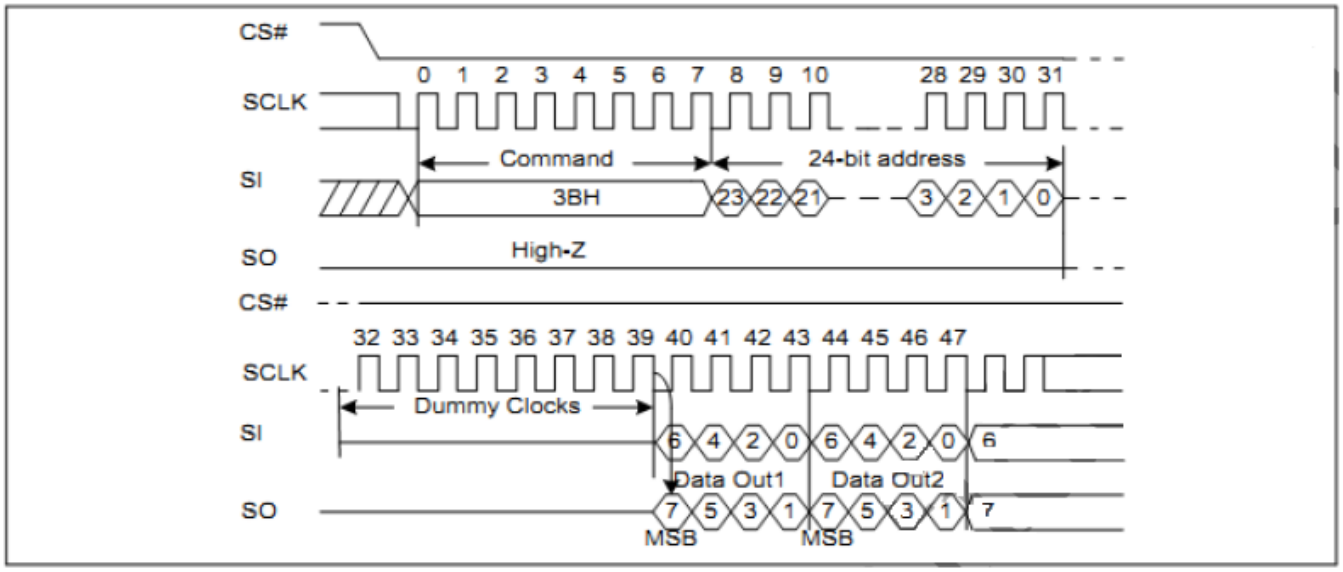
Figure7. Read Data Bytes at Higher Speed Sequence Diagram



Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

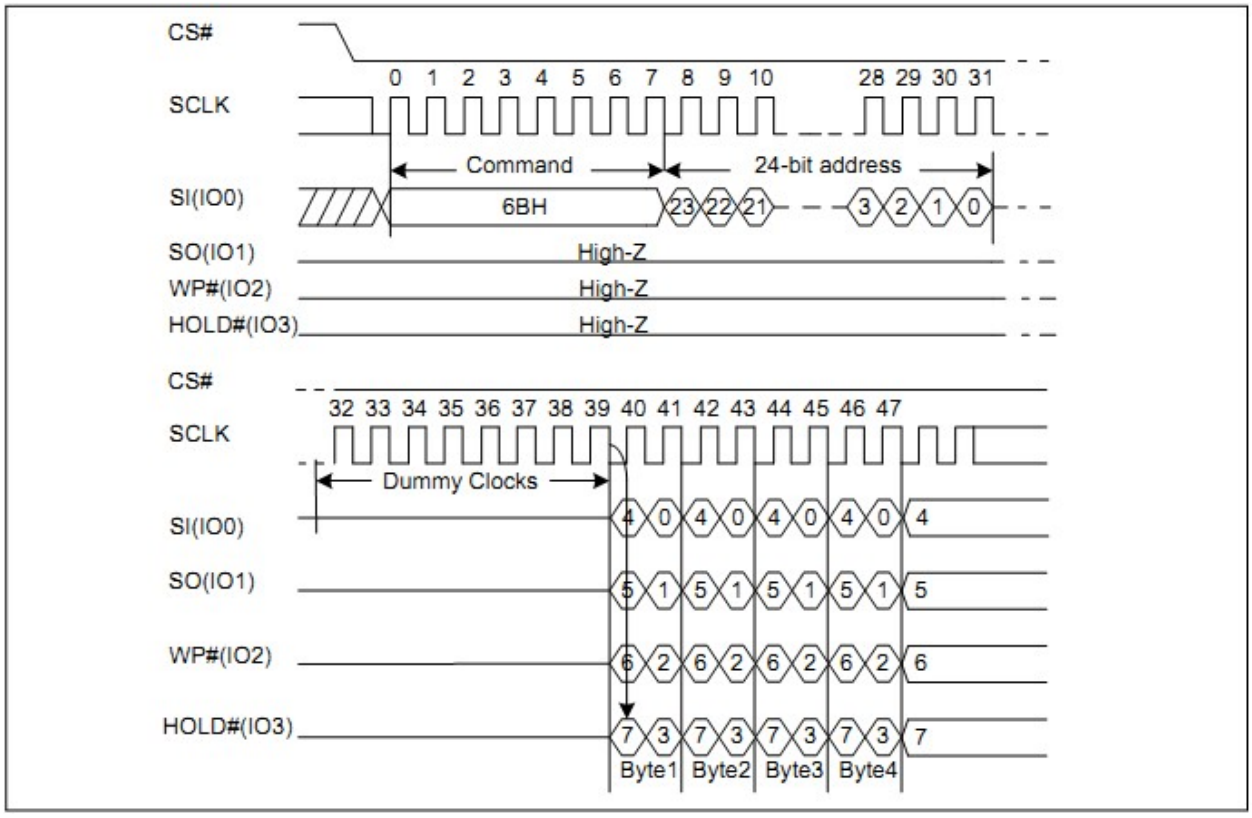
Figure8. Dual Output Fast Read Sequence Diagram



Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure9. Quad Output Fast Read Sequence Diagram



Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read With “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) =AXH, then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure11. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

Figure10. Dual I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)

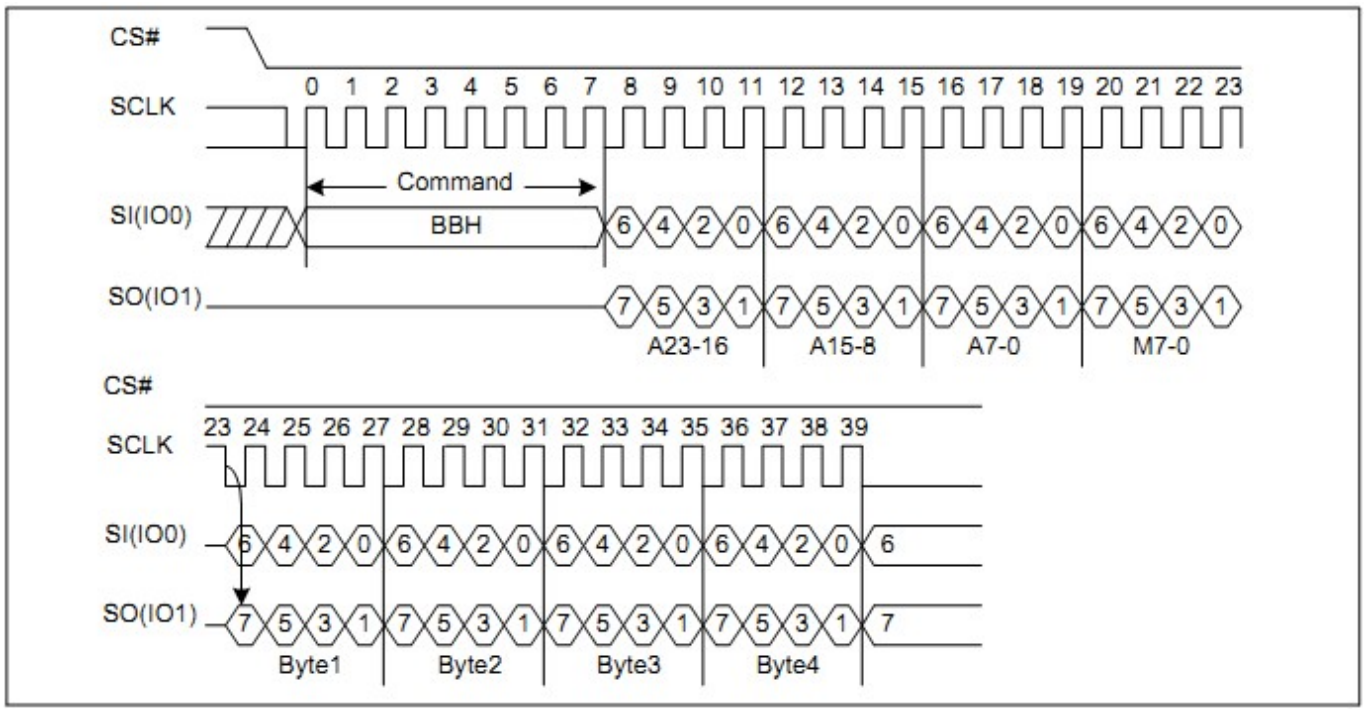
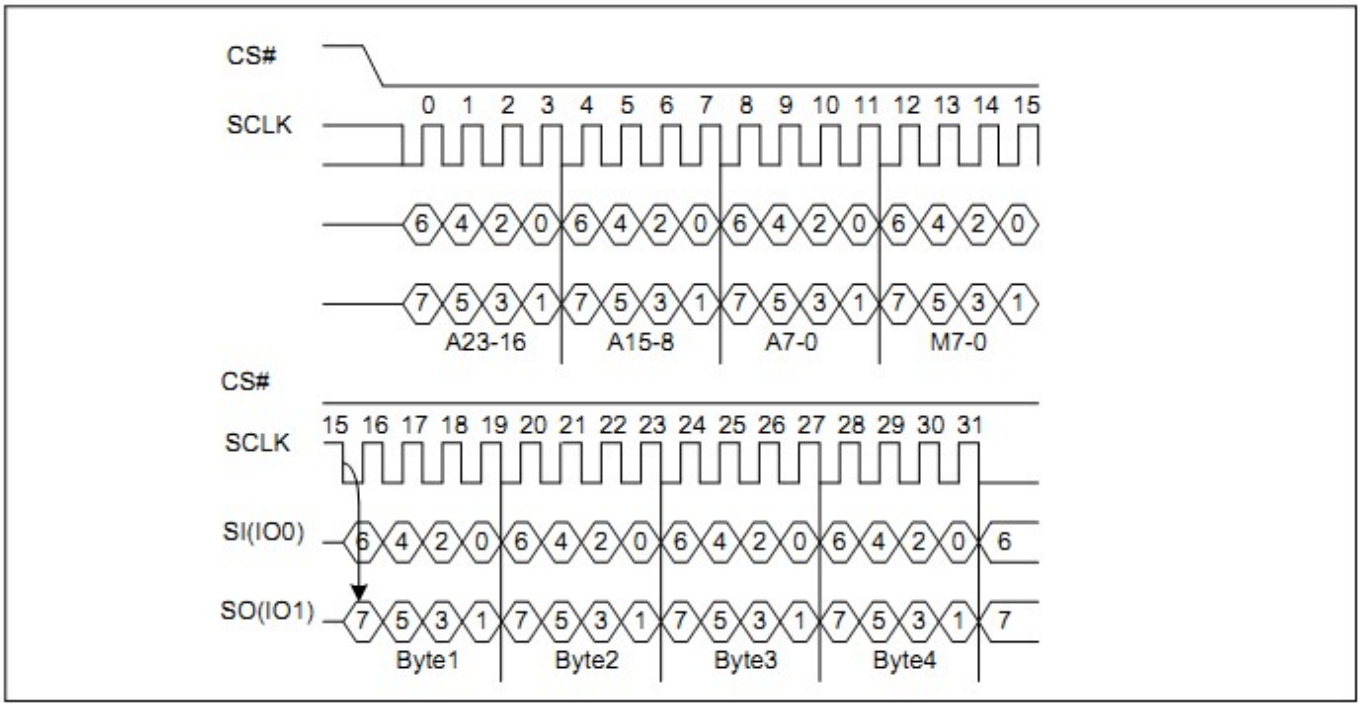


Figure11. Dual I/O Fast Read Sequence Diagram (M7-0= AXH)



Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure12. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read With “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) =AXH, then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure13. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

Figure12. Quad I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)

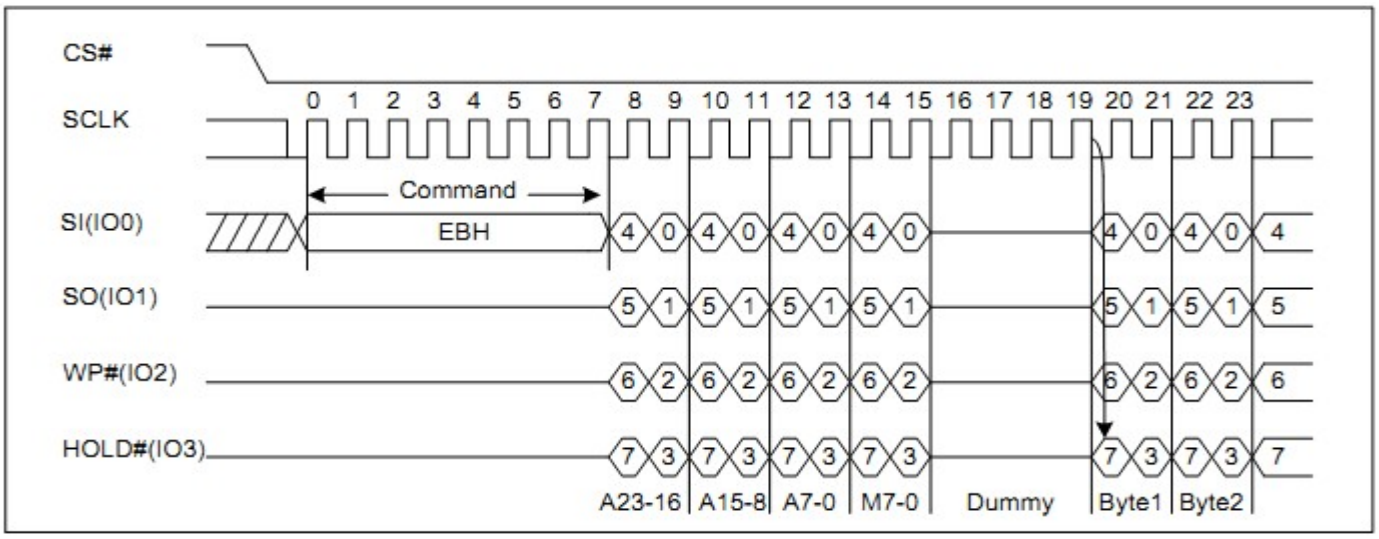
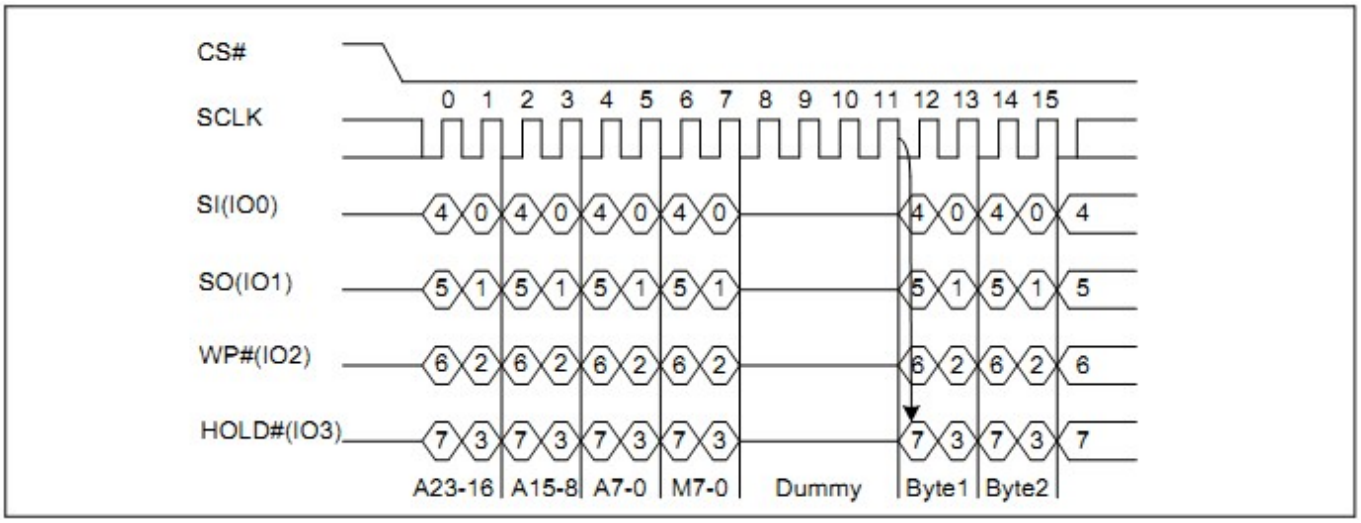


Figure13. Quad I/O Fast Read Sequence Diagram (M7-0= AXH)



Page Program (PP) (02H)

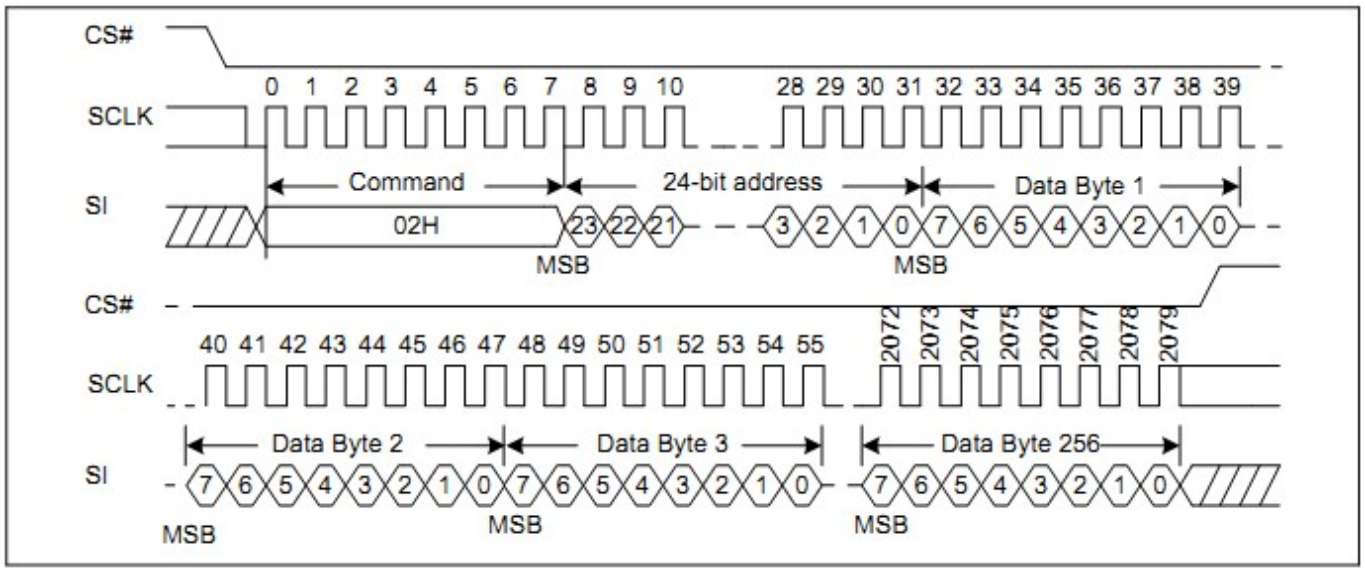
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low sending Page Program command 3-byte address on SI at least 1 byte data on SI CS# goes high. The command sequence is shown in Figure14. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (SEC, TB, BP2, BP1,BP0) is not executed.

Figure 14. Page Program Sequence Diagram

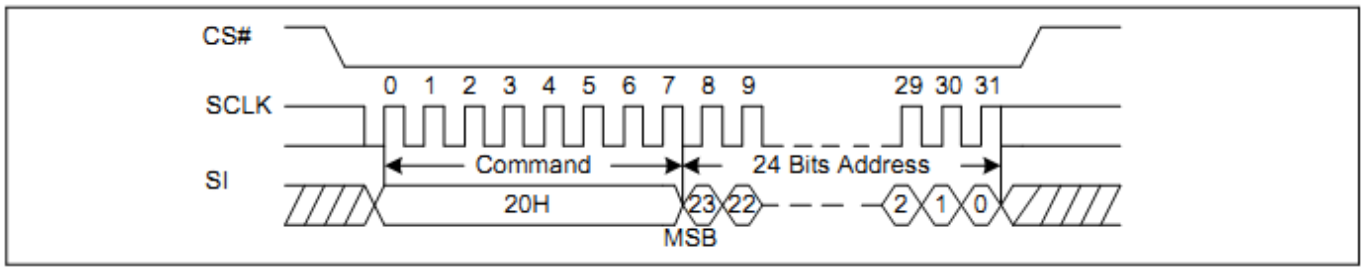


Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low sending Sector Erase command 3-byte address on SI CS# goes high. The command sequence is shown in Figure15. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bit (see Table1.0&1.1) is not executed.

Figure15. Sector Erase Sequence Diagram

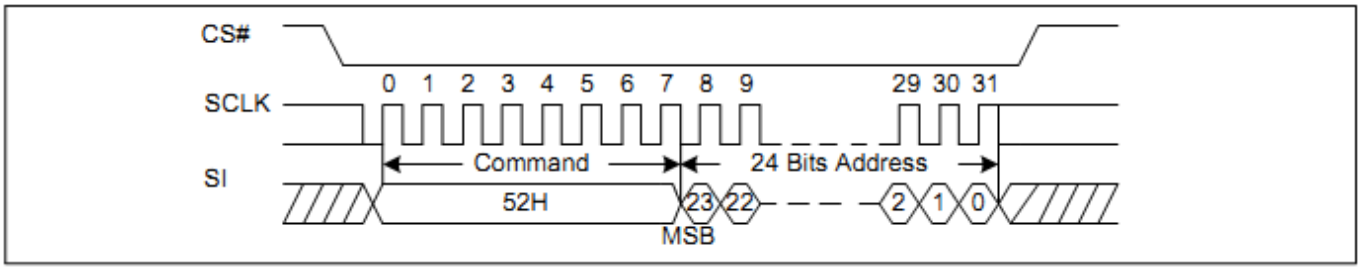


32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low sending 32KB Block Erase command 3-byte address on SI CS# goes high. The command sequence is shown in Figure16. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see Table1.0&1.1) is not executed.

Figure 16. 32KB Block Erase Sequence Diagram

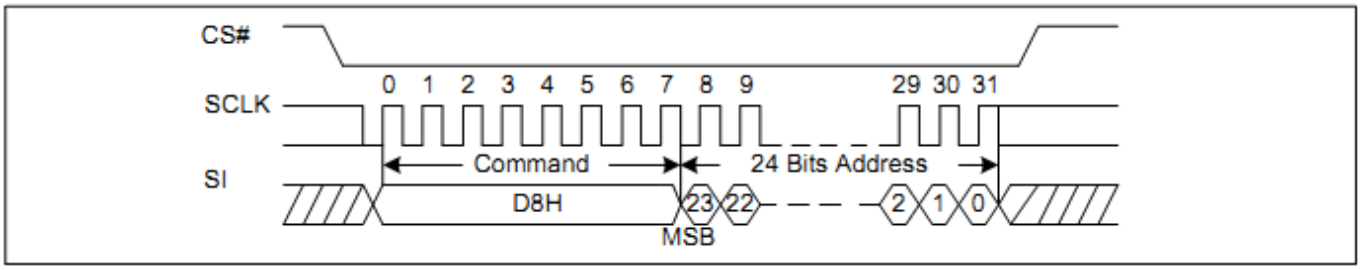


64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low sending 64KB Block Erase command 3-byte address on SI CS# goes high. The command sequence is shown in Figure17. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see Table1.0&1.1) is not executed.

Figure17. 64KB Block Erase Sequence Diagram

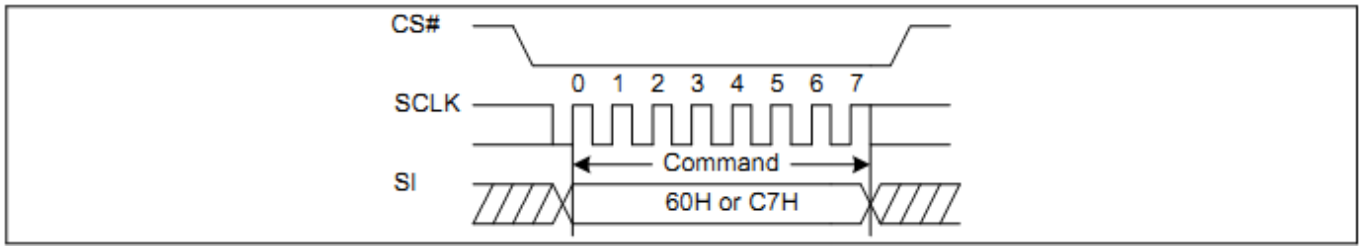


Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low sending Chip Erase command CS# goes high. The command sequence is shown in Figure18. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed only if the Block Protect (BP2, BP1, BP0) bits are “000” when CMP=0, or “110/111” when CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure18. Chip Erase Sequence Diagram



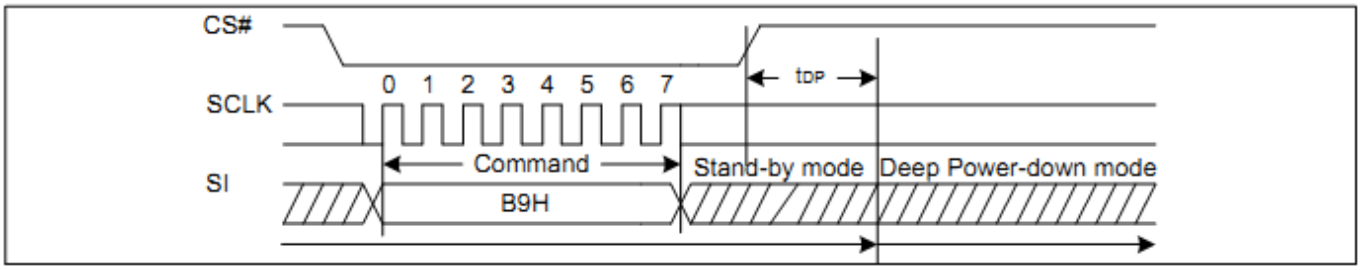
Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low sending Deep Power-Down command CS# goes high. The command sequence is shown in Figure19. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure19. Deep Power-Down Sequence Diagram



Release from Deep Power-Down And Read Device ID (RDI) (ABH)

The Release from Power-Down or Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure20. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure20. The Device ID value for the ACE25C800G is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure20, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 20. Release Power-Down Sequence Diagram

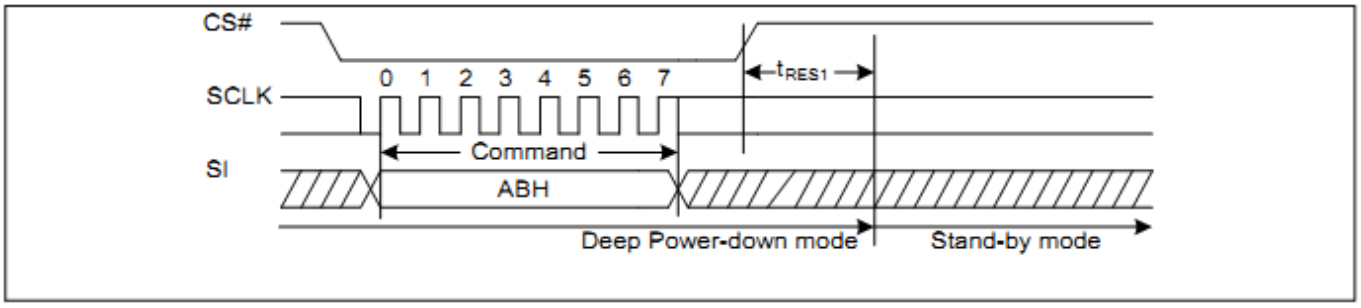
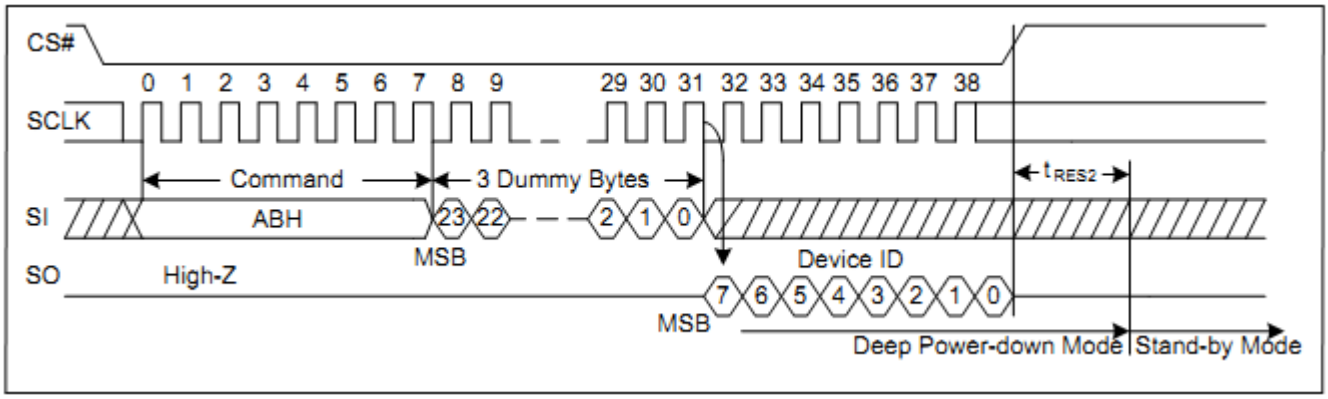


Figure21. Release Power-Down/Read Device ID Sequence Diagram

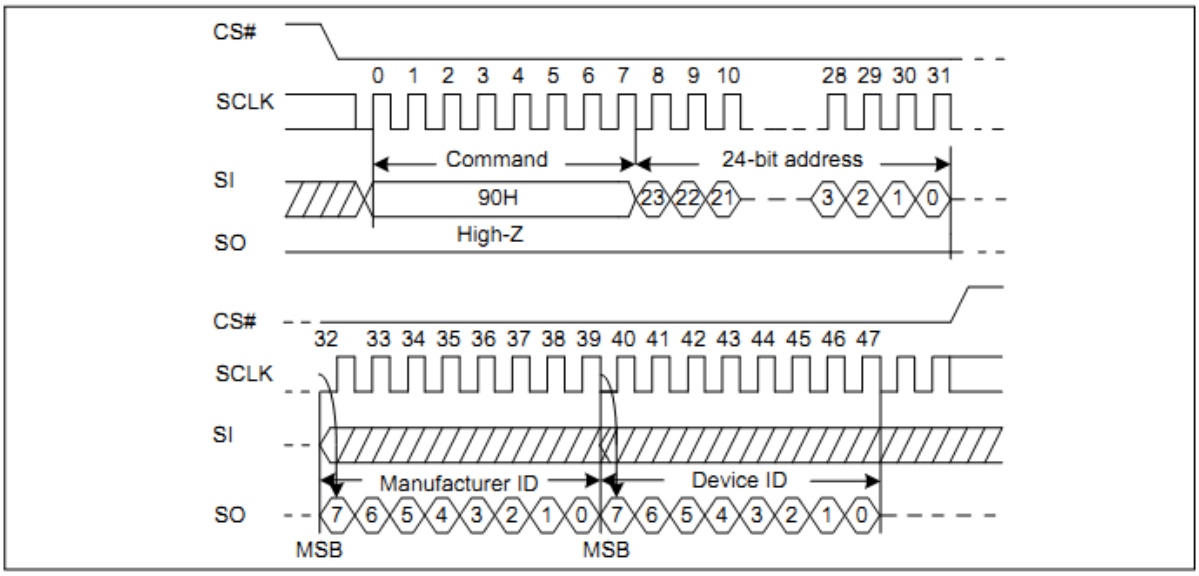


Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/ Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure22. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 22. Read Manufacture ID/ Device ID Sequence Diagram

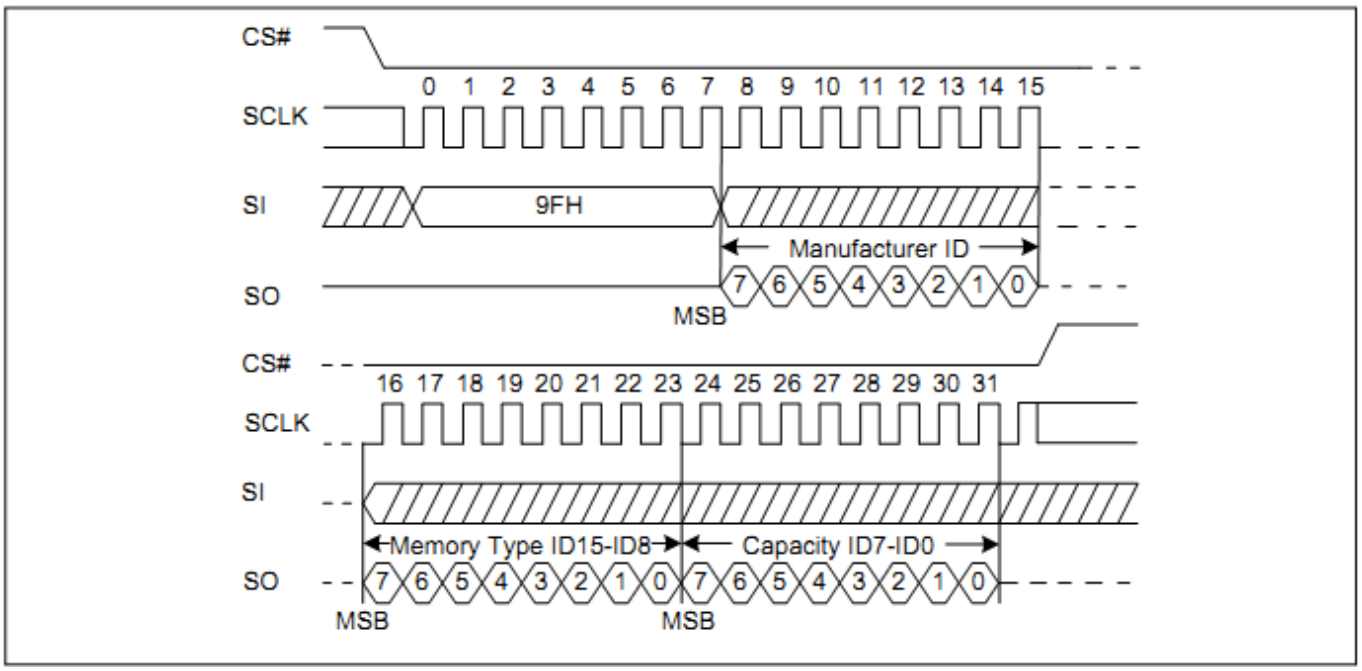


Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure23. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 23. Read Identification ID Sequence Diagram

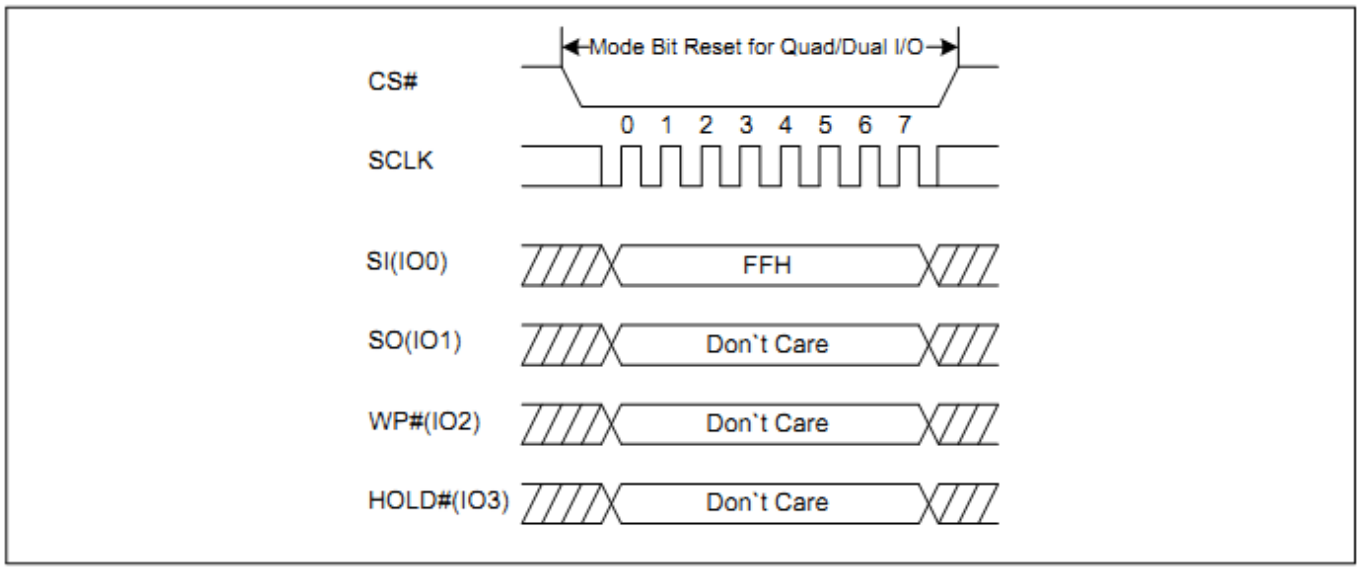


Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

Because the ACE25C800G has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the ACE25C800G will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is show in Figure24.

Figure24. Continuous Read Mode Reset Sequence Diagram



Erase Security Registers (44H)

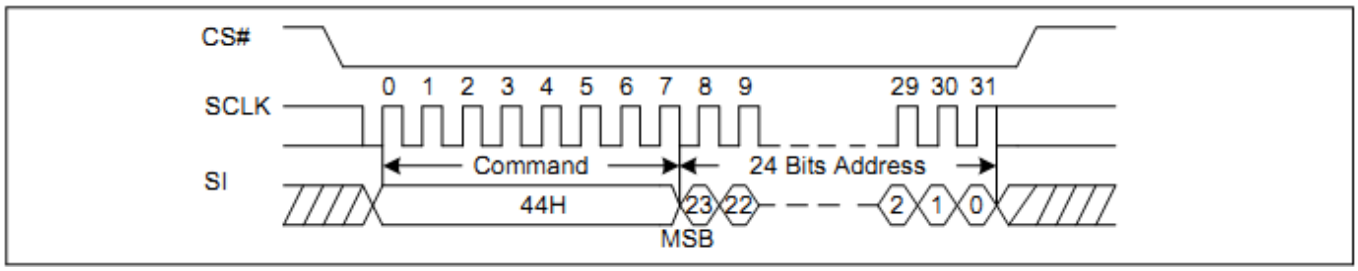
The ACE25C800G provides four 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low sending Erase Security Registers command CS# goes high. The command sequence is shown in Figure33. CS# must be driven high after the eighth bit of the command code has been latched in otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 1	00H	01H	Don't Care
Security Registers 2	00H	02H	Don't Care
Security Registers 3	00H	03H	Don't Care

Figure 33. Erase Security Registers command Sequence Diagram



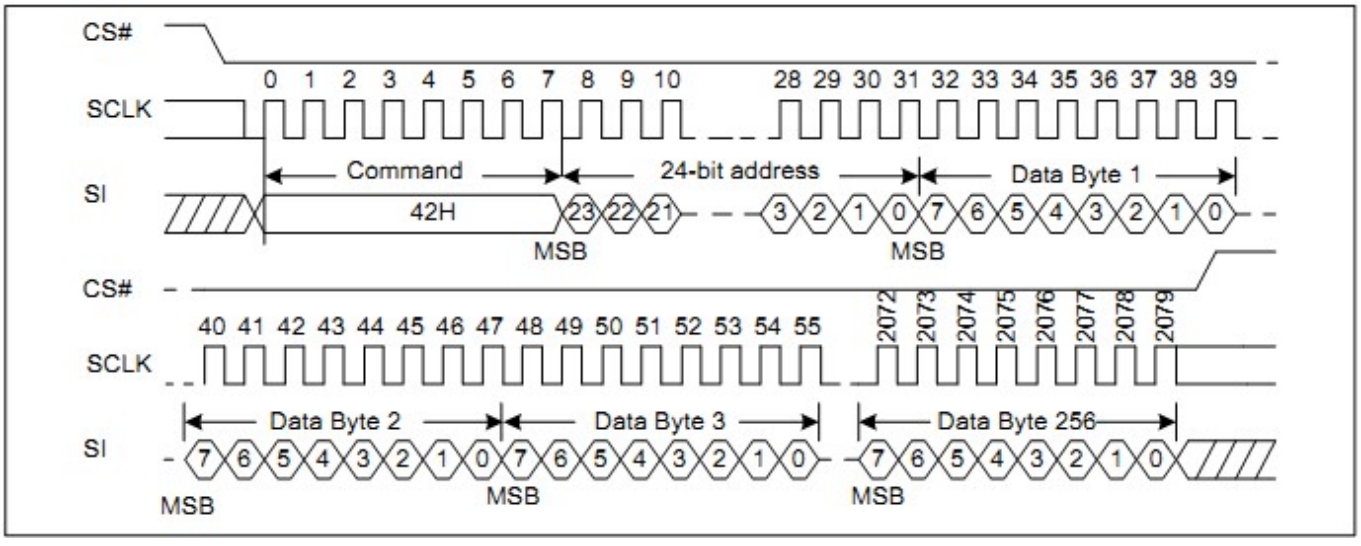
Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

Figure25. Program Security Registers command Sequence Diagram

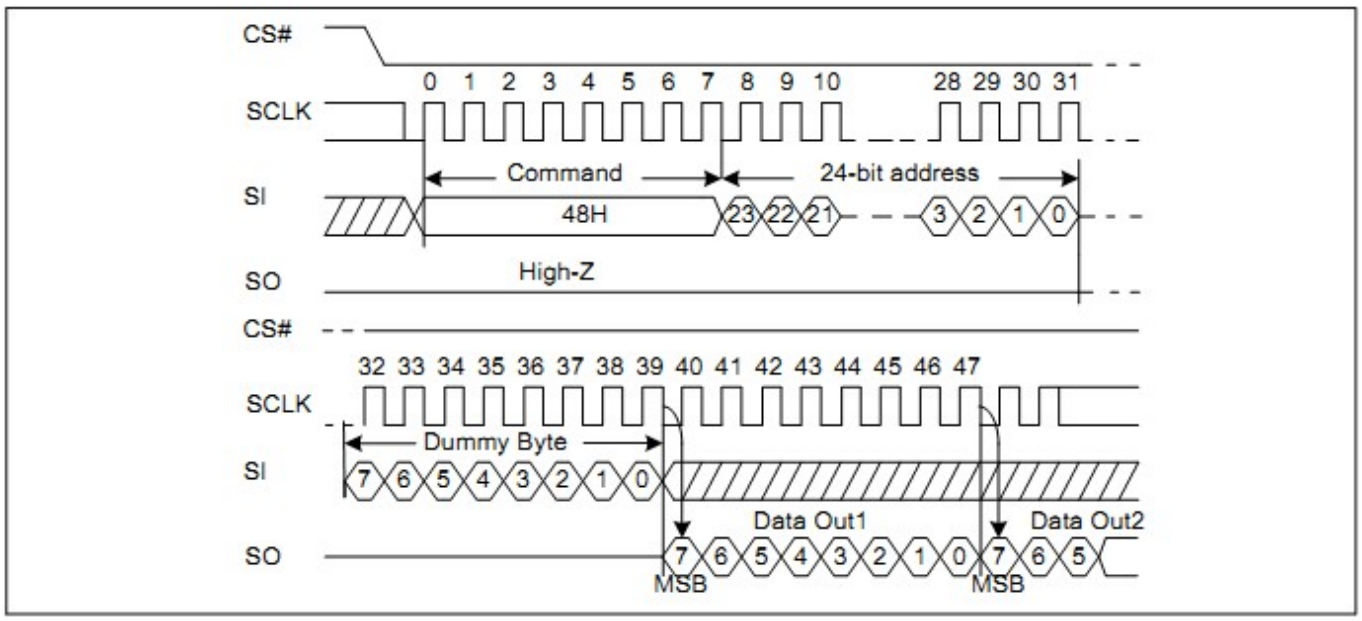


Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A8	A7-A0
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

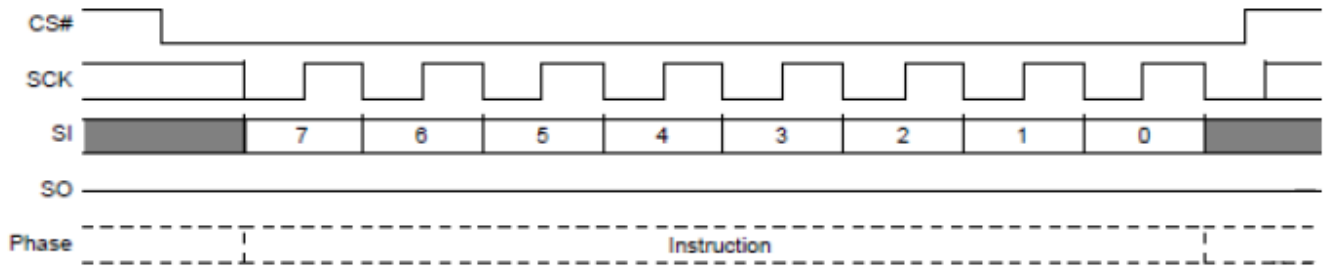
Figure26. Read Security Registers command Sequence Diagram



Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described on page 40 can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued prior to each Write Status Registers (01h) command. Write Enable for Volatile Status Register command (Figure 28) will not set the Write Enable Latch (WEL) bit, it is only valid for the next following Write Status Registers command, to change the volatile Status Register bit values.

Figure27. Write Enable for Volatile Status Register



Power – On Timing

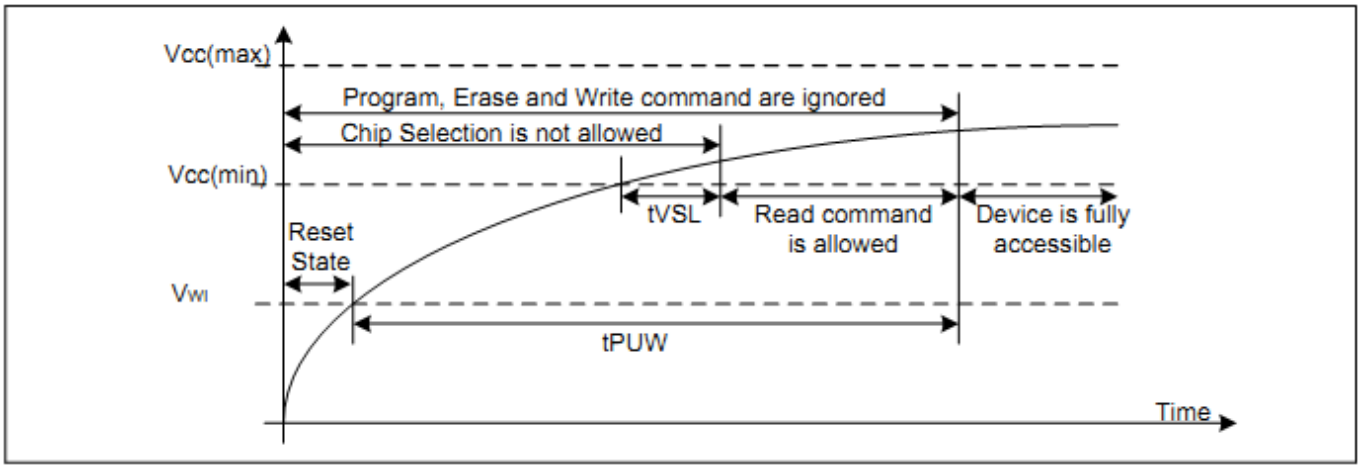


Table3. Power-Up Timing And Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	10		us
tPUW	Time Delay From VCC(min) To Write Instruction	1	10	ms
VWI	Write Inhibit Voltage VCC(min)	1	2.5	V

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

Data Retention And Endurance

Parameter	Test Condition	Min	Units
Minimum Pattern Data Retention Time	150℃	10	Years
	125℃	20	Years
Erase / Program Endurance	-40 to 85 ℃	100K	Cycles

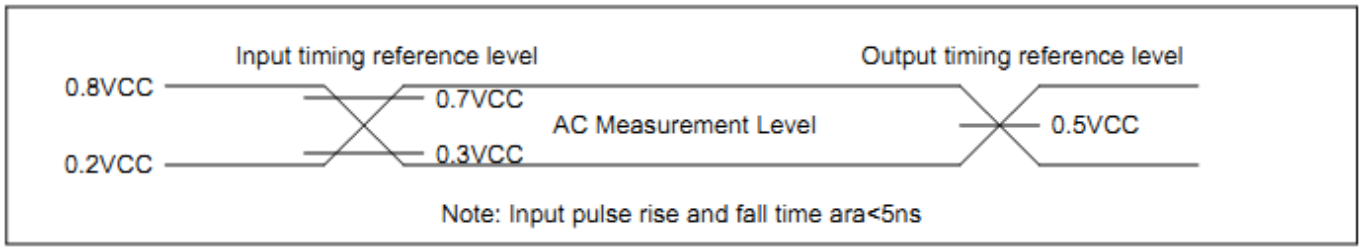
Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Output Short Circuit Current	200	mA
Applied Input / Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

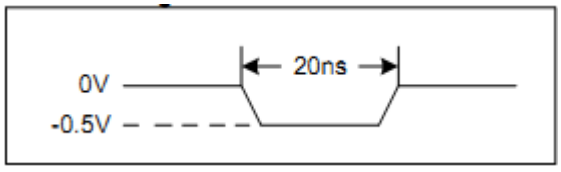
Figure28. Input Test Waveform And Measurement Level



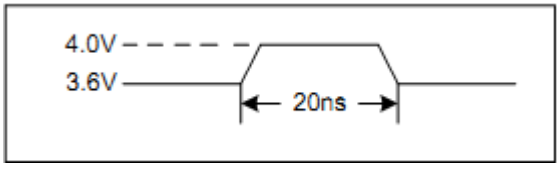
Capacitance Measurement Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pause Voltage	0.2VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



Dc Characteristic

(T=-40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	CS#=VCC, VIN=VCC or VSS		13	25	μA
ICC2	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		2	5	μA
ICC3	Current: Read Single/Dual/Quad 1MHz	SCLK=0.1VCC/ 0.9VCC(1)		3/4/5	3.5/5/6	mA
	Current: Read Single/Dual/ Quad 33MHz			5/11/19	7.5/12/19.5	
	Current: Read Single/Dual/ Quad 50MHz			6.5/16/30	9.5/17/33	
	Current: Read Single/Dual/ Quad 108MHz			10/33/60	12/35/65	
ICC4	Operating Current (PP)	CS#=VCC			15	mA
ICC5	Operating Current(WRSR)	CS#=VCC			5	mA
ICC6	Operating Current (SE)	CS#=VCC			20	mA
ICC7	Operating Current (BE)	CS#=VCC			20	mA
ICC8	Operating Current (CE)	CS#=VCC			20	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL=100μA			0.4	V
VOH	Output High Voltage	IOH=-100μA	VCC-0.2			V

Note: ICC3 is measured with ATE loading

AC Characteristics

(T=-40℃~85℃, VCC=2.7~3.6V, CL=30pf)

Symbol	Parameter	Min	Typ	Max	Unit
fC	Serial Clock Frequency For: FAST_READ(0BH), Dual Output(3BH)	DC.		108	MHz
fC1	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O(EBH), Quad Output(6BH)	DC.		108	MHz
fR	Serial Clock Frequency For: Read(03H)	DC.		55	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1(2)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1(2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# No Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time（read/write）	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5			ns
tHHCH	Hold# High Setup Time (relative to Clock)	5			ns
tCHHL	Hold# High Hold Time (relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			6	ns
tHHQX	Hold# Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid			7	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			0.1	μs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			3	μs
tRES2	CS# High To Standby Mode With Electronic Signature Read			1.5	μs
tSUS	CS# High To Next Command After Suspend			2	us
tW	Write Status Register Cycle Time		2	15(1)	ms
tPP	Page Programming Time		0.7	2.4	ms
tSE	Sector Erase Time		100	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.2/0.4	1/1.2	s
tCE	Chip Erase Time(ACE25C800G)		8	20	s

Note: 1. tW can be up to 45ms at -40□ during the characterization of the current design. It will be improved in the future design.

2. Tested with clock frequency less than 50MHz.

Figure29. Serial Input Timing

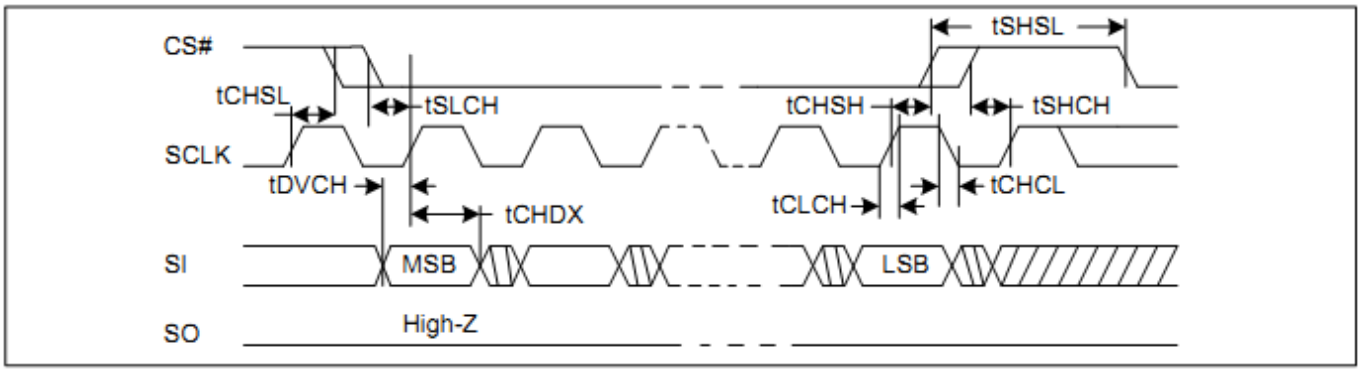


Figure30. Output Timing

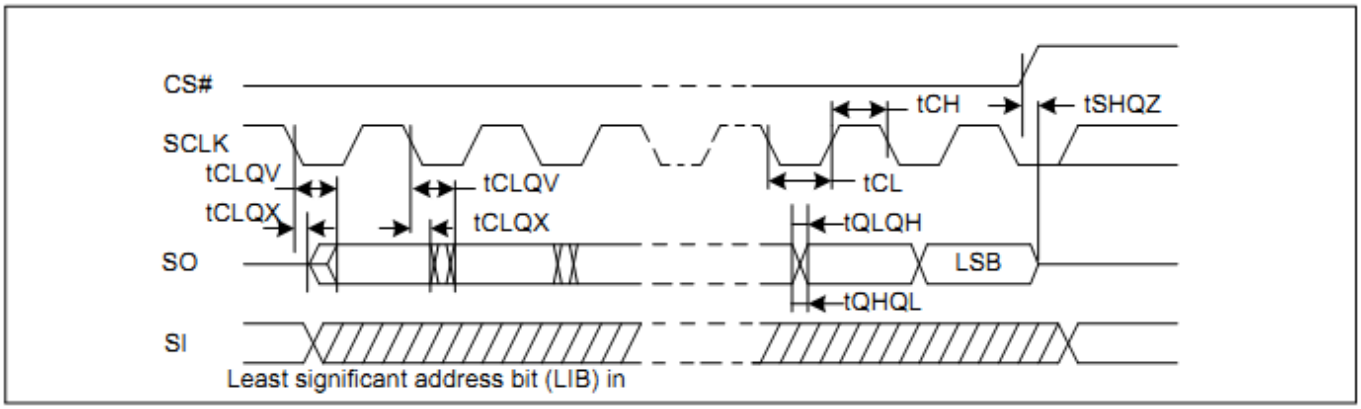
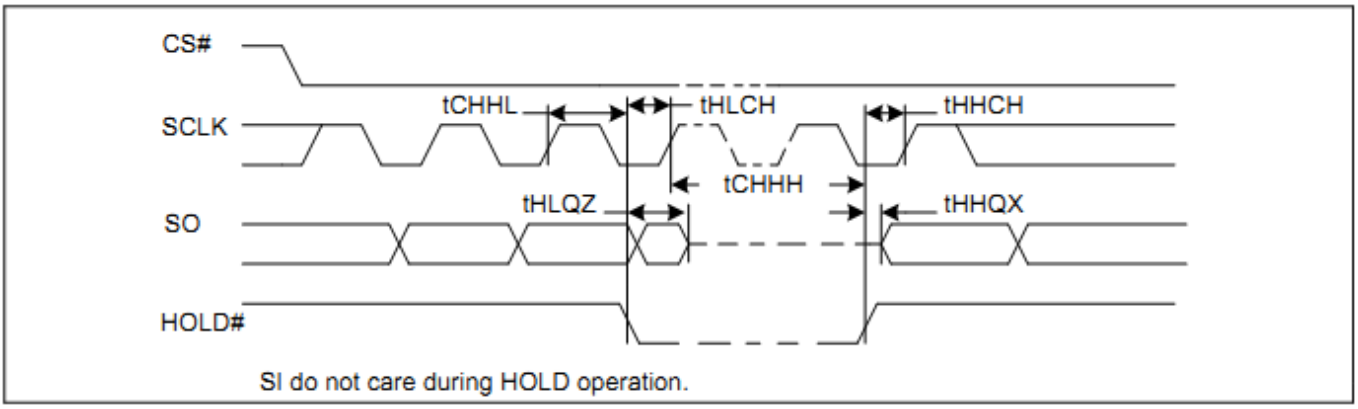
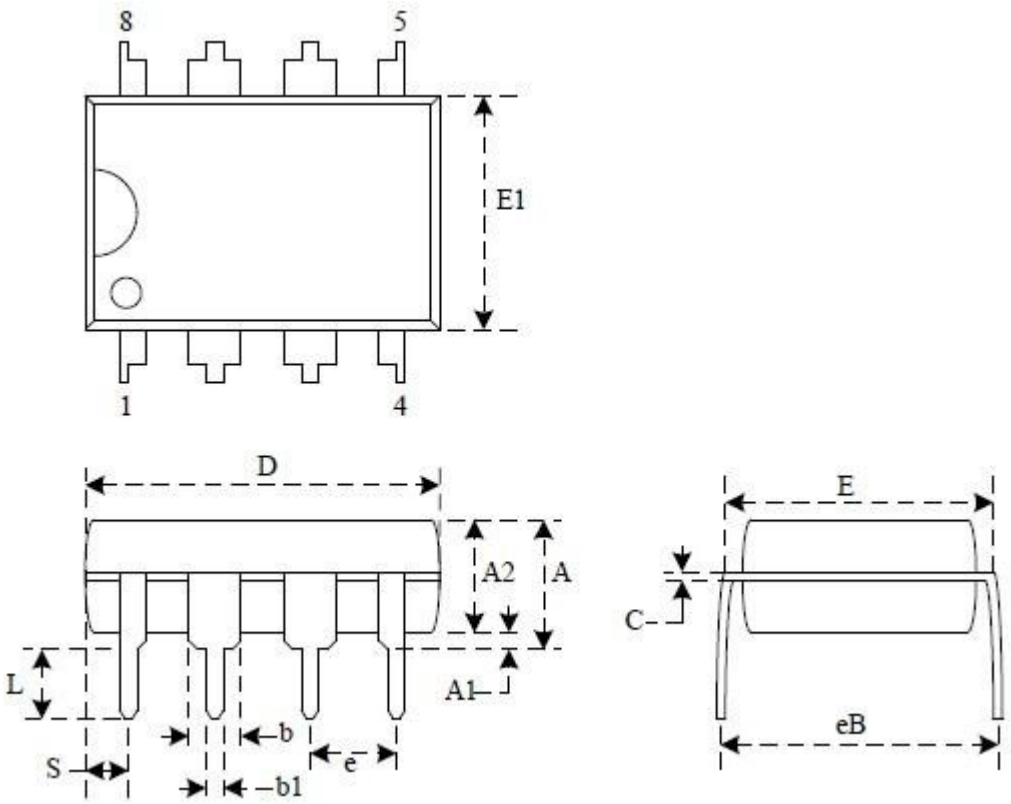


Figure31. Hold Timing



Packaging information

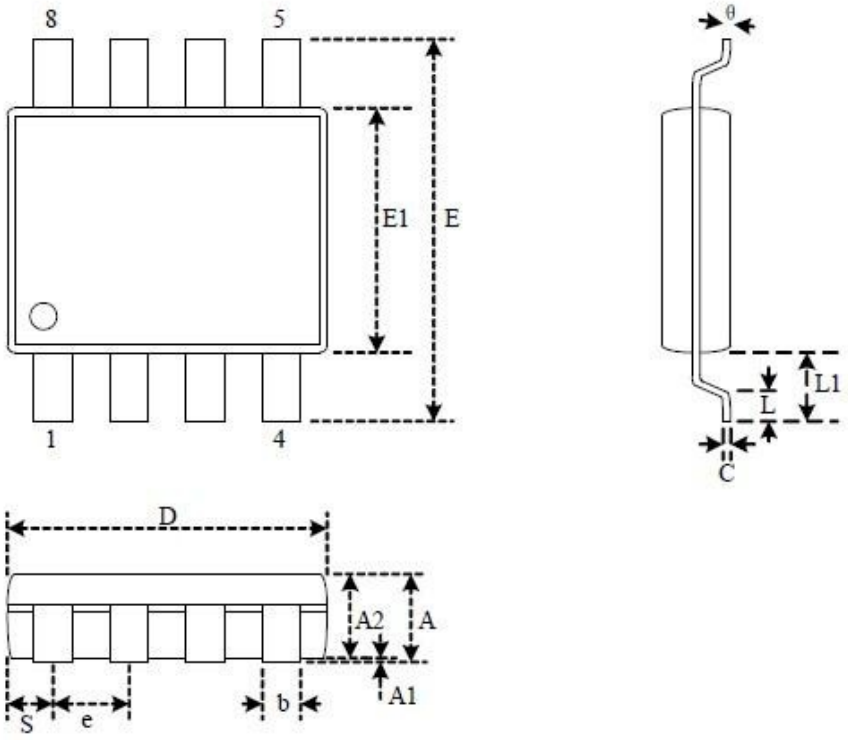
DIP-8



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A			5.33			0.21
A1	0.38			0.015		
A2	3.18	3.30	3.43	0.125	0.130	0.135
b	0.36	0.46	0.56	0.014	0.018	0.022
b1	1.14	1.52	1.78	0.045	0.060	0.070
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.800
E	7.62	7.87	8.13	0.300	0.310	0.320
E1	6.22	6.35	6.48	0.245	0.250	0.255
e		2.54			0.10	
eB	7.87	8.89	9.53	0.310	0.350	0.375
SL	2.92	3.30	3.81	0.115	0.130	0.15
S	0.76	1.14	1.52	0.030	0.045	0.060

Packaging information

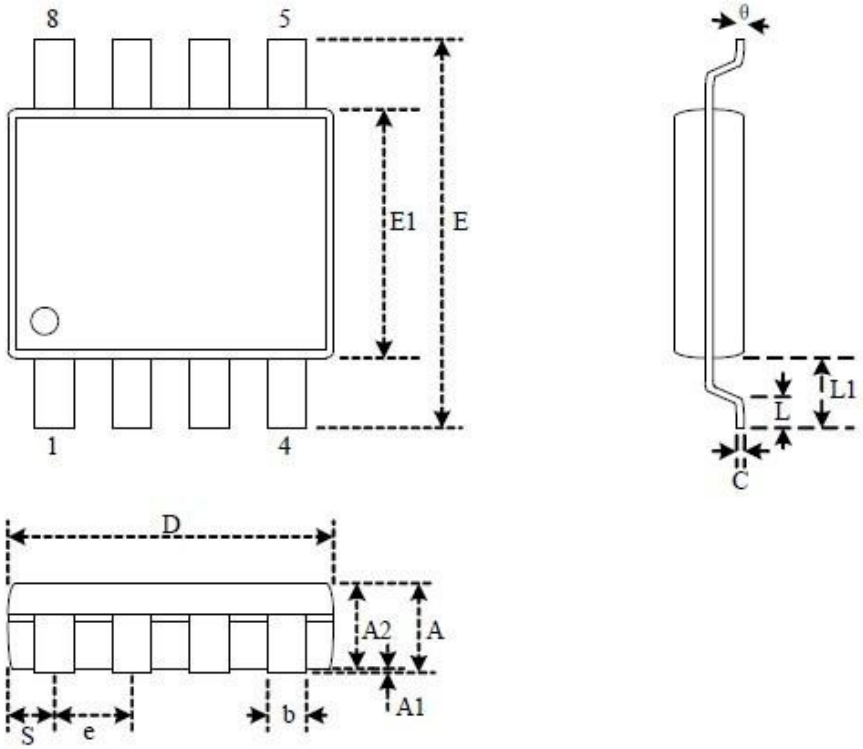
SOP-8 (150mil)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A			1.75			0.069
A1	0.10	0.15	0.20	0.004	0.006	0.008
A2	1.35	1.45	1.55	0.053	0.057	0.061
b	0.36	0.41	0.51	0.014	0.016	0.020
C	0.15	0.20	0.25	0.006	0.008	0.010
D	4.77	4.90	5.03	0.188	0.193	0.198
E	5.80	5.99	6.2	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.158
e		1.27			0.050	
L	0.46	0.66	0.86	0.018	0.026	0.034
L1	0.85	1.05	1.25	0.033	0.041	0.049
S	0.41	0.54	0.67	0.016	0.021	0.026
Θ	0	5	8	0	5	8

Packaging information

SOP-8 (208mil)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A			2.16			0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.36	0.41	0.51	0.014	0.016	0.020
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.13	5.23	5.33	0.202	0.206	0.210
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e		1.27			0.050	
L	0.50	0.65	0.80	0.020	0.026	0.031
L1	1.21	1.31	1.41	0.048	0.052	0.056
S	0.62	0.74	0.88	0.024	0.029	0.035
Θ	0	5	8	0	5	8

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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