ACE25Q512G

512K BIT SPI NOR FLASH Memory Series

Description

The ACE25Q512G is 512K-bit Serial Peripheral Interface(SPI) Flash memory, and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (/WP), and I/O3 (/HOLD). The Dual I/O data is transferred with speed of 216Mbits/s and the Quad I/O & Quad output data is transferred with speed of 432Mbits/s. The device uses a single low voltage power supply, ranging from 2.7 Volt to 3.6 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID and three 256-bytes Security Registers.

Features

- **Serial Peripheral Interface (SPI)**

- Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
- Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
- Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3

- **Read**

- Normal Read (Serial): 50MHz clock rate
- Fast Read (Serial): 108MHz clock rate
- Dual/Quad (Multi-I/O) Read: 108MHz clock rate

- Program

- Serial-input Page Program up to 256bytes

- **Erase**

- Block erase (64/32 KB)
- Sector erase (4 KB)
- Chip erase
- Erase Suspend and Resume

- **Program/Erase Speed**

- Page Program time: 0.7ms typical
- Sector Erase time: 60ms typical
- Block Erase time: 0.3/0.5s typical
- Chip Erase time: 0.5s typical

- **Low Power Consumption**

- 20mA maximum active current
- 5uA maximum power down current

- **Software/Hardware Write Protection**

- 3x256-Byte Security Registers with OTP Lock
- Enable/Disable protection with WP Pin
- Write protect all/portion of memory via software
- Top or Bottom, Sector or Block selection

- **Single Supply Voltage**

- Full voltage range: 2.7~3.6V

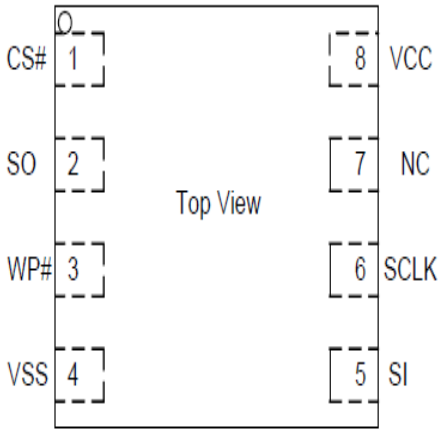
- **Temperature Range**

- Industrial (-40℃ to +85℃)

- **Cycling Endurance/Data Retention**

- Typical 100k Program-Erase cycles on any sector
- Typical 20-year data retention at +55℃

Packaging Type

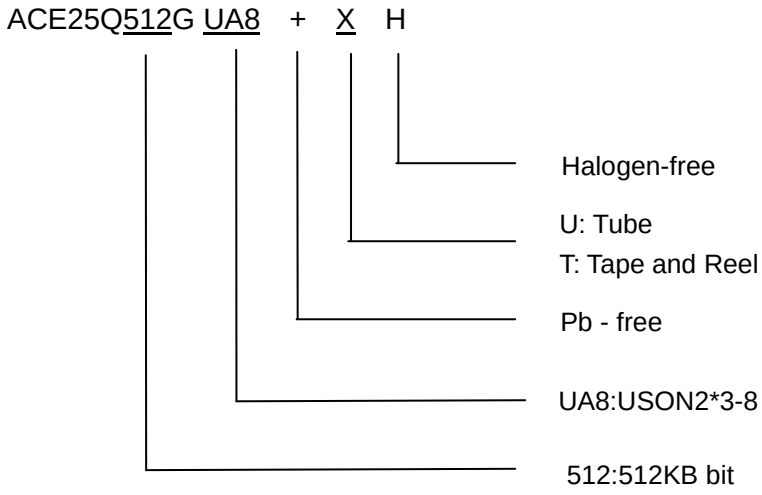


Signal Names

Table 1

Pin No	Pin Name	I/O	Function
1	/CS	I	Chip Select
2	SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual or Quad Instructions.
3	/WP (IO2)	I/O	Write Protect in single bit or Dual data Instructions. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions.
4	VSS		Ground
5	SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual or Quad Instructions.
6	SCLK	I	Serial Clock
7	/HOLD# (IO3)	I/O	Hold (pause) serial transfer in single bit or Dual data Instructions. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions.
8	VCC		Core and/ O Power Supply

Ordering information



Uniform Block Sector Architecture

Table 2 ACE25Q512G Block/Sector Addresses

Memory Density	Block(64kbyte)	Block(32kbyte)	Sector No.	Sector Size(KB)	Address range
512Kbit	Block 0	Half block 0	Sector 0	4	000000h-000FFFh
			Sector 7	4	007000h-007FFFh
		Half block 1	Sector 8	4	008000h-008FFFh
				4	
			Sector 15	4	00F000h-00FFFFh

Notes:

1. Block = Uniform Block, and the size is 64K bytes.
2. Half block = Half Uniform Block, and the size is 32k bytes.
3. Sector = Uniform Sector, and the size is 4K bytes.

Device Operation

Standard SPI Instructions

The ACE25Q512G features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI Instructions

The ACE25Q512G supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI Instructions

The ACE25Q512G supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read” (6BH, EBH) instructions. These instructions allow data to be transferred t-o or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.PI Mode

Operation Features

Supply Voltage

Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see operating ranges of page 35). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10nF to 100nF) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in operating ranges of page 35).

When VCC has passed the POR threshold, the device is reset.

Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

Hold Condition

The Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in Figure 1)

The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. Also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Figure 1 Hold condition activation

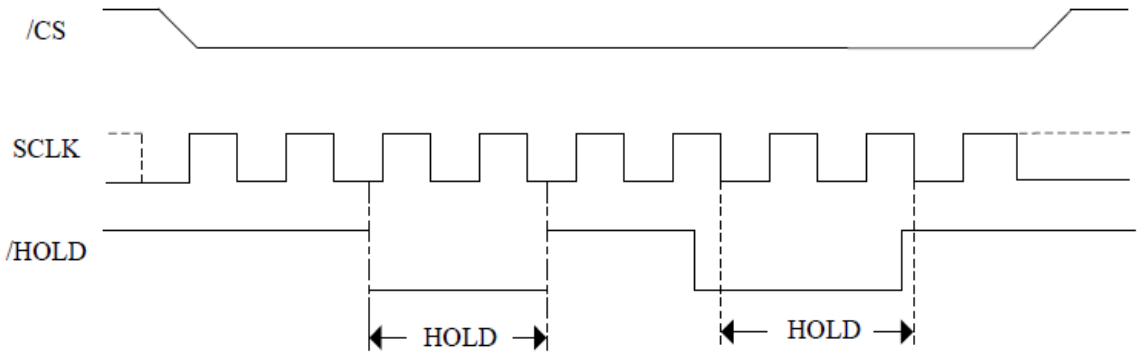


Figure 1

Status Register

Status Register Table

See Table 3 and Table 4 for detail description of the Status Register bits. Status Register-2 (SR2) and Status Register-1 (SR1) can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection, Quad SPI setting, Security Register lock status, and Erase/Program Suspend status.

Table 3 Status Register-2 (SR2)

BIT	Name	Function	Default Value	Description
7	SUS	Suspend Status	0	0 = Erase/Program not suspended 1 = Erase/Program suspended
6	Reserved	Reserved	0	
5	LB3	Security Register	0	OTP Lock Bits 3:1 for Security Registers 3:1 0 = Security Register not protected
4	LB2		0	
3	LB1		0	
2	Reserved		0	
1	QE		0	0 = Quad Mode Not Enabled, the /WP pin and /HOLD are enabled. 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled
0	SRP1		0	0 = SRP0 selects whether /WP input has effect on protection of the status register 1 = SRP0 selects Power Supply Lock Down or OTP Lock Down mode

Table 4 Status Register-1 (SR1)

BIT	Name	Function	Default Value	Description
7	SRP0	Status Resister Protect 0	0	0 = /WP input has no effect or Power Supply Lock Down mode 1 = /WP input can protect the Status Register or OTP Lock Down
6	SEC	Sector/Block Protect	0	0 = BP2-BP0 protect 64KB blocks 1 = BP2-BP0 protect 4KB sectors
5	TB	Top/Bottom Protect	0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up
4	BP2	Block Protect Bits	0	000b = No protection See Table 6 for protection ranges
3	BP1		0	
2	BP0		0	
1	WEL	Write Enable Latch	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	WIP	Write in Progress Status	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

The Status and Control Bits

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

SEC, TB, BP2, BP1, BP0 bits

The Block Protect (SEC, TB, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When the Block Protect (SEC, TB, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 6).becomes protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (SEC, TB, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply or ground).

LB3/LB2/LB1 bit

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the 256byte Security Registers will become read-only permanently, LB3/2/1 for Security Registers 3:1.

SUS bit

The SUS bit is a read only bit in the status register2 (bit7) that is set to 1 after executing an Erase/Program Suspend (75H) instruction. The SUS bit is cleared to 0 by Erase/Program Resume (7AH) instruction as well as a power-down, power-up cycle.

Status Register Protect Table

Table5

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written To again until the next Power-Down,Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and not be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact ACE for details.

Write Protect Features

1. Software Protection: The Block Protect (SEC, TB, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
2. Hardware Protection: /WP going low to protected the BP0~SEC bits and SRP0~1 bits.
3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.
4. Write Enable: The Write Enable Latch (WEL) bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction.

Status Register Memory Protection

Protect Table

Table 6 ACE25Q512G Status Register Memory Protection

Status Register Content					Memory Content			
SEC	TB	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	X	X	0	0	NONE	NONE	NONE	NONE
0	X	X	0	1	0	000000H-00FFFFH	64KB	ALL
0	X	X	1	X	0	000000H-00FFFFH	64KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	0	00F000H-00FFFFH	4KB	Top Block
1	0	0	1	0	0	00E000H-00FFFFH	8KB	Top Block
1	0	0	1	1	0	00C000H-00FFFFH	16KB	Top Block
1	0	1	0	X	0	008000H-00FFFFH	32KB	Top Block
1	0	1	1	0	0	008000H-00FFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block
1	X	1	1	1	0	000000H-00FFFFH	64KB	ALL

Device Identification

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 7 ACE25Q512G ID Definition table

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	E0	40	10
90H	E0		05
ABH			05

Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 8, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must driven high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Instruction Set Table

Table 8

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Write Enable	06H					
Write Disable	04H					
Read Status Register-1	05H	(S7-S0)				
Read Status Register-2	35H	(S15-S8)				
Write Enable for Volatile Status	50H					
Write Status Register	01H	(S7-S0)	(S15-S8)			
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)		
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	dummy	(D7-D0)(5)		
Set Burst with Wrap	77h	dummy	dummy	dummy	W8-W0	
Continuous Read Reset	FFH	FFH				
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte
Sector Erase	20H	A23-A16	A15-A8	A7-A0		
Block Erase(32K)	52H	A23-A16	A15-A8	A7-A0		
Block Erase(64K)	D8H	A23-A16	A15-A8	A7-A0		

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Chip Erase	C7/60H					
Program/Erase Suspend	75H					
Program/Erase Resume	7AH					
Deep Power-Down	B9H					
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	
Release From Deep Power-Down	ABH					
Manufacturer/ Device ID	90H	dummy	dummy	00H	(M7-M0)	(ID7-ID0)
JEDEC ID	9FH	(M7-M0)	(ID15-ID8)	(ID7-ID0)		
Erase Security Registers(6)	44H	A23-A16	A15-A8	A7-A0		
ProgramSecurity Registers(6)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)
Read Security Registers(6)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Enable Reset	7Eh					
Reset Device	99h					

Notes:

1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
2. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3
3. Quad Output Data
   IO0 = (D4, D0,…..)
   IO1 = (D5, D1,…..)
   IO2 = (D6, D2,…..)
   IO3 = (D7, D3,…..)
4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
5. Fast Read Quad I/O Data

   IO0 = (x, x, x, x, D4, D0,…)

   IO1 = (x, x, x, x, D5, D1,…)

   IO2 = (x, x, x, x, D6, D2,…)

   IO3 = (x, x, x, x, D7, D3,…)

6. Security Registers Address:

   Security Register0: A23-A16=00h, A15-A8=00h, A7-A0= Byte Address;

   Security Register1: A23-A16=00h, A15-A8=01h, A7-A0= Byte Address;

   Security Register2: A23-A16=00h, A15-A8=02h, A7-A0= Byte Address;

   Security Register3: A23-A16=00h, A15-A8=03h, A7-A0= Byte Address;

   Security Register 0 can be used to store the Flash Discoverable Parameters,

   The feature is upon special order, please contact ACE for details.

Configuration and Status Instructions

Write Enable (06H)

See Figure 2, the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction /CS goes high.

Figure 2 Write Enable Sequence Diagram

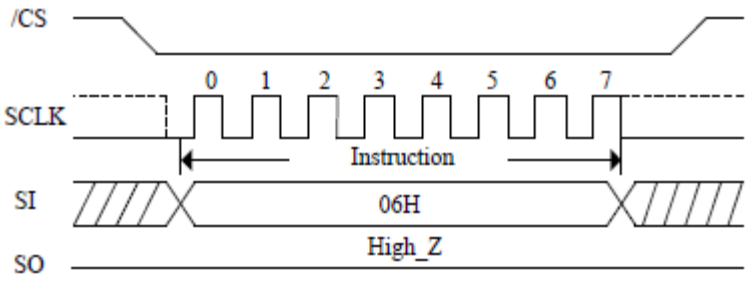


Figure 2

Write Disable (04H)

See Figure 3, the Write Disable instruction is for resetting the Write Enable Latch bit. The Write Disable instruction sequence: /CS goes low sending the Write Disable instruction /CS goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

Figure 3, Write Disable Sequence Diagram

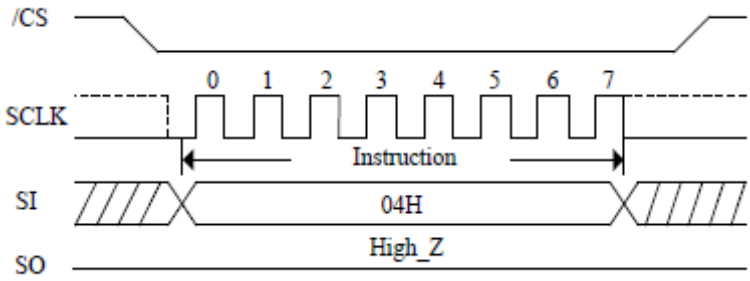


Figure 3

Read Status Register (05H or 35H)

See Figure 4, the Read Status Register (RDSR) instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code “05H”, the SO will output Status Register bits S7~S0. The instruction code “35H”, the SO will output Status Register bits S15~S8.

Figure 4. Read Status Register Sequence Diagram

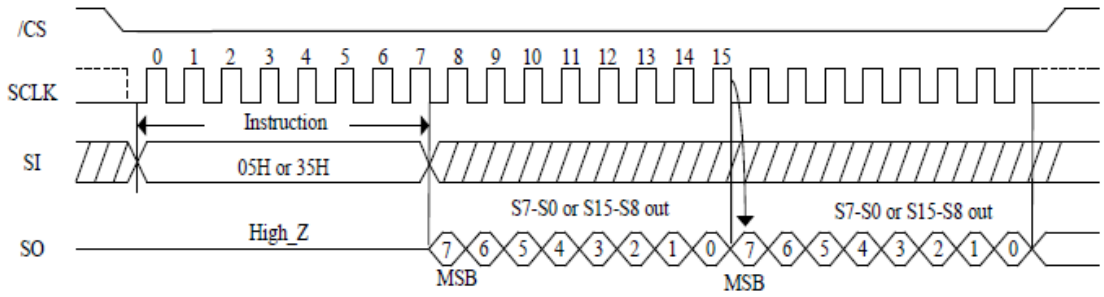


Figure 4

Write Status Register (01H)

See Figure 5, the Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S15, S1 and S0 of the Status Register. /CS must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register instruction is not executed. If /CS is driven high after eighth bit of the data byte, the QE and SRP1 bits will be cleared to 0. As soon as /CS is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (SEC, TB, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3. The Write Status Register instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (/WP) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

Figure 5 Write Status Register Sequence Diagram

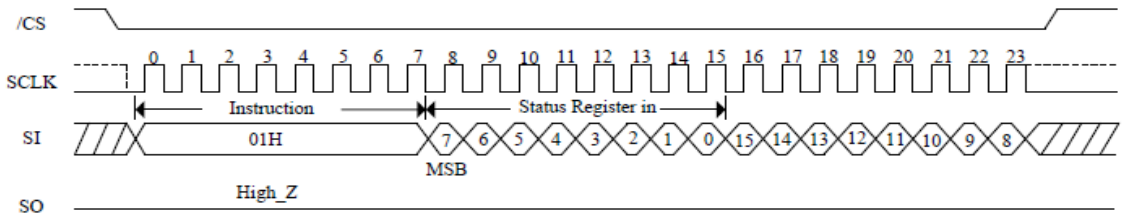


Figure 5

Write Enable for Volatile Status Register (50H)

See Figure 6, the non-volatile Status Register bits can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to each Write Status Registers (01h) instruction. Write Enable for Volatile Status Register instruction will not set the Write Enable Latch bit, it is only valid for the next following Write Status Registers instruction, to change the volatile Status Register bit values.

Figure 6 Write Enable for Volatile Status Register

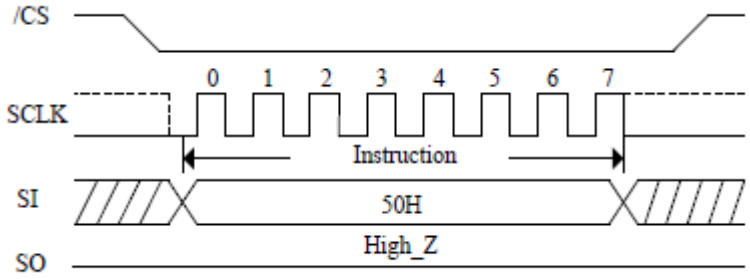


Figure 6

Read Instructions

Read Data (03H)

See Figure 7, the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving /CS high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress. Normal read mode running up to 50MHz.

Figure 7 Read Data Bytes Sequence Diagram

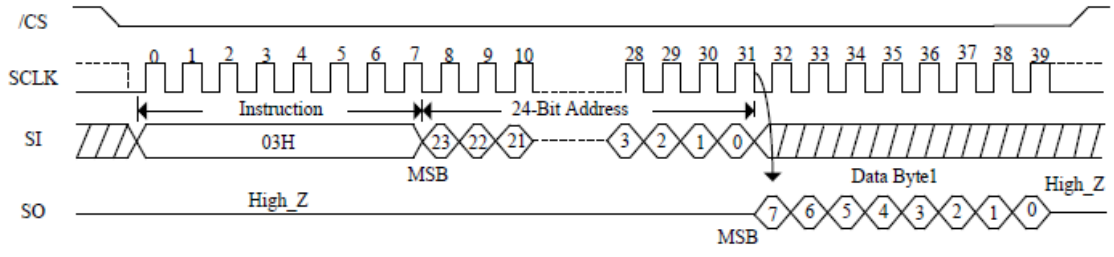


Figure 7

Fast Read (0BH)

See Figure 8, the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 8 Fast Read Sequence Diagram

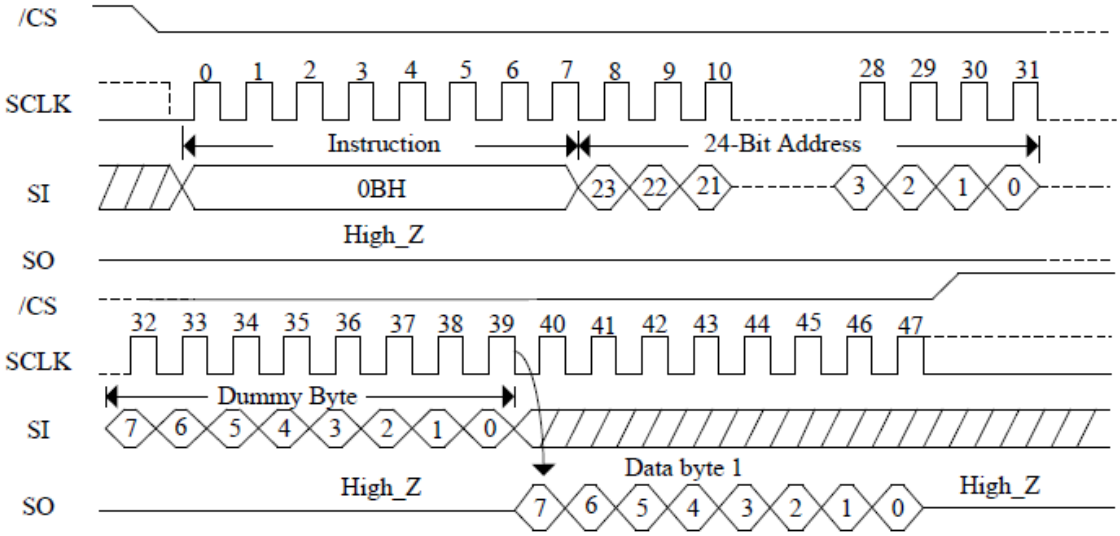


Figure 8

Dual Output Fast Read (3BH)

See Figure 9, the Dual Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 9 Dual Output Fast Read Sequence Diagram

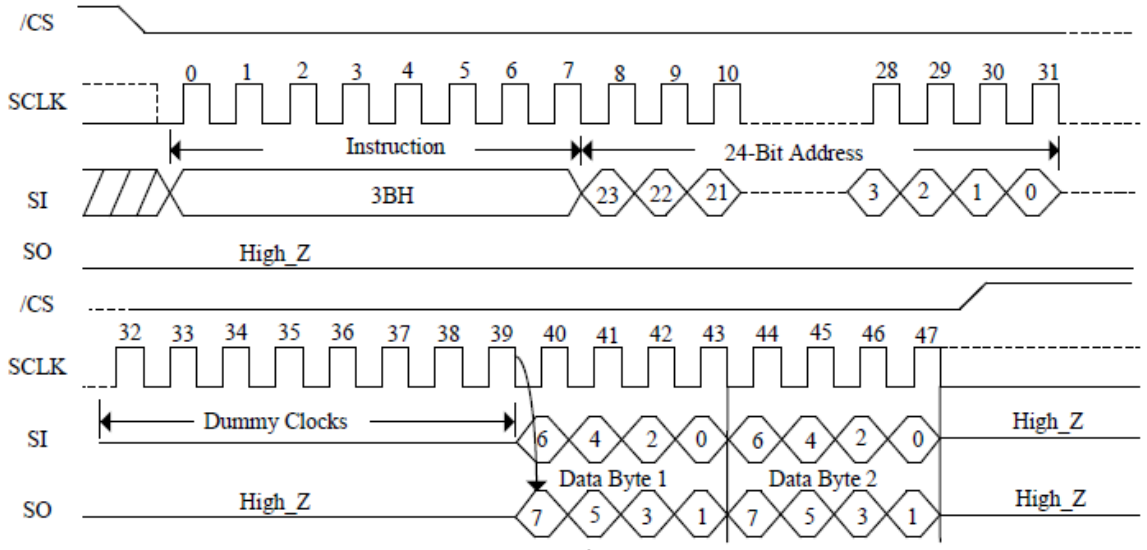


Figure 9

Quad Output Fast Read (6BH)

See Figure 10, the Quad Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 10 Quad Output Fast Read Sequence Diagram

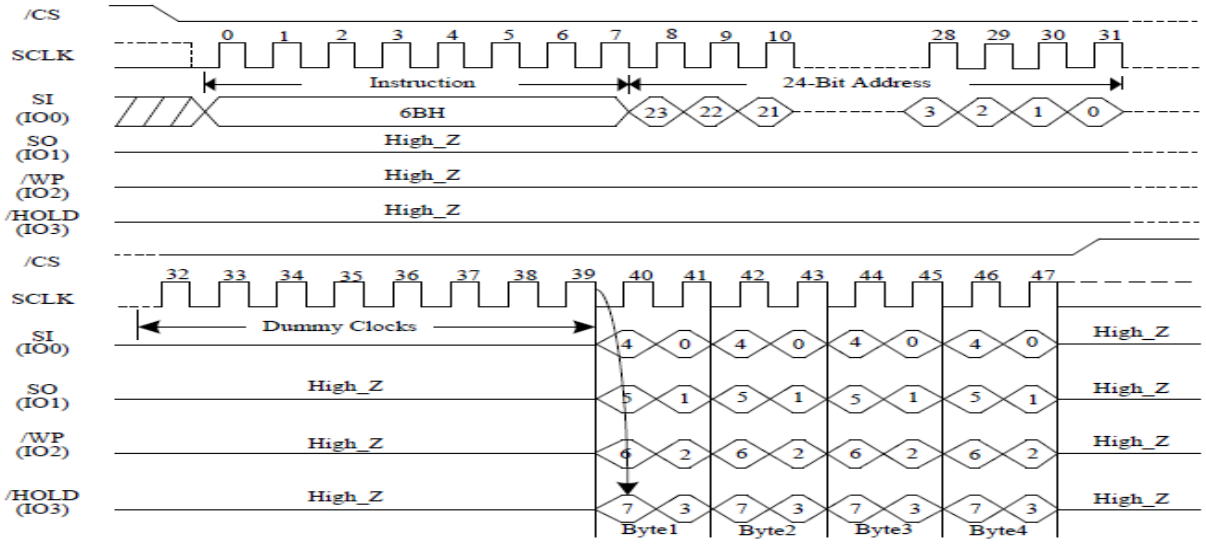


Figure 10

Dual I/O Fast Read (BBH)

See Figure 11, the Dual I/O Fast Read instruction is similar to the Dual Output Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 11 Dual I/O Fast Read Sequence Diagram (Initial command or previous M5-4≠10)

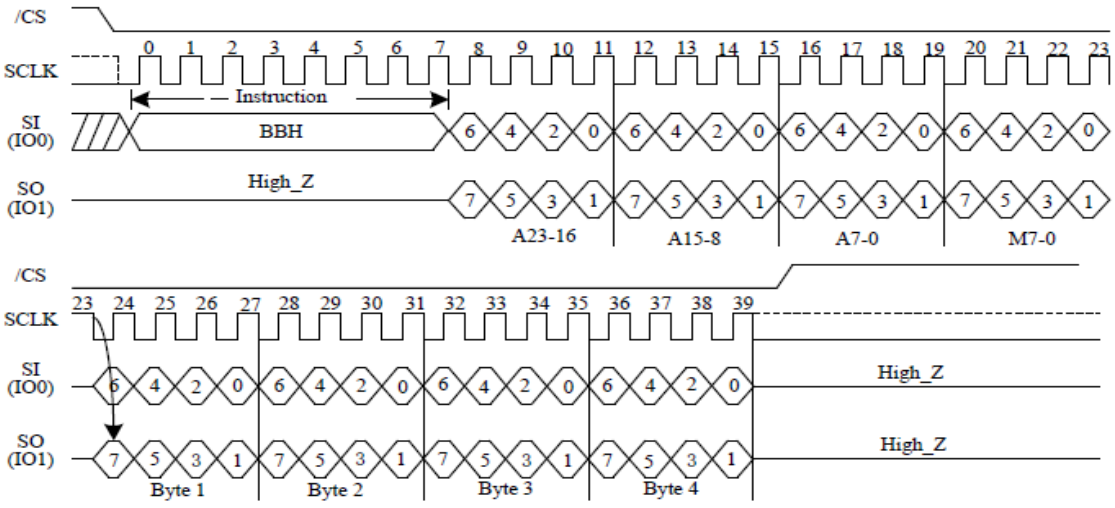


Figure 11

Dual I/O Fast Read with “Continuous Read Mode”

The Fast Read Dual I/O command can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 14. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O command through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. If the “Continuous Read Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O command (after /CS is raised and then lowered) does not require the BBH instruction code, as shown in Figure 12. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next command (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A “Continuous Read Mode” Reset command can also be used to reset (M7-0) before issuing normal commands (see Continuous Read Mode Reset (FFH or FFFFH)).

Figure 12 Dual I/O Fast Read Sequence Diagram (Previous command set M5-4 =10)

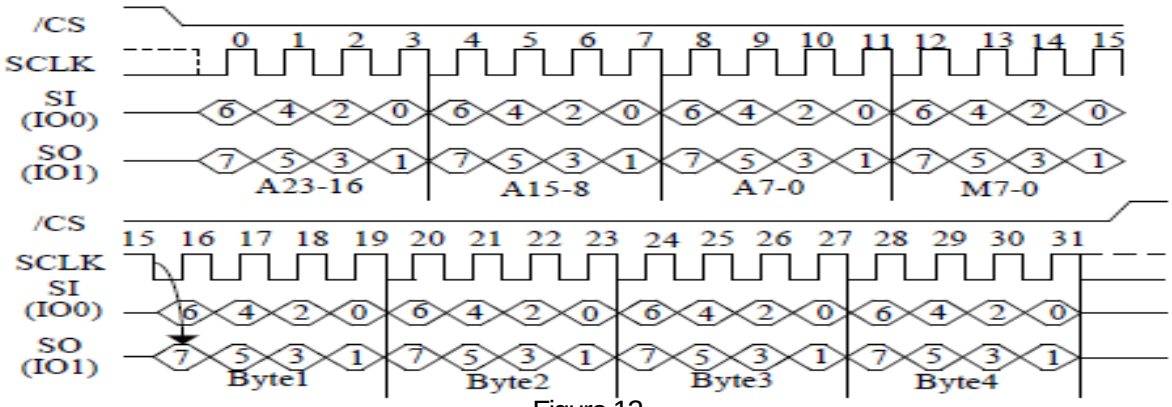


Figure 12

Quad I/O Fast Read (EBH)

See Figure 13, the Quad I/O Fast Read instruction is similar to the Dual I/O Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read instruction.

Figure 13 Quad I/O Fast Read Sequence Diagram (Initial command or previous M5-4≠10)

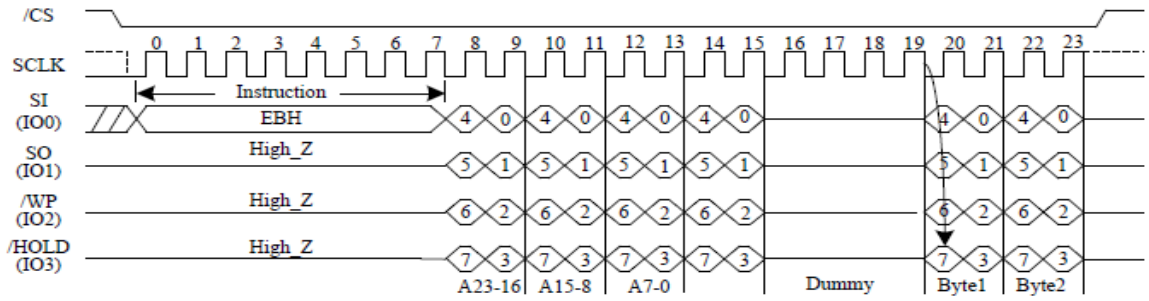


Figure 13

Quad I/O Fast Read with “Continuous Read Mode”

See Figure 14, the Fast Read Quad I/O command can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0), The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. If the “Continuous Read Mode” bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after /CS is raised and then lowered) does not require the EBH instruction code, This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next command (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A “Continuous Read Mode” Reset command can also be used to reset (M7-0) before issuing normal commands (see Continuous Read Mode Reset (FFH or FFFFH)).

Figure 14 Quad I/O Fast Read Sequence Diagram (Previous command set M5-4 =10)

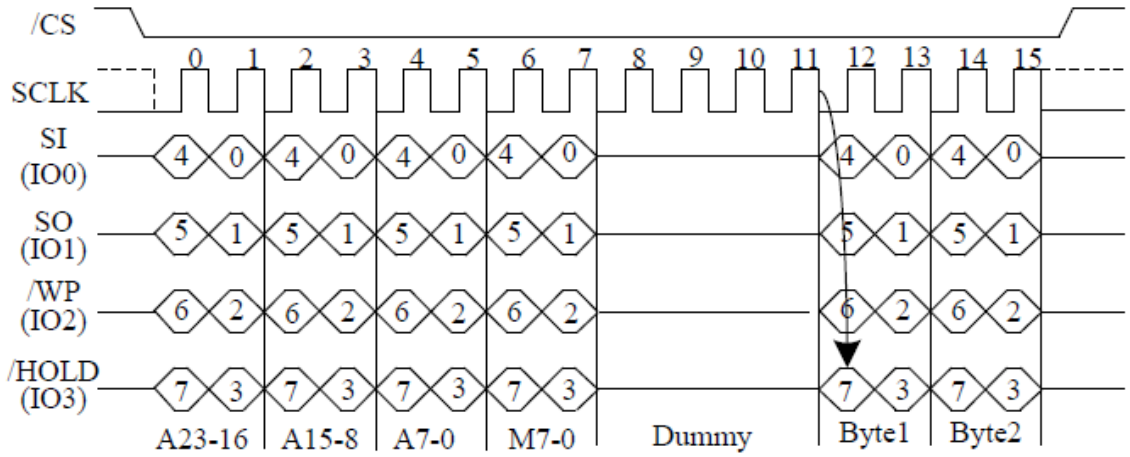


Figure 14

Continuous Read Mode Reset (FFH or FFFFH)

The “Continuous Read Mode” bits are used in conjunction with “Fast Read Dual I/O” and “Fast Read Quad I/O” Instructions to provide the highest random Flash memory access rate with minimum SPI instruction overhead, thus allowing more efficient XIP (execute in place) with this device family.

The “Continuous Read Mode” bits M7-0 are set by the Dual/Quad I/O Read Instructions. M5-4 are used to control whether the 8-bit SPI instruction code (BBH or EBH) is needed or not for the next instruction. When M5-4 = (1,0), the next instruction will be treated the same as the current Dual/Quad I/O Read instruction without needing the 8-bit instruction code; when M5-4 do not equal to (1,0), the device returns to normal SPI instruction mode, in which all instructions can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

Figure 15 the Continuous Read Mode Reset instruction (FFH or FFFFH) can be used to set M4 = 1, thus the device will release the Continuous Read Mode and return to normal SPI operation.

To reset “Continuous Read Mode” during Quad I/O operation, only eight clocks are needed. The instruction is “FFH”. To reset “Continuous Read Mode” during Dual I/O operation, sixteen clocks are needed to shift in instruction “FFFFH

Figure 15 Continuous Read Mode Reset Sequence Diagram

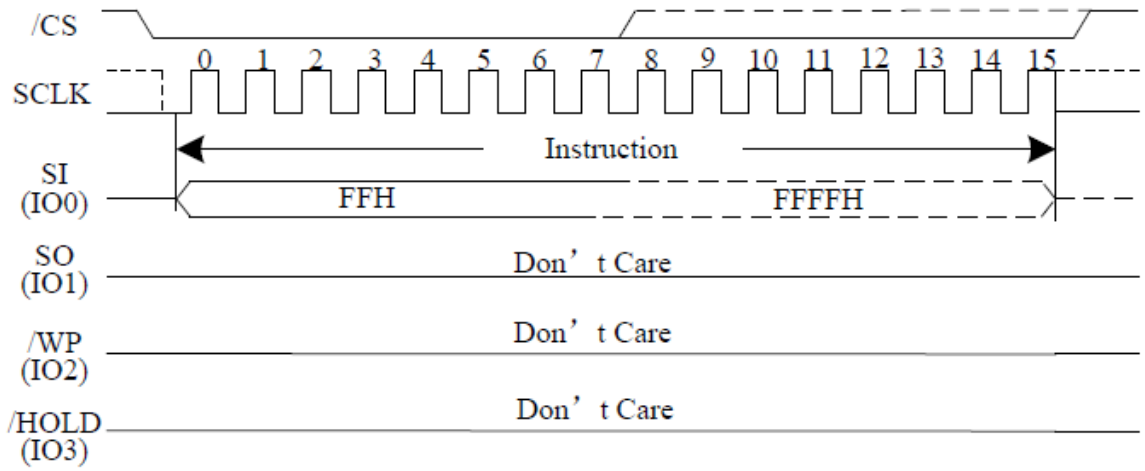


Figure 15

Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around”

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) instruction prior to EBh. The “Set Burst with Wrap” (77h) instruction can either enable or disable the “Wrap Around” feature for the following EBh instructions. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8,16,32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. Wrap bit W7 and the lower nibble W3-0 are not used.

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” and “Word Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4=1. The default value of W4 upon power on is 1.

Table 9

W6	W5	W4 = 0		W4 =1 (DEFAULT)	
		Wrap Around	Wrap Length	Wrap Around	Wrap Length
0	0	Yes	8-byte	No	N/A
0	1	Yes	16-byte	No	N/A
1	0	Yes	32-byte	No	N/A
1	1	Yes	64-byte	No	N/A

Figure 16 Set Burst with Wrap Command Sequence

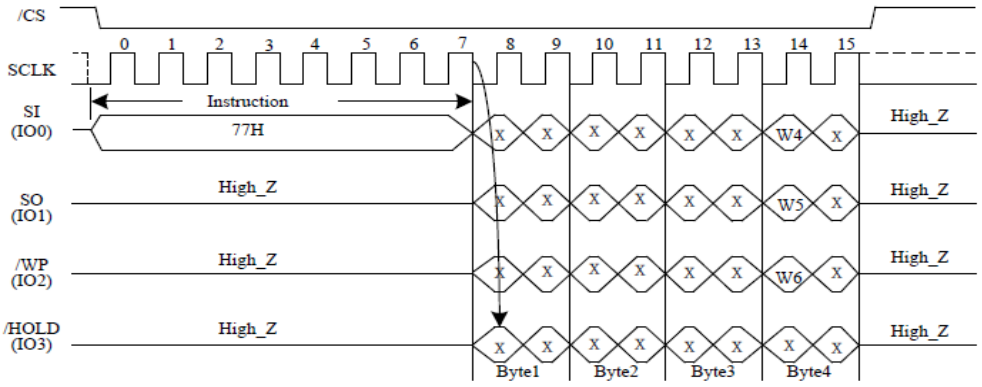


Figure 16

ID and Security Instructions

Read Manufacture ID/ Device ID (90H)

See Figure 17, the Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90H” followed by a 24-bit address (A23-A0) of 000000H. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 17 Read Manufacture ID/ Device ID Sequence Diagram

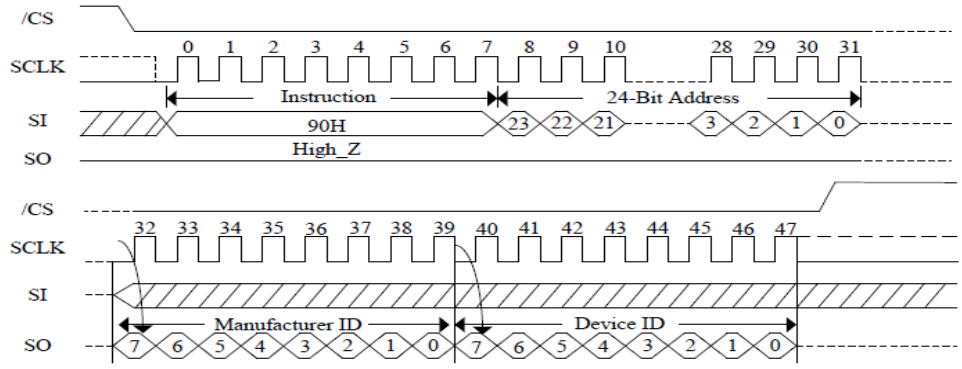


Figure 17

JEDEC ID (9FH)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

See Figure 18, he device is first selected by driving /CS to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving /CS to high at any time during data output. When /CS is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 18 JEDEC ID Sequence Diagram

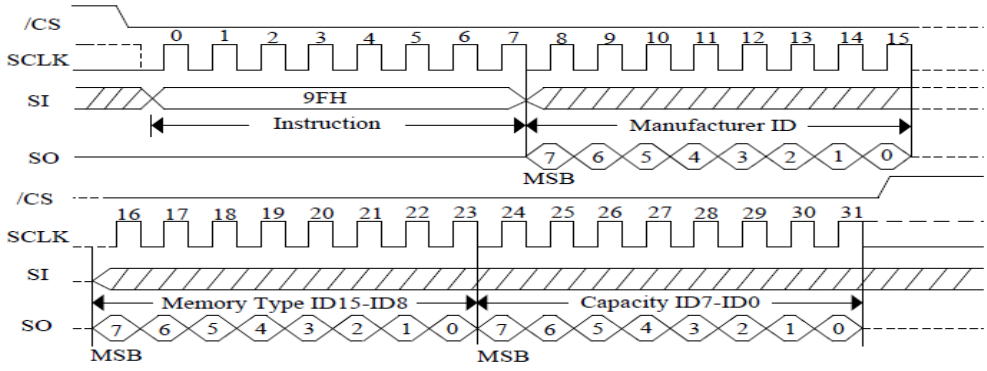


Figure 18

Deep Power-Down (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (see ICC1 and ICC2). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 19

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP. While in the power-down state only the Release from Deep Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

Figure 19 Deep Power-Down Sequence Diagram

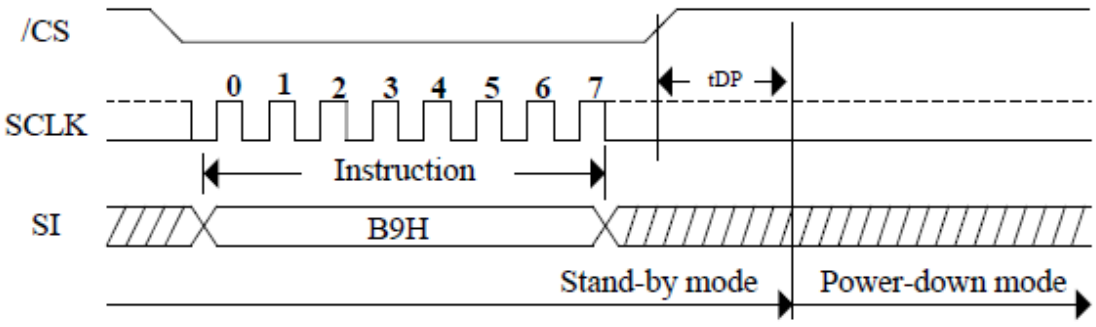


Figure 19

Release from Deep Power-Down/Read Device ID (ABH)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

See Figure 20 , to release the device from the Power-Down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABH” and driving /CS high Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instruction are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in See Figure 21 The Device ID value for the ACE25Q512G is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in See Figure 21, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instruction will be accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and will not have any effects on the current cycle.

Release Power-Down Sequence Diagram

Figure 20 Release Power-Down Sequence Diagram

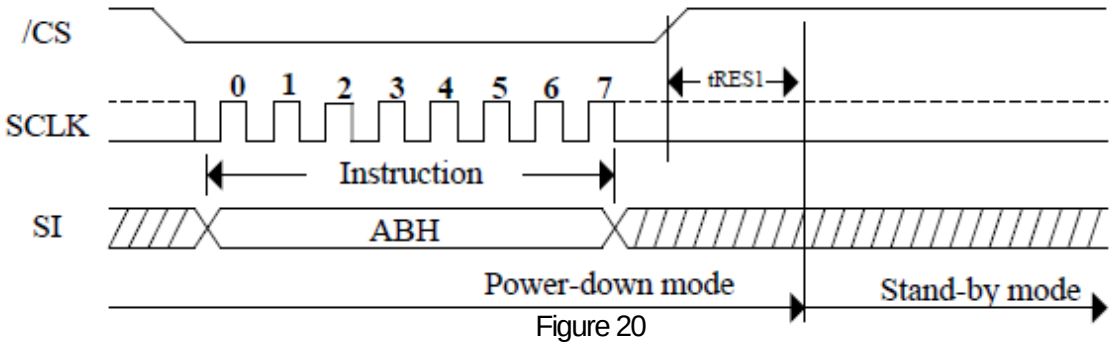


Figure 20

Figure 21 Release Power-Down/Read Device ID Sequence Diagram

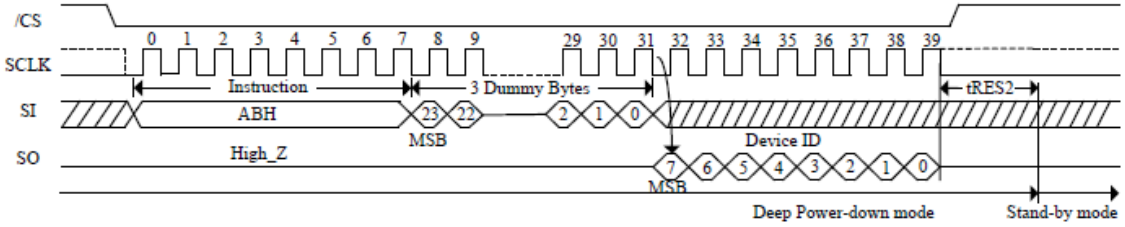


Figure 21

Read Security Registers (48H)

See Figure 22, the Read Security Registers instruction is similar to Fast Read instruction. The instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the instruction is completed by driving /CS high

Table 10

Address	A23-A16	A15-A8	A7-A0
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

Figure 22 Read Security Registers instruction Sequence Diagram

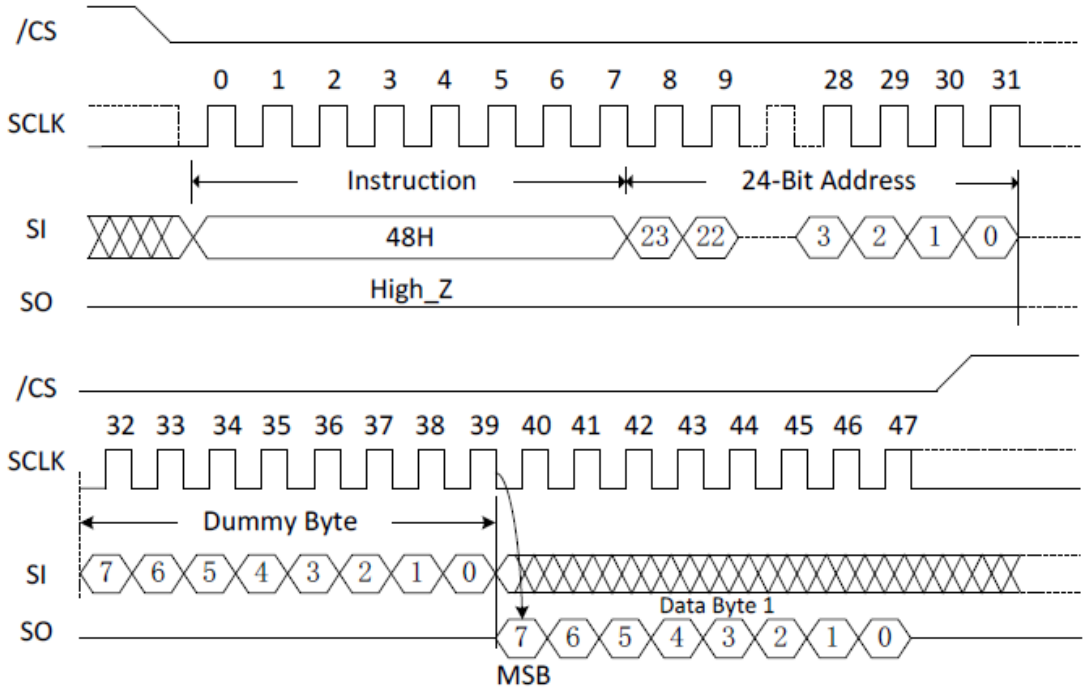


Figure 22

Erase Security Registers (44H)

The ACE25Q512G provides three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

See Figure 23, the Erase Security Registers instruction is similar to Sector/Block Erase instruction. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers instruction sequence: /CS goes low sending Erase Security Registers instruction /CS goes high. /CS must be driven high after the eighth bit of the instruction code has been latched in otherwise the Erase Security Registers instruction is not executed. As soon as /CS is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers instruction will be ignored.

Table 11

Address	A23-A16	A15-A8	A7-A0
Security Registers 1	00H	01H	Don't Care
Security Registers 2	00H	02H	Don't Care
Security Registers 3	00H	03H	Don't Care

Figure 23, Erase Security Registers instruction Sequence Diagram

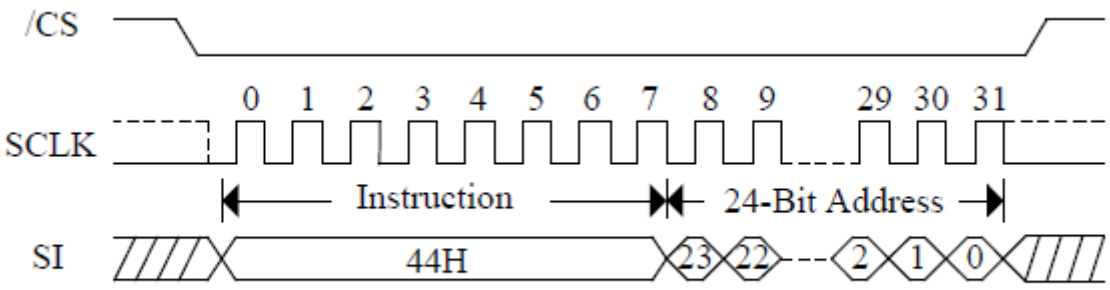


Figure 23

Program Security Registers (42H)

See Figure 24, the Program Security Registers instruction is similar to the Page Program instruction. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Program Security Registers instruction. The Program Security Registers instruction is entered by driving /CS Low, followed by the instruction code (42H), three address bytes and at least one data byte on SI. As soon as /CS is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is

0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers will be permanently locked. Program Security Registers instruction will be ignored.

Table 12

Address	A23-A16	A15-A8	A7-A0
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

Figure 24 Program Security Registers instruction Sequence Diagram

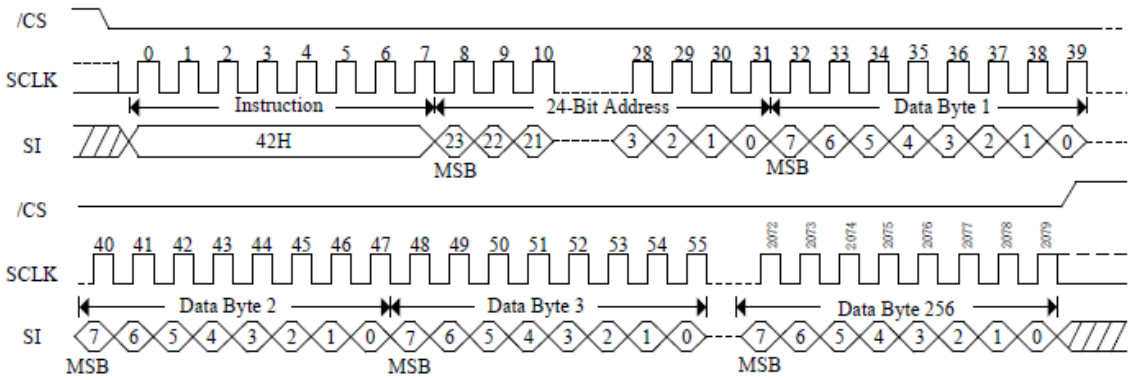


Figure 24

Program and Erase Instructions

Page Program (02H)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

See Figure 25, the Page Program instruction is entered by driving /CS Low, followed by the instruction code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low sending Page Program instruction 3-byte address on SI at least 1 byte data on SI /CS goes high. The instruction sequence is shown in Figure16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see Table 6) is not executed.

Figure 25 Page Program Sequence Diagram

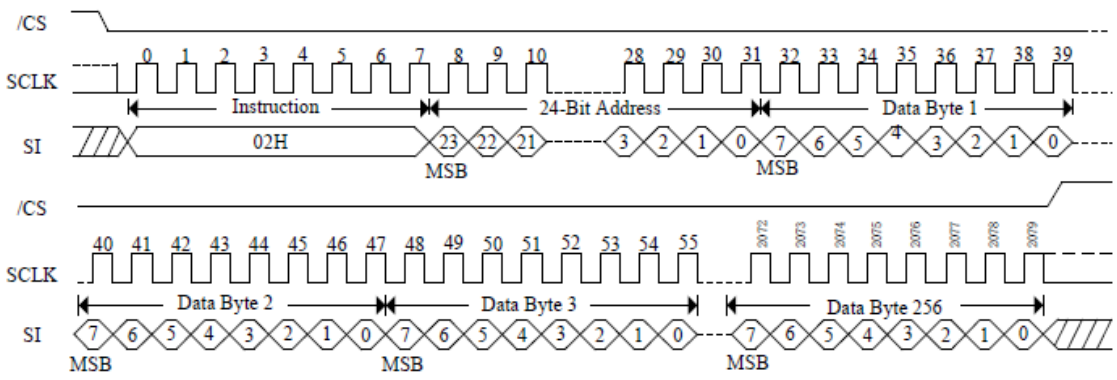


Figure 25

Sector Erase (20H)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence.

See Figure 26, the Sector Erase instruction sequence: /CS goes low sending Sector Erase instruction 3-byte address on SI /CS goes high. The instruction sequence is shown in Figure18. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see *Table 6*) is not executed.

Figure 26 Sector Erase Sequence Diagram

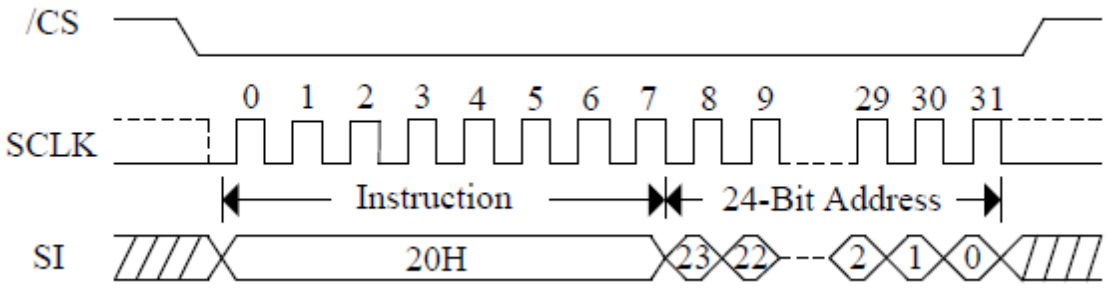


Figure 26

32KB Block Erase (52H)

The 32KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 32KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See Figure 27, the 32KB Block Erase instruction sequence: /CS goes low sending 32KB Block Erase instruction 3-byte address on SI /CS goes high. The instruction sequence is shown in Figure19. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see Table 6) is not executed.

Figure 27 32KB Block Erase Sequence Diagram

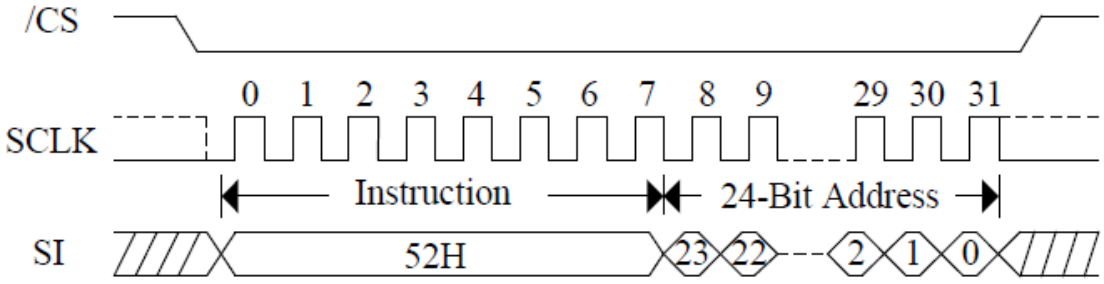


Figure 27

64KB Block Erase (D8H)

The 64KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 64KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See Figure 28, the 64KB Block Erase instruction sequence: /CS goes low sending 64KB Block Erase instruction 3-byte address on SI /CS goes high. The instruction sequence is shown in Figure20. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase instruction is not executed. As soon as /CS is driven high, theself-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see Table 6) is not executed.

Figure 28 64KB Block Erase Sequence Diagram

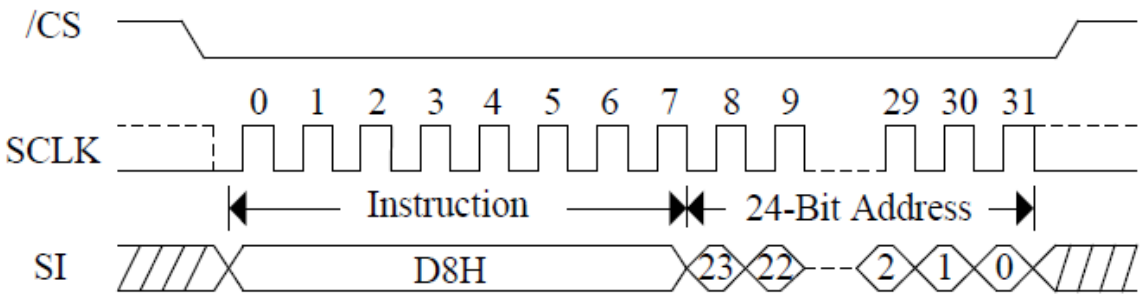


Figure 28

Chip Erase (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 29.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE. While the Chip Erase cycle is in progress, theself-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, BP0) bits (see Table 6) is not executed.

Figure 29 64KB Block Erase Sequence Diagram

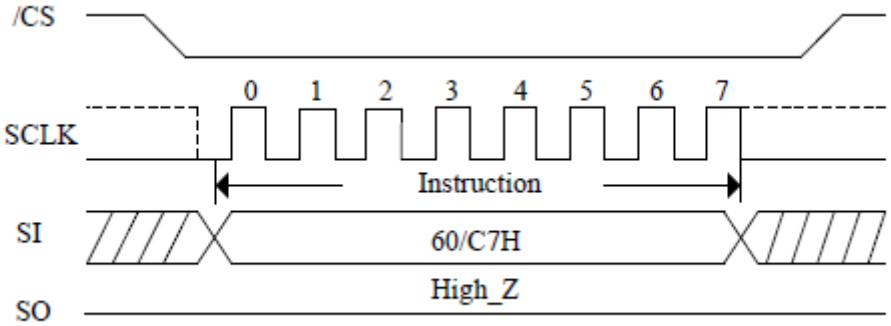


Figure 29

Erase / Program Suspend (75H)

The Erase/Program Suspend instruction allows the system to interrupt a Sector or Block Erase operation, then read from or program data to any other sector. The Erase/Program Suspend instruction also allows the system to interrupt a Page Program operation and then read from any other page or erase any other sector or block. The Erase/Program Suspend instruction sequence is shown in Figure 30.

The Write Status Registers instruction (01h) and Erase instructions (20h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Registers instruction (01h), and Program instructions (02h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program operation.

Figure 30 Erase/Program Suspend Command Sequence

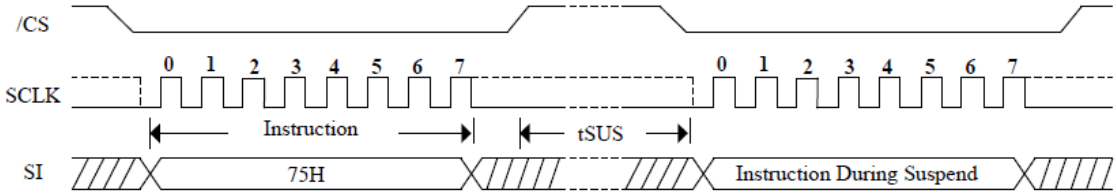


Figure 30

Erase / Program Resume (7AH)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume instruction is issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 31.

Figure 31 Erase/Program Resume Command Sequence

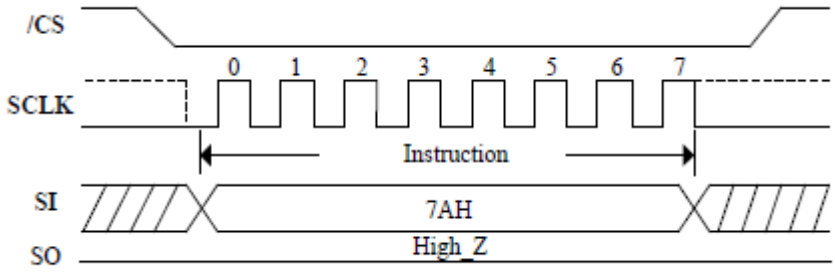


Figure 31

Reset Device Instructions

Enable Reset (7Eh) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the ACE25Q512G provides a software Reset instruction instead of a dedicated RESET pin. Once the software Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both “Enable Reset (7Eh)” and “Reset (99h)” instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (7Eh)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (7Eh)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately 30us to reset. During this period, no command will be accepted.

The Enable Reset (7Eh) and Reset (99h) instruction sequence is shown in Figure 32.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 32 Reset (7Eh) and Reset (99h) Command Sequence

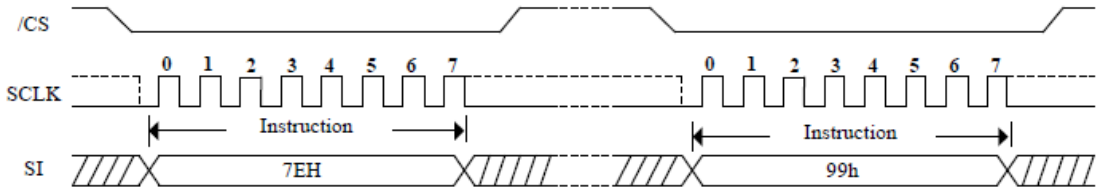


Figure 32

Electrical Characteristics

Table 13 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0Vto VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	℃
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	–2000 to +2000	V

Notes:

1. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms)

Operating Ranges

Table14

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	FR = 108MHz, fR = 50MHz	2.7	3.6	V
Temperature Operating	TA	Commercial Industrial	0 -40	+70 +85	℃

Data Retention and Endurance

Table 15

Parameter	Test Condition	Min	Units
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85°C	100K	Cycles

Latch Up Characteristics

Table16

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

Power-up Timing

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To /CS Low	10		us
tPUW	Time Delay From VCC(min) To Write Instruction	1	10	ms
VWI	Write Inhibit Voltage VCC(min)	1	2.5	V

Figure 33 Power-up Timing and Voltage Levels

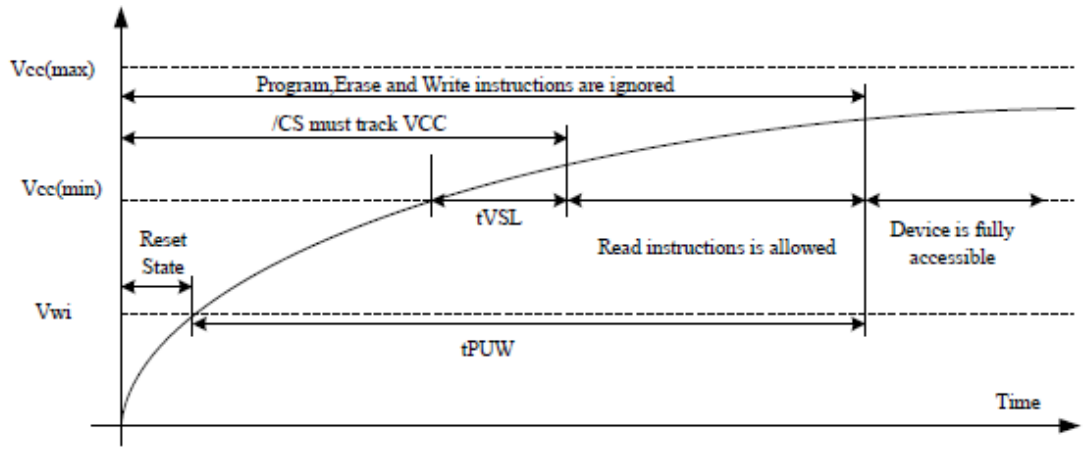


Figure 33

DC Electrical Characteristics
(T= -40℃~85℃, VCC=2.7~3.6V)
Table17

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
ILI	Input Leakage Current				±2	µA
ILO	Output Leakage Current				±2	µA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		13	25	µA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		2	5	µA
ICC3	Current: Read Single/Dual/Quad 1MHz	SCLK=0.1VCC/ 0.9VCC(1)		3/4/5	3.5/5/6	mA
	Current: Read Single/Dual/Quad 33MHz			5/11/19	7.5/12/19.5	mA
	Current: Read Single/Dual/Quad 50MHz			6.5/16/30	9.5/17/33	mA
	Current: Read Single/Dual/Quad 108MHz			10/33/60	12/35/65	mA
ICC4	Operating Current(Page Program)	/CS=VCC			15	mA
ICC5	Operating Current(WRSR)	/CS=VCC			5	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC			20	mA
ICC7	Operating Current(Block Erase)	/CS=VCC			20	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC			20	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100µA			0.4	V
VOH	Output High Voltage	IOH =-100µA	VCC-0.2			V

Note:
(1) ICC3 is measured with ATE loading

AC Measurement Conditions

Table18

Symbol	Parameter	Min	Tpy	Max	Unit
CL	Load Capacitance			30	pF
TR, TF	Input Rise And Fall time			5	ns
VIN	Input Pause Voltage	0.2VCC to 0.8VCC			V
IN	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V
OUT	Output Timing Reference Voltage	0.5VCC			V

Figure 34 AC Measurement I/O Waveform

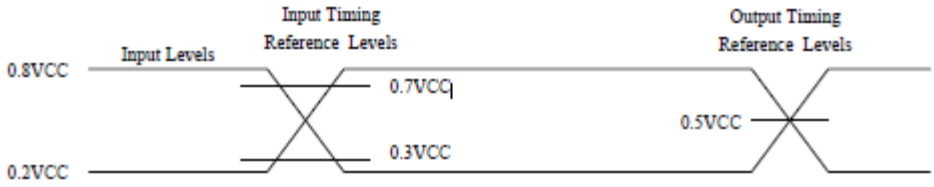


Figure 34

AC Electrical Characteristics

Table19

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fc	Clock frequency for all instructions, except Read Data(03H)	DC.		108	MHz
fR	Clock freq. Read Data instruction(03H)	DC.		55	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time（read/write）	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns
tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid			7	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			0.1	µs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			3	µs
tRES2	/CS High To Standby Mode With Electronic Signature Read			1.5	µs
tSUS	/CS High To Next Instruction After Suspend			2	µs
tW	Write Status Register Cycle Time		10	15(2)	ms
tBP1	Byte Program Time (First Byte) (3)		5	10	µs
tBP2	Additional Byte Program Time (After First Byte) (3)		2.8	5	µs
tPP	Page Programming Time		0.7	2.4	ms
tSE	Sector Erase Time		60	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.3/0.5	1.2/1.5	s
tCE	Chip Erase Time		0.5	1.5	s

Note:

1. Tested with clock frequency lower than 50 MHz.
2. tW can be up to 45 ms at -40℃ during the characterization of the current design. It will be improved in the future design.
3. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.

Figure 35 Serial Input Timing

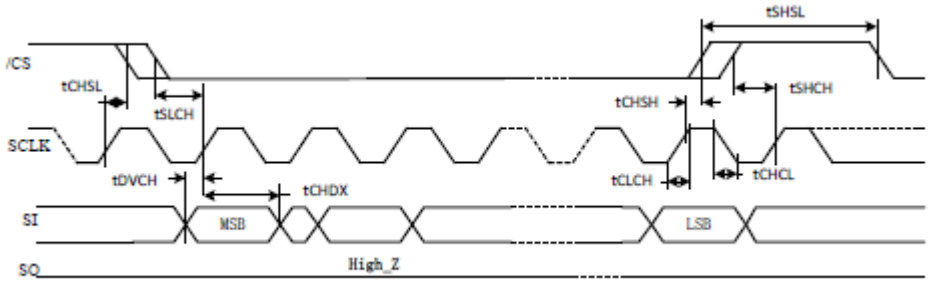


Figure 35

Figure 36 Output Timing

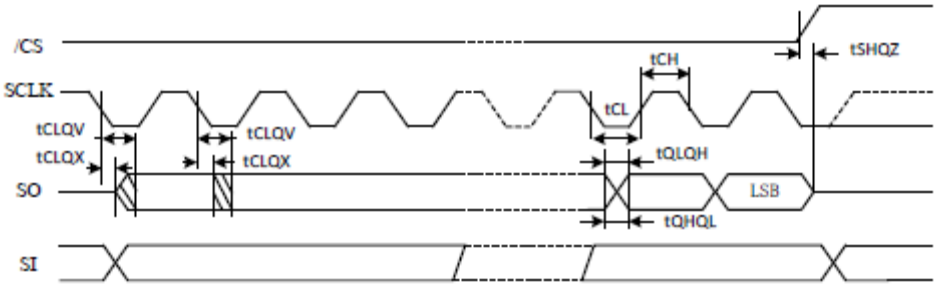


Figure 36

Figure 37 Hold Timing

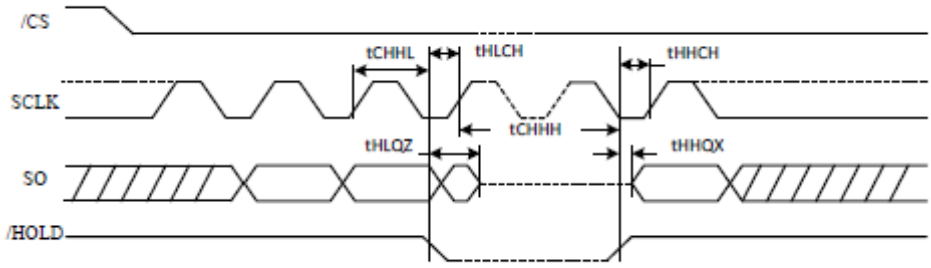
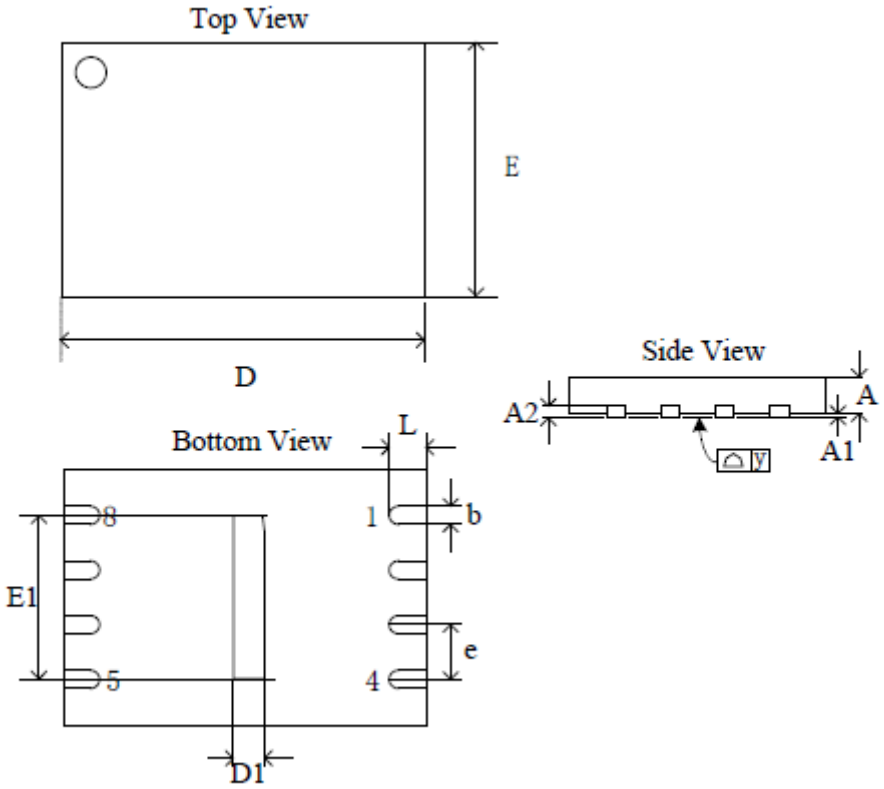


Figure 37

Packaging information

USON8



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	0.50	0.55	0.60	0.02	0.022	0.024
A1			0.05			0.002
A2	0.13	0.15	0.18	0.005	0.006	0.007
b	0.18	0.25	0.30	0.007	0.010	0.118
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	0.15	0.20	0.30	0.006	0.008	0.012
E	1.90	2.00	2.10	0.0752	0.079	0.083
E1	1.50	1.60	1.70	0.059	0.063	0.067
e		0.50			0.020	
y	0.00		0.05	0.000		0.002
L	0.30	0.35	0.45	0.012	0.014	0.018

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ACE Technology Co., LTD.
http://www.ace-ele.com/