ACPM-7353

CDMA Dual Band 4x5 Power Amplifier Module (Cellular/PCS)

Data Sheet

Description

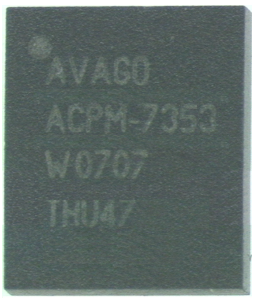
The ACPM-7353 is a dual-band PAM (Power Amplifier Module) designed for CDMA (code division multiple access) cellular and PCS. The ACPM-7353 meets stringent CDMA linearity requirements to and beyond 28dBm output power in both bands. The 4mmx5mm form factor 14-pin surface mount package is self contained, incorporating 50ohm input and output matching networks

The ACPM-7353 features 5th generation of CoolPAM circuit technology which supports 3 modes – bypass, mid and high power modes. The CoolPAM is stage bypass technology which enables power amplifier to lower power consumption. Active bypass feature is added to 5th generation to enhance power added efficiency at low output range and this technology extends talk time of mobiles more by further saving power amplifier's current consumption.

The power amplifier is manufactured on an advanced InGaP HBT (hetero-junction Bipolar Transistor) MMIC (microwave monolithic integrated circuit) technology offering state-of-the-art reliability, temperature stability and ruggedness

The Module is housed in a cost effective, small and thin 4x5mm package.

Component Image



Features

- Dual-Band PA (Cellular and PCS)
- Small Size (4x5mm)
- Thin Package (0.9mm typ)
- Excellent Linearity
- 3-mode power control
  Bypass / Mid Power Mode / High Power Mode
- High Efficiency at max output power
- 14-pin surface mounting package
- Internal 50ohm matching networks for both RF input and output
- Lead-free, RoHS compliant, Green

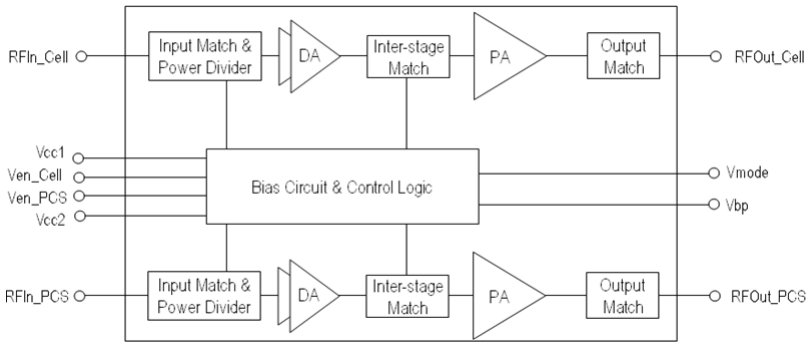
Applications

- Digital CDMA Cellular and PCS Dual Band

Ordering Information

Part Number	Number of Devices	Container
ACPM-7353-TR1G	1000	178mm (7") Tape/Reel
ACPM-7353-BLK	100	Bulk

Functional Block Diagram



Absolute Maximum Ratings

No damage assuming only one parameter is set at limit at a time with all other parameters set at or below typical value

Operation of any single parameter outside these conditions with the remaining parameters set at or below typical values may result in permanent damage.

Description	Min	Typ	Max	Unit	Associated Pins
RF Input Power (high power mode) Output power (bypass mode, Cell & PCS) Output power in mid power mode (Cell) Output power in mid power mode (PCS)		0	10 11 16 18	dBm	RFIn_Cell, RFIn_PCS RFOut_Cell, RFOut_PCS RFOut_Cell RFOut_PCS
DC Supply Voltage	0	3.4	5.0	V	Vcc1, Vcc2
Enable Voltage	0	2.6	3.3	V	Ven
Mode Control Voltage	0	2.6	3.3	V	Vmode
Bypass Control	0	2.6	3.3	V	Vbp
Storage Temperature	-55	25	+125	°C	

Recommended Operating Condition

Description		Min	Typ	Max	Unit
DC Supply Voltage		3.2	3.4	4.2	V
Enable Voltage (Ven)	LOW HIGH	0 1.35	0 2.6	0.5 2.9	V V
Mode Control Voltage (Vmode)	LOW HIGH	0 1.35	0 2.6	0.5 2.9	V V
Bypass Control Voltage (Vbp)	LOW HIGH	0 1.35	0 2.6	0.5 2.9	V V
Operating Frequency Cellular PCS		 824 1850		 849 1910	 MHz MHz
Ambient Temperature		-30	25	85	°C

Operating Logic Table

Power Mode	Ven	Vbp	Vmode	Cellular Pout	PCS Pout
High Power Mode	HIGH	HIGH	LOW	~28dBm	~28dBm
Mid Power Mode	HIGH	HIGH	HIGH	~16dBm	~18dBm
Bypass Mode	HIGH	LOW	–	~11dBm	~11dBm
Shut Down Mode	LOW	LOW	LOW	–	–

Electrical Characteristics in Cellular Band

- Conditions: Vcc=3.4V, Ven=2.6V, T=25°C, Zin/Zout=50ohm

Characteristics		Condition	Min	Typ	Max	Unit
Operating Frequency Range			824	–	849	MHz
Gain		High Power Mode, Pout=28 dBm	24	27.5		dB
		Mid Power Mode, Pout=16 dBm	14	17.5		dB
		Bypass Power Mode, Pout=11dBm	8.5	12		dB
Power Added Efficiency		High Power Mode, Pout=28 dBm	35.3	38.2		%
		Mid Power Mode, Pout=16 dBm	12.8	16.7		%
		Bypass Power Mode, Pout=11dBm	8.0	12.0		%
Total Supply Current		High Power Mode, Pout=28 dBm		485	525	mA
		Mid Power Mode, Pout=16 dBm		69	90	mA
		Bypass Power Mode, Pout=11dBm		29	43	mA
Quiescent Current		High Power Mode	68	91	115	mA
		Mid Power Mode	11	23	33	mA
		Bypass Mode	1	3	5	mA
Enable Current					100	uA
Mode Control Current					100	uA
Bypass Control Current					100	uA
Total Current in Power-down mode		Ven=0V, Vmode=0V, Vbp=0V		0.2	5	μA
Adjacent Channel Power Ratio	900 kHz offset 1.98 MHz offset	High Power Mode, Pout=28 dBm		-48 -59	-46 -56	dBc dBc
	900 kHz offset 1.98 MHz offset	Mid Power Mode, Pout=16 dBm		-52 -68	-46 -57	dBc dBc
	900 kHz offset 1.98 MHz offset	Bypass Mode, Pout=11dBm		-58 -68	-46 -57	dBc dBc
Harmonic Suppression	Second Third	High Power Mode, Pout=28 dBm			-30 -40	dBc dBc
Input VSWR				2:1	2.5:1	
Stability (Spurious Output)		In-Band Load VSWR <= 5:1, All Phase Out of Band Load VSWR <= 10:1, All Phase Forwarded power fixed			-60	dBc
Noise Power in Rx Band				-136	-132	dBm/Hz
Ruggedness		No Damage Pout<28dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR

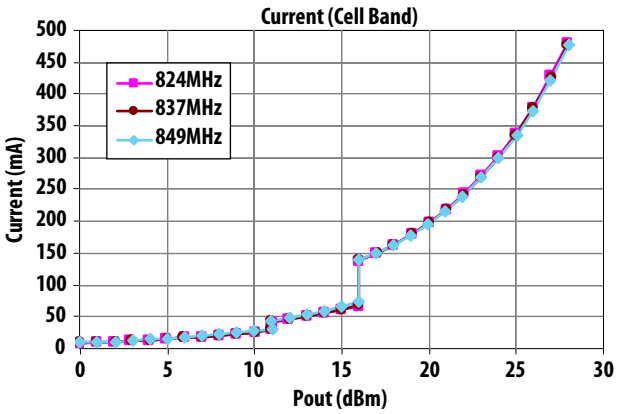
Electrical Characteristics in PCS Band

- Conditions: Vcc=3.4V, Ven=2.6V, T=25°C, Zin/Zout=50ohm

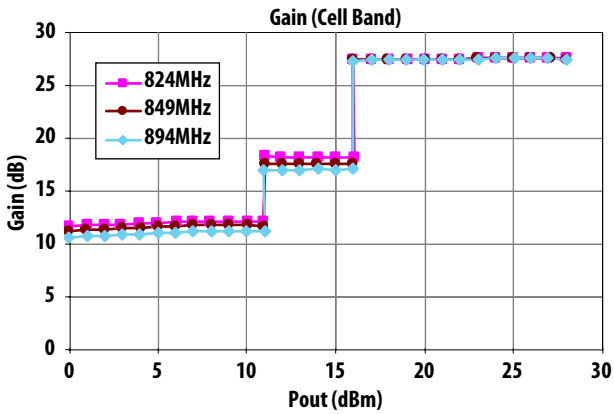
Characteristics		Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range			1850	–	1910	MHz
Gain		High Power Mode, Pout=28 dBm	23	26		dB
		Mid Power Mode, Pout=18 dBm	13	16.5		dB
		Bypass Power Mode, Pout=11dBm	6.5	10.5		dB
Power Added Efficiency		High Power Mode, Pout=28 dBm	35.3	38.2		%
		Mid Power Mode, Pout=18 dBm	15.1	19.1		%
		Bypass Power Mode, Pout=11dBm	7.6	10.6		%
Total Supply Current		High Power Mode, Pout=28 dBm		485	535	mA
		Mid Power Mode, Pout=18 dBm		95	120	mA
		Bypass Power Mode, Pout=11dBm		32	45	mA
Quiescent Current		High Power Mode	80	105	125	mA
		Mid Power Mode	18	28	38	mA
		Bypass Mode	1	3	5	mA
Enable Current					100	uA
Mode Control Current					100	uA
Bypass Control Current					100	uA
Total Current in Power-down mode		Ven=0V, Vmode=0V, Vbp=0V		0.2	5	µA
Adjacent Channel Power Ratio	1.25 MHz offset 1.98 MHz offset	High Power Mode, Pout=28 dBm		-48 -56	-46 -53	dBc dBc
	1.25 MHz offset 1.98 MHz offset	Mid Power Mode, Pout=18 dBm		-56 -63	-46 -53	dBc dBc
	1.25 MHz offset 1.98 MHz offset	Bypass Mode, Pout=11 dBm		-54 -66	-46 -53	dBc dBc
Harmonic Suppression	Second Third	High Power Mode, Pout=28 dBm			-30 -40	dBc dBc
Input VSWR				2:1	2.5:1	
Stability (Spurious Output)		In-Band Load VSWR <= 5:1, All Phase Out of Band Load VSWR <= 10:1, All Phase Forwarded power fixed			-60	dBc
Noise Power in Rx Band				-138.5	-133	dBm/Hz
Ruggedness		No Damage Pout<28dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR

Characteristics Data of Cell Band

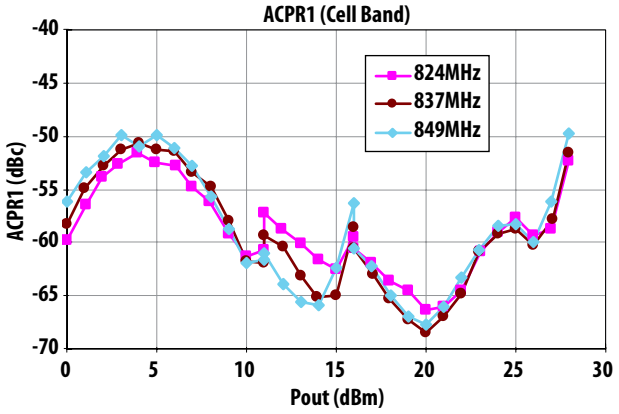
(Vcc=3.4V, Ven=2.6, Vbp, Vmode= 0V or 2.6V, T=25°C, Zin/Zout=50ohm, IS-95 RL)



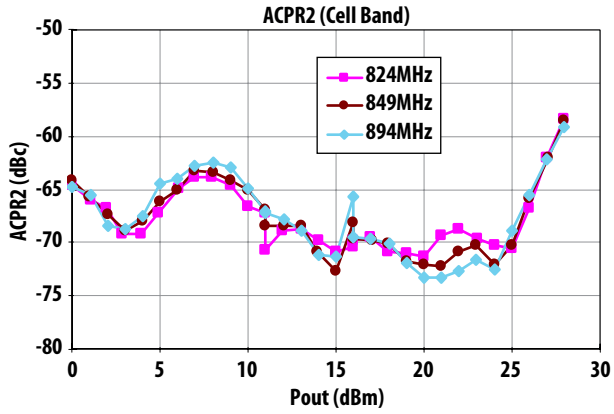
Total Current vs. Output Power



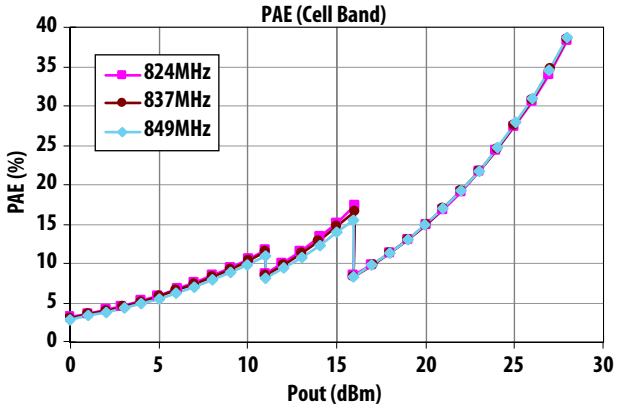
Gain vs. Output Power



Adjacent Channel Power Ratio 1 vs. Output Power



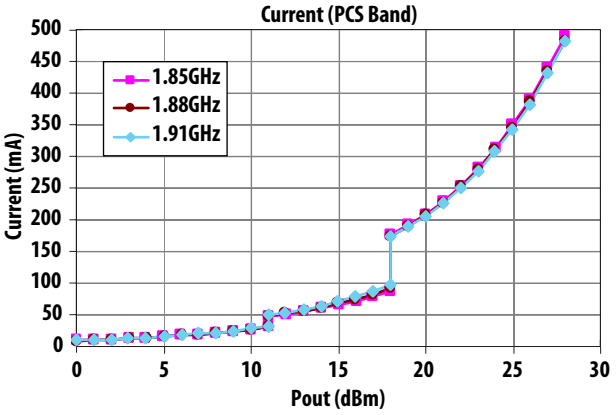
Adjacent Channel Power Ratio 2 vs. Output Power



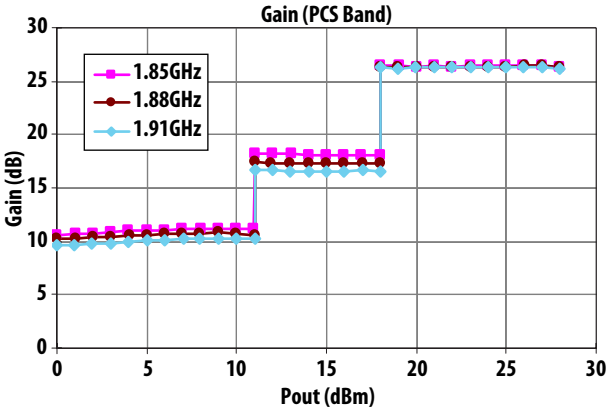
Power Added Efficiency vs. Output Power

Characteristics Data of PCS Band

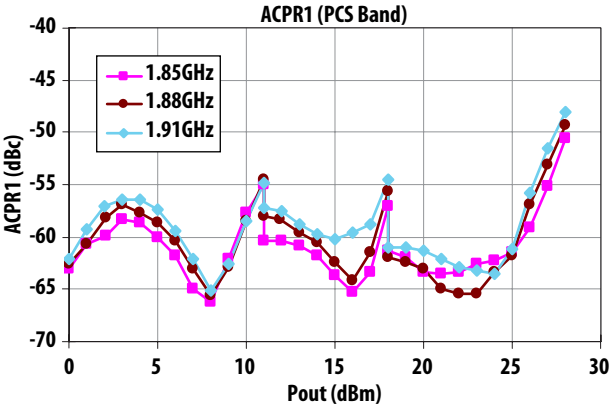
(Vcc=3.4V, Ven=2.6, Vbp, Vmode= 0V or 2.6V, T=25°C, Zin/Zout=50ohm, IS-95 RL)



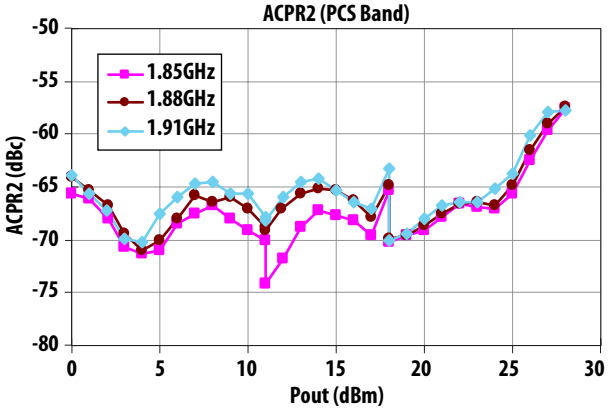
Total Current vs. Output Power



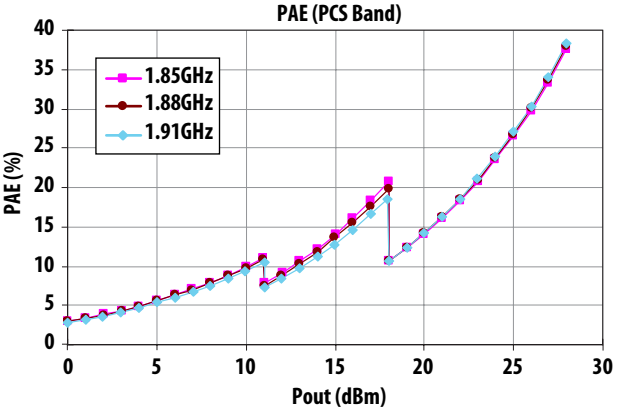
Gain vs. Output Power



Adjacent Channel Power Ratio 1 vs. Output Power

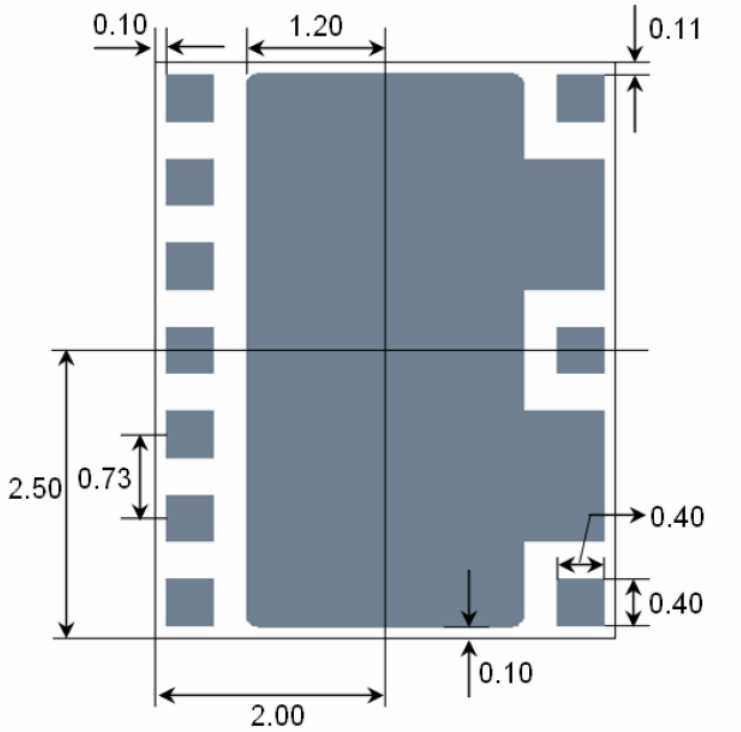


Adjacent Channel Power Ratio 2 vs. Output Power



Power Added Efficiency vs. Output Power

Footprint



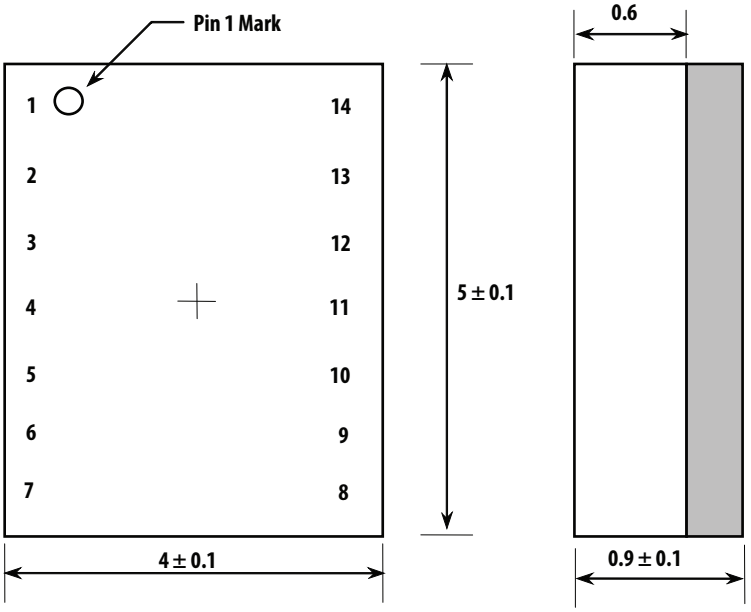
X-RAY TOP VIEW

All dimensions are in millimeters

PIN DESCRIPTIONS

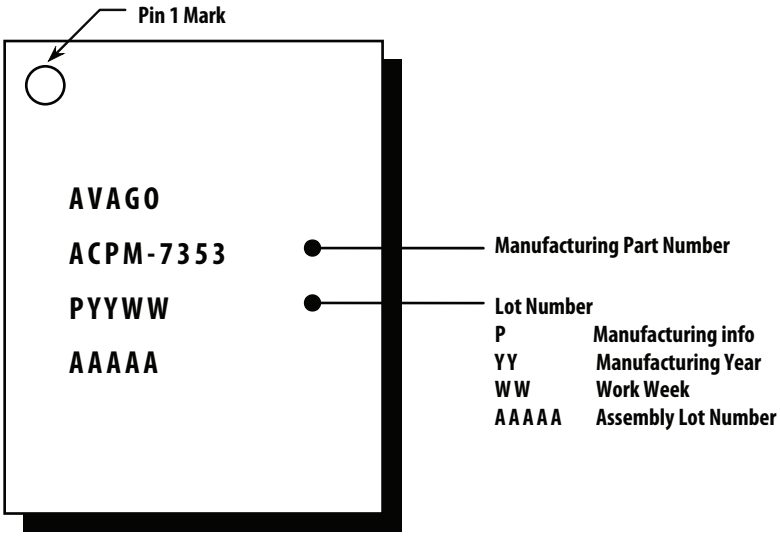
Pin #	Name	Description
1	RFIn_Cell	Cellular Band RF Input
2	Vmode	Mode Control
3	Vbp	Bypass Control
4	Vcc1	Supply Voltage
5	Ven_Cell	Cellular Band PA Enable
6	Ven_PCS	PCS Band PA Enable
7	RFIn_PCS	PCS Band RF Input
8	RFOut_PCS	PCS Band RF Output
9	GND	Ground
10	GND	Ground
11	Vcc2	Supply Voltage
12	GND	Ground
13	GND	Ground
14	RFOut_Cell	Cellular Band RF Output

Package Dimensions

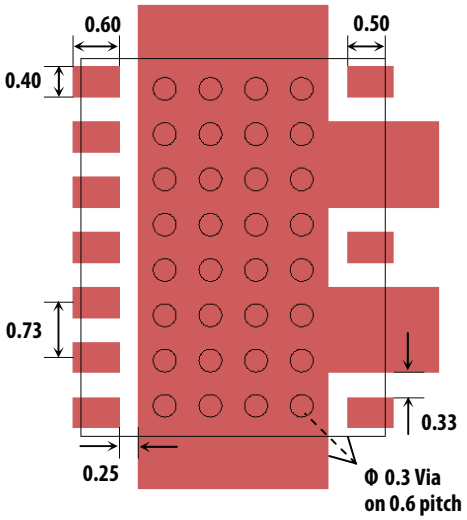


All dimensions are in millimeters

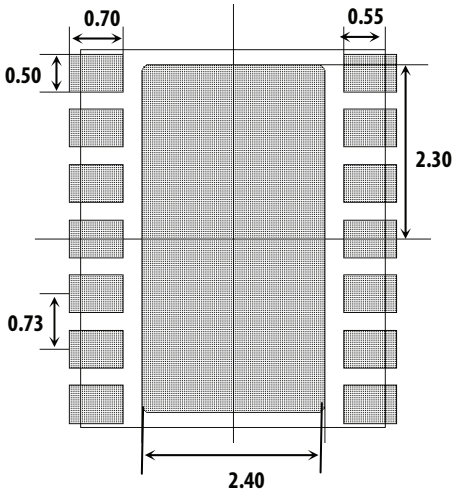
Marking Specification



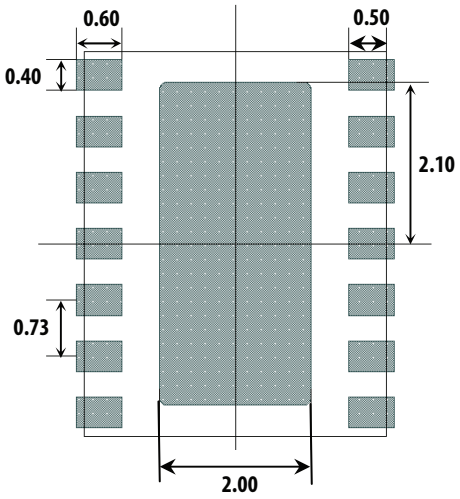
Metallization



Solder Mask Opening



Solder Paste Stencil Aperture



PCB Design Guidelines

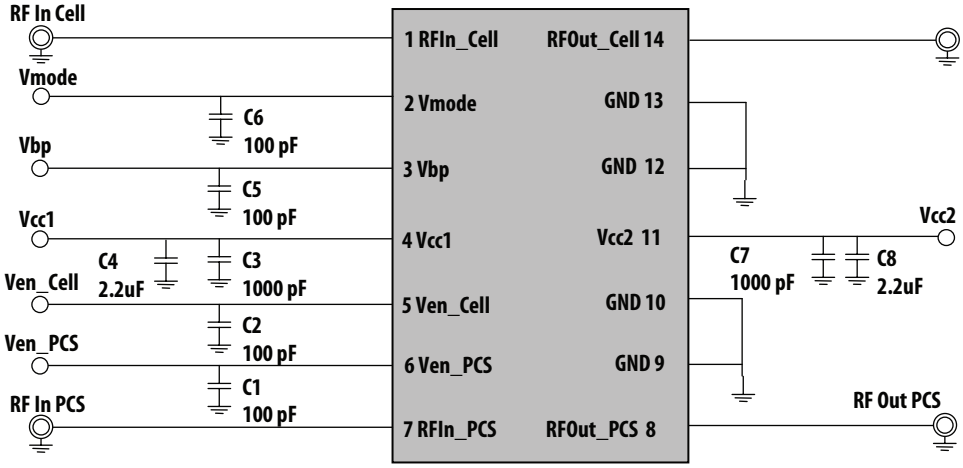
The recommended PCB land pattern is shown in figures on the left side. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

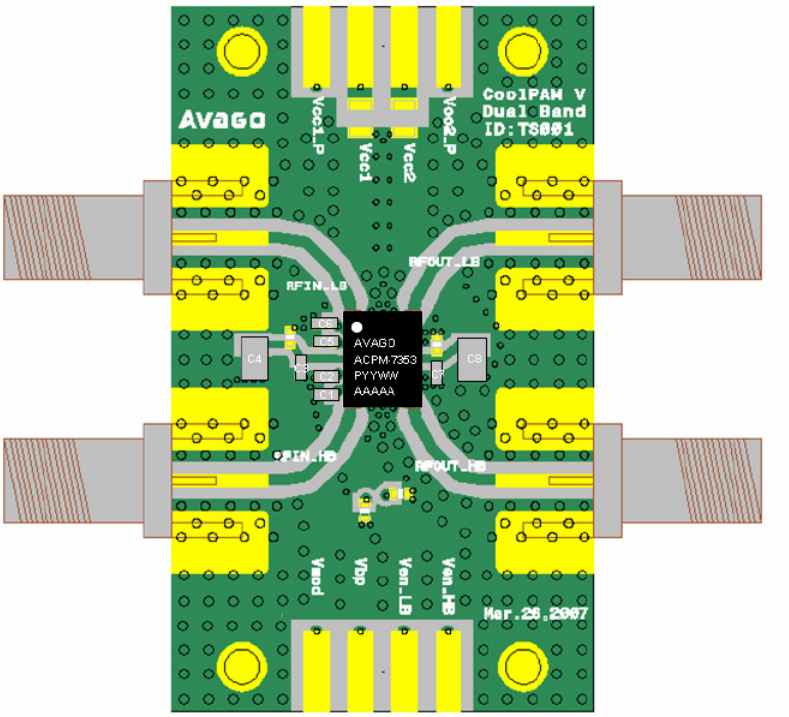
A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown here. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm(4mils) or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

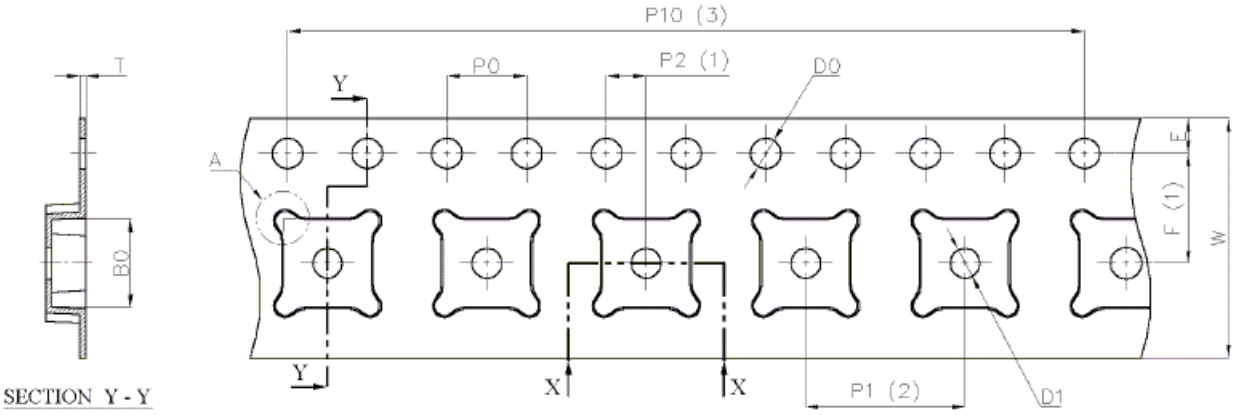
Evaluation Board Schematic

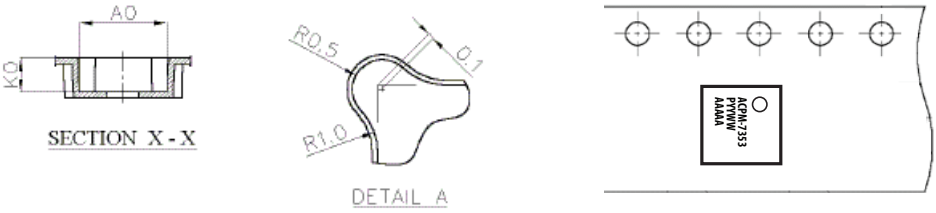


Evaluation Board Description



Tape and Reel Information





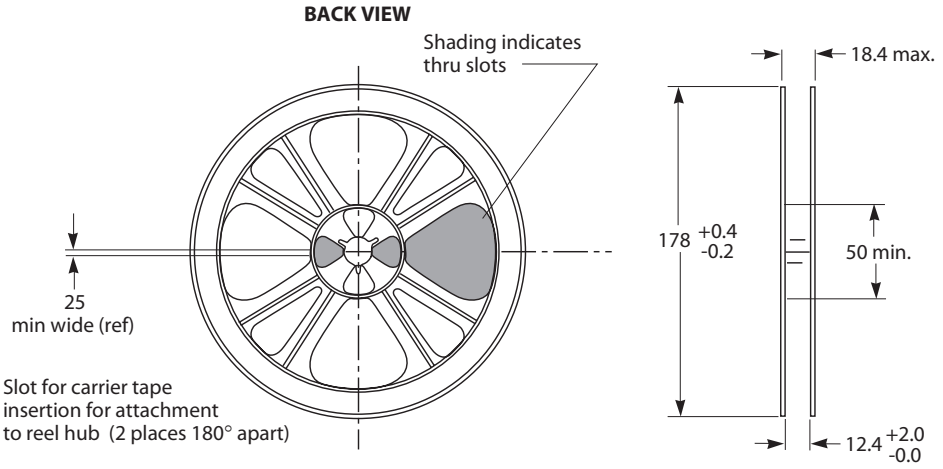
Dimension List

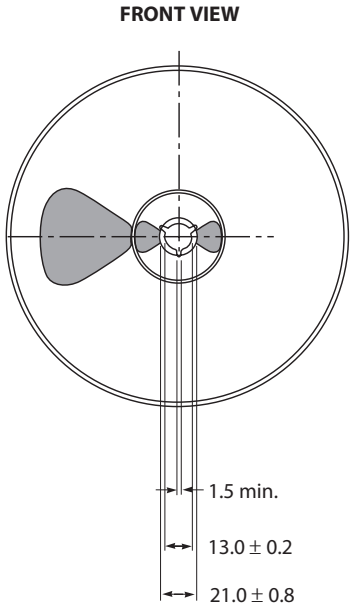
Annote	Millimeter
A0	4.40±0.10
B0	5.30±0.10
K0	1.20±0.10
D0	1.55±0.05
D1	1.60±0.10
P0	4.00±0.10

Annote	Millimeter
P2	2.00±0.05
P10	40.00±0.20
E	1.75±0.10
F	5.50±0.05
W	12.00±0.30
T	0.30±0.05

Tape and Reel Format – 4 mm x 5 mm

Reel Drawing





NOTES:
1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

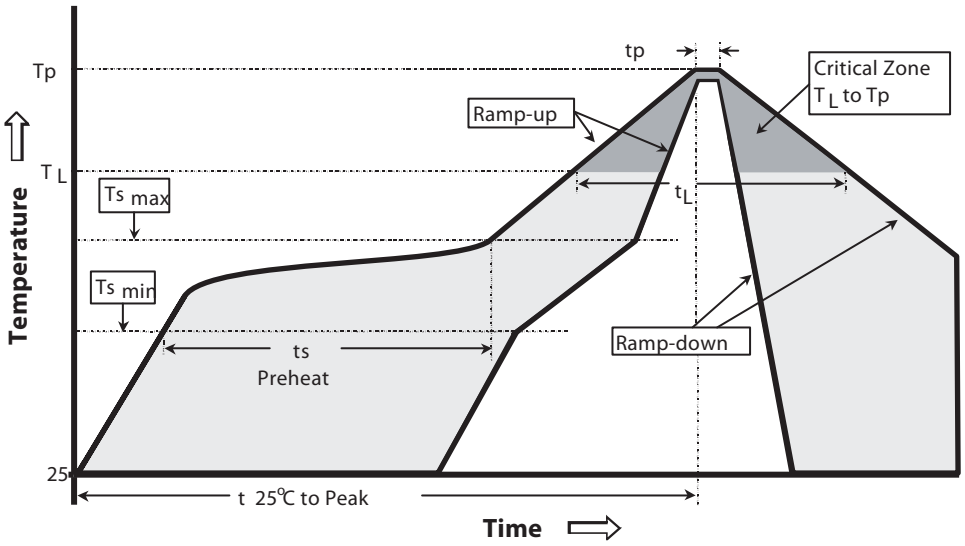
ACPM-7353 is MSL3. Thus, according to the J-STD-033 p.10, the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-7353 is targeted at 260°C +0/-5°C. Figure and table on next page show typical SMT profile for maximum temperature of 260 +0/-5°C.

Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30°C/60% RH or as stated
1	Unlimited at =< 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

Reflow Profile Recommendations



Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Typical SMT Reflow Profile for Maximum Temperature = 260 +0/ -5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3°C/sec max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100°C 150°C 60-120 sec	 150°C 200°C 60-120 sec
Tsmax to TL - Ramp-up Rate		 3°C/sec max
Time maintained above: - Temperature (TL) - Time (TL)	 183°C 60-150 sec	 217°C 60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.6.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours with factory conditions <30°C and 60% RH as listed in the Table 5-1 on the J-STD-020D p.6.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above has not been satisfied. The baking conditions are listed in the Table 4-1 on the J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 andIPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in table of Moisture Classification Level and Floor Life. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table on follwoing page lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating this table:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C, 35°C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified) Maximum Percent Relative Humidity

		Maximum Percent Relative Humidity										
Package Type and Body Thickness	**Moisture Sensitivity Level**	**5%**	**10%**	**20%**	**30%**	**40%**	**50%**	**60%**	**70%**	**80%**	**90%**	
Body Thickness ≥3.1 mm Including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	94	44	32	26	16	7	5	4	35°C
		∞	∞	124	60	41	33	28	10	7	6	30°C
		∞	∞	167	78	53	42	36	14	10	8	25°C
		∞	∞	231	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	8	7	6	6	6	4	3	3	35°C
		∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	3	3	3	2	2	2	2	1	1	35°C
		∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	2	2	2	2	1	1	1	1	1	35°C
		∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	1	1	1	1	1	1	1	1	1	35°C
		∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	58	30	22	3	2	1	35°C
		∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	12	9	7	6	5	2	2	1	35°C
		∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	5	4	3	3	2	2	1	1	1	35°C
		∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	3	2	2	2	2	1	1	1	1	35°C
		∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	1	1	1	1	1	1	1	0.5	0.5	35°C
		∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	17	1	0.5	0.5	35°C
		∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	8	5	1	0.5	0.5	35°C
		∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	7	4	3	2	1	0.5	0.5	35°C
		∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	7	3	2	2	1	1	0.5	0.5	35°C
		∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	7	2	1	1	1	1	1	0.5	0.5	35°C
		∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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