

January 1996

# ACS541MS

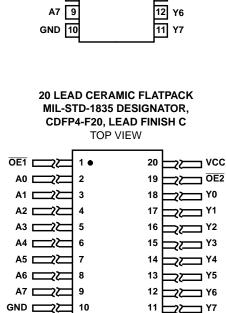
# **Radiation Hardened Octal Buffer/** Line Driver Three-State

Features	Pinouts
<ul> <li>Devices QML Qualified in Accordance with MIL-PRF-38535</li> <li>Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96710 and Intersil's QM Plan</li> <li>1.25 Micron Radiation Hardened SOS CMOS</li> <li>Total Dose</li></ul>	20 LEAD CERAMIC DUAL-IN-LINE MIL-STD-1835 DESIGNATOR, CDIP2-T20, LEAD FINISH C TOP VIEW 0E1 1 20 VCC A0 2 19 0E2 A1 3 18 Y0 A2 4 17 Y1 A3 5 16 Y2 A4 6 15 Y3 A5 7 14 Y4 A6 8 13 Y5 A7 9 12 Y6 GND 10 11 Y7
<ul> <li>Input Logic Levels <ul> <li>VIL = 30% of VCC Max</li> <li>VIH = 70% of VCC Min</li> </ul> </li> <li>Input Current ≤ 1µA at VOL, VOH</li> <li>Fast Propagation Delay</li></ul>	20 LEAD CERAMIC FLATPACK MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C TOP VIEW
Description	

The Intersil ACS541MS is a Radiation Hardened Octal Buffer/Line Driver, with three-state outputs. The output enable pins OE1, OE2 control the Three-State outputs. If either enable is high the output will be in a high impedance state. For data output both enables must be low.

The ACS541MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

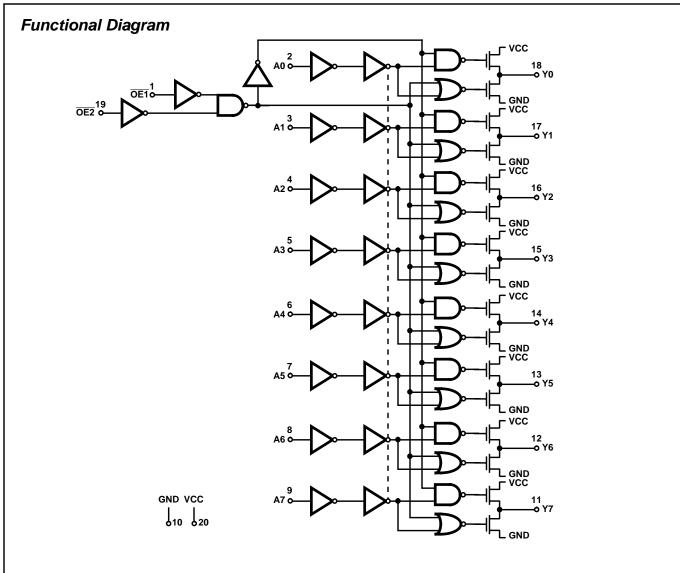
The ACS541MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line package (D suffix).



# **Ordering Information**

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9671001VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9671001VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACS541D/Sample	25°C	Sample	20 Lead SBDIP
ACS541K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACS541HMSR	25°C	Die	Die

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. 1-888-INTERSIL or 321-724-7143 | Copyright © Intersil Corporation 1999



#### TRUTH TABLE

INPUTS			OUTPUTS
OE1	OE2	An	Yn
L	L	н	Н
L	L	L	L
н	Х	Х	Z
Х	Н	Х	Z

NOTE: L = Low Logic Level, H = High Logic Level, Z = High Impedance

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# **Die Characteristics**

#### DIE DIMENSIONS:

102 mils x 102 mils 2,600mm x 2,600mm

## METALLIZATION:

Type: AlSi Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

#### **GLASSIVATION:**

Type: SiO<sub>2</sub> Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

 $<2.0 \text{ x} 10^5 \text{ A/cm}^2$ 

## BOND PAD SIZE:

> 4.3 mils x 4.3 mils

> 110µm x 110µm

## Metallization Mask Layout

