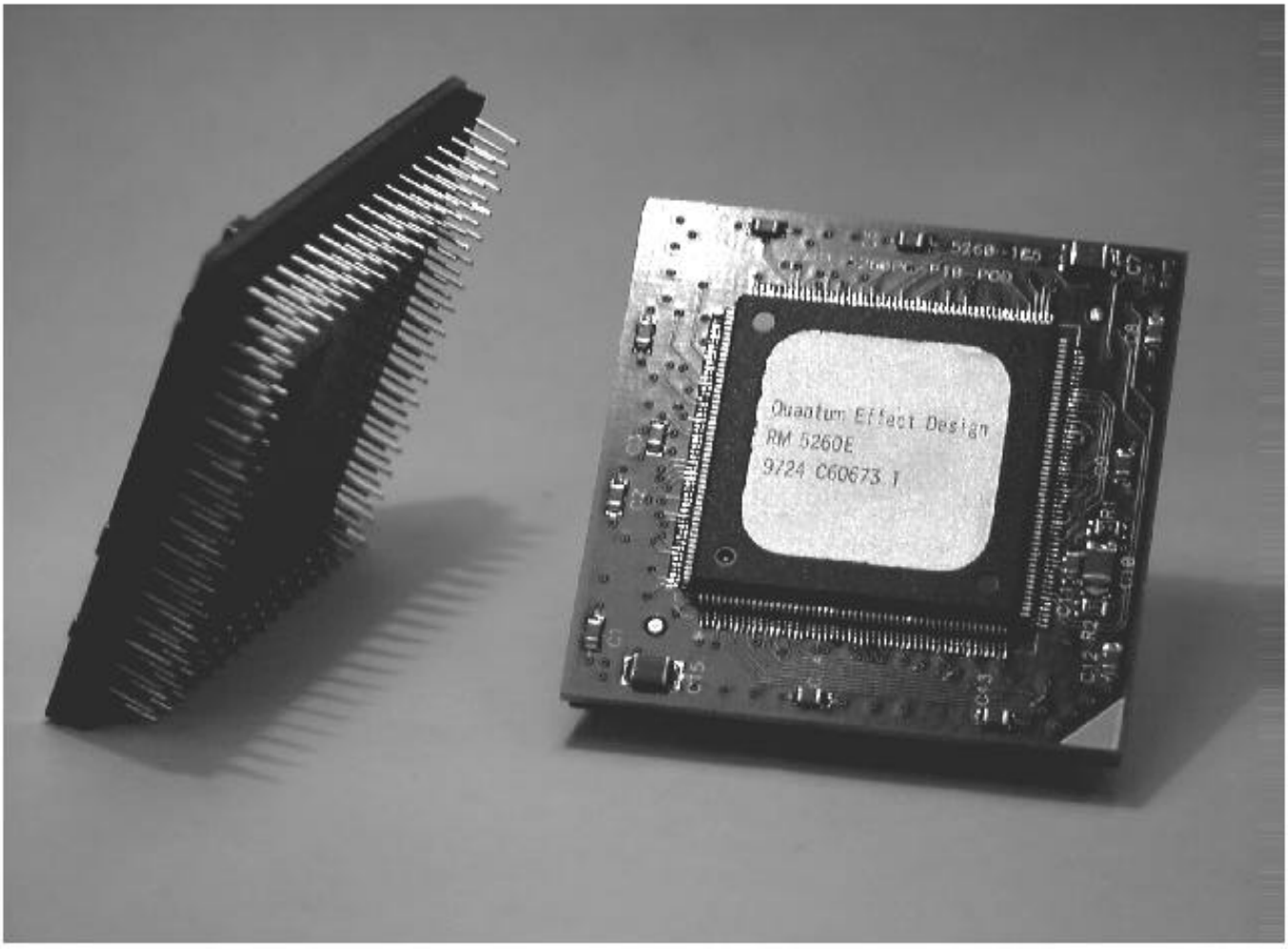
ACT5260PC-P10-POD
FR4 Adapter

The Aeroflex ACT5260PC-P10-POD adapts a QED RM5260 MIPS microprocessor to an R4400PC, R4600 or R4700 processor's 179 pin PGA footprint. This product allows the evaluation of the latest MIPS IV 5XXX series performance in existing 4XXX series hardware. Some of the performance enhancements include:

- **Allows potentially higher pipeline clock rates due to it multiplication of the input clock by 2,3,4,5,6,7 or 8 compared to the 4XXX series method of multiplying the input clock by only 2, then dividing it down by 2,3,4 etc for output system clock.**
- **The RM5260 is a 3.3 volt device with 5 volt tolerant I/O's.**
- **It has a fully operational IEEE 1149.1 JTAG boundary scan interface.**
- **On-board supply de-coupling capacitors and PLL filter network.**



ACT5260 FR4 Adapter

ACT5260 DESCRIPTION:

The ACT5260 is a highly integrated superscalar microprocessor that implements a superset of the MIPS IV Instruction Set Architecture(ISA). It has a high performance 64-bit integer unit, a high throughput, fully pipelined 64-bit floating point unit, an operating system friendly memory management unit with a 48-entry fully associative TLB, a 16 KByte 2-way set associative instruction cache, a 16 KByte 2-way set associative data cache, and a high-performance 64-bit system interface. The ACT5260 can issue both an integer and a floating point instruction in the same cycle.

The ACT5260 is ideally suited for high-end embedded control applications such as internetworking, high performance image manipulation, high speed printing, and 3-D visualization.

HARDWARE OVERVIEW

The ACT5260 offers a high-level of integration targeted at high-performance embedded applications. Some of the key elements of the ACT5260 are briefly described below.

Superscalar Dispatch

The ACT5260 has an efficient asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating-point computation instruction simultaneously. With respect to superscalar issue, integer instructions include alu, branch, load/store, and floating-point load/store, while floating-point computation instructions include floating-point add, subtract, combined multiply-add, converts, etc. In combination with its high throughput fully pipelined floating-point execution unit, the superscalar capability of the ACT5260 provides unparalleled price/performance in computationally intensive embedded applications.

CPU Registers

Like all MIPS ISA processors, the ACT5260 CPU has a simple, clean user visible state consisting of 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits.

Pipeline

For integer operations, loads, stores, and other non-floating-point operations, the ACT5260 uses the simple 5-stage pipeline also found in the circuits R4600, R4700, and R5000. In addition to this standard pipeline, the ACT5260 uses an extended seven stage pipeline for floating-point operations. Like the R5000, the ACT5260 does virtual to physical translation in parallel with cache access.

Integer Unit

Like the R5000, the ACT5260 implements the MIPS IV Instruction Set Architecture, and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I-III instruction sets. Additionally, the ACT5260 includes two implementation specific instructions not found in the baseline MIPS IV ISA but that are useful in the embedded market place. Described in detail in a later section, these instructions are integer multiply-accumulate and 3-operand integer multiply.

The ACT5260 integer unit includes thirty-two general purpose 64-bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/divide unit. Additional register resources include: the HI/LO result registers for the two-operand integer multiply/ divide operations, and the program counter(PC).

Register File

The ACT5260 has thirty-two general purpose registers with register location 0 hard wired to zero. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

ALU

The ACT5260 ALU consists of the integer adder/ subtractor, the logic unit, and the shifter. The adder performs address calculations in addition to arithmetic operations, the logic unit performs all logical and zero shift data moves, and the shifter performs shifts and store alignment operations. Each of these units is optimized to perform all operations in a single processor cycle

For Detail Information regarding the operation of the Quantum Effect Design (QED) RISCMark™ RM5260™, 64-Bit Superscalar Microprocessor see the QED datasheet.

Application Considerations:

Although the device has a 4XXX PC 179 pin PGA compatible footprint, it is not a drop-in replacement since the RM5260 has a different clocking scheme. The RM5260 does not generate the system clocks the same as the R4400, R4600 and R4700. Instead, the system clock is an input, which is multiplied up to the pipeline rate. On the adapter, the Tclock and Rclock pins are floating; not connected to anything. SYNCout and IOout are connected to ground to commit possible unconnected CMOS inputs to a level. Depending on the system configuration, accommodating the clocking difference can be as simple as a few re-routing jumpers or generating divisors of the original MasterClock and the addition of some phase-skewing buffers to emulate the Rclock and Tclock system clocks. In addition, the boot time mode bit serial stream needs to be scrutinized before plugging in a RM5260 into an R4700 or R4400 socket. The R4700 is closest to the RM5260 whereas the R4400 is quite different.

Figure 2 is an example of what had to be done to an Algorithmics P4000i (IDT79S460) Single Board Computer which was originally configured for an R4700 with a 50 MHz input clock (100 MHz pipeline) and a divide by 2 output clock (50 MHz bus rate). With three wire jumpers, the ACT5260PC-P10-POD was up and running with no changes to the boot and monitor PROM or any recompilation of application programs. In this case, the R4700's modebit stream happened to be compatible, where a board jumper used to change the output clocks (Tclock and Rclock) from divide by 2 to divide by 3 had the effect of changing the Pclock multiplier from 2 to 3, upping the pipeline rate up to 150 Mhz without changing the board oscillator.

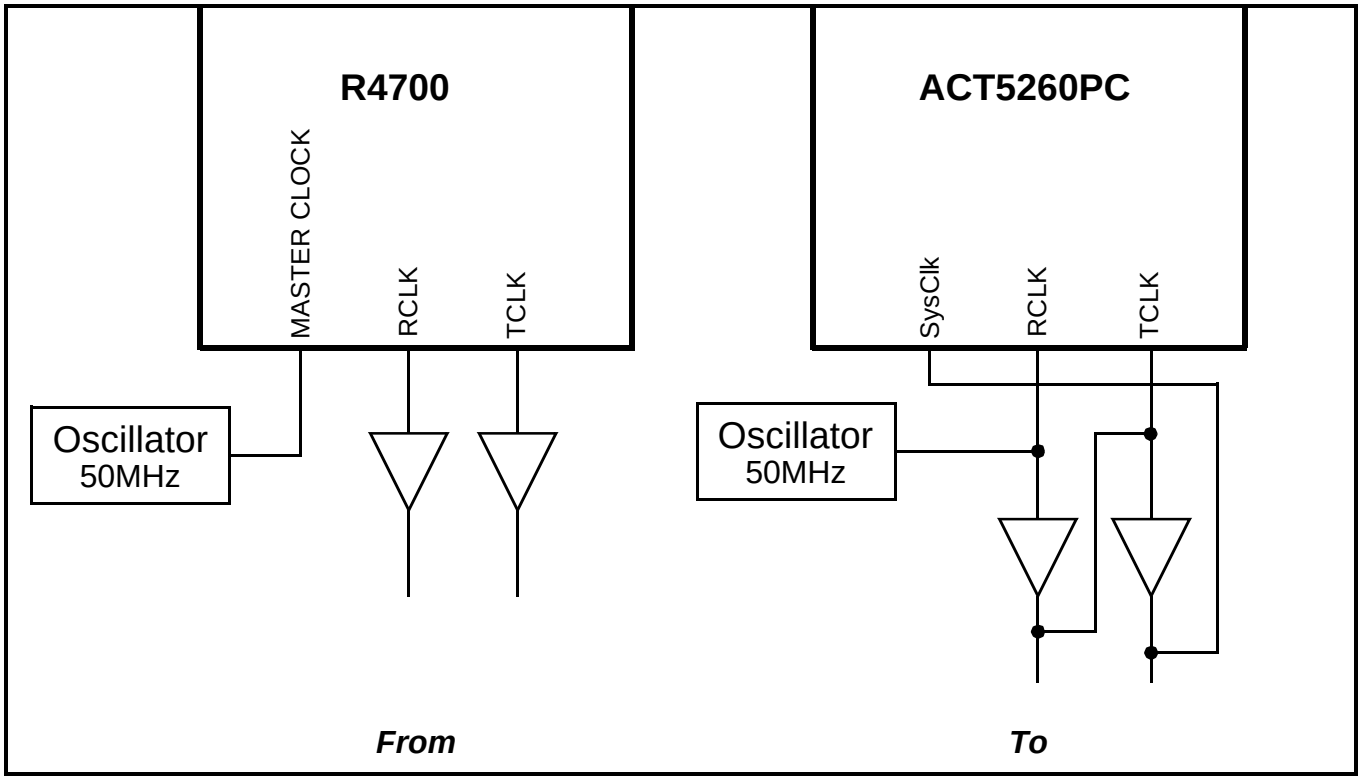


Figure 2 – Setup Example

Boot Time Mode Stream Comparison Chart – 5260 vs 4700

5260		4700	
Mode Bit	**Description**	**Mode Bit**	**Description**
0	Reserved (must be zero)	0	Reserved: Must be zero (0)
4..1	Write-back data rate 0 → DDDD 1 → DDxDDx 2 → DDxxDDxx 3 → DxDxDxDx 4 → DDxxxDDxxx 5 → DDxxxxDDxxxx 6 → DxxDxxDxxDxx 7 → DDxxxxxxDDxxxxxx 8 → DxxxDxxxDxxxDxxx 9–15 reserved	4..1	Write-back data rate 0 → D 1 → DDx 2 → DDxx 3 → DxDx 4 → DDxxx 5 → DDxxxx 6 → DxxDxx 7 → DDxxxxxx 8 → DxxxDxxx 9–15 reserved
7..5	Pclock to SysClock Multiplier 0 → Multiply by 2, 1 → Multiply by 3 2 → Multiply by 4, 3 → Multiply by 5 4 → Multiply by 6, 5 → Multiply by 7 6 → Multiply by 8, 7 reserved	7..5	Clock divisor 0 → 2,1 → 3 2 → 4, 3 → 5 4 → 6, 5 → 7 6 → 8, 7 → reserved
8	Specifies byte ordering. Logically ORed with BigEndian input signal. 0 → Little endian 1 → Big endian	8	0 → Little endian 1 → Big endian
10..9	00 → R4000 compatible non-block writes, 01 → reserved, 10 → pipelined non-block writes, 11 → non-block write re-issue	10..9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue
11	0 → Enable the timer interrupt on Int[5], 1 → Disable the timer interrupt on Int[5].	11	0 → Enable the timer interrupt on Int[5], 1 → Disable the timer interrupt on Int[5].
12	Reserved: Must be zero (0)	12	Reserved: Must be zero (0)
14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)	14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)
15	Reserved: Must be zero (0)	15	0 ⇒ TClock[0] enabled, 1 ⇒ TClock[0] disabled
17..16	System configuration identifiers - software visible in processor Config[21..20]	16	0 ⇒ TClock[1] enabled, 1 ⇒ TClock[1] disabled
		17	0 ⇒ RClock[0] enabled, 1 ⇒ RClock[0] disabled
18	0 → Set Timer/Counter to run at Pclock/2 1 → Set Timer/Counter to run at Pclock	18	0 ⇒ RClock[1] enabled, 1 ⇒ RClock[1] disabled
21..19	Reserved: Must be zero (0)	255..19	Reserved: Must be zero (0)
24..22	Write address to write data delay in P cycles 000 → 0 cycles(R5000), ..., 111 → 7 cycles		
255..25	Reserved: Must be zero (0)		

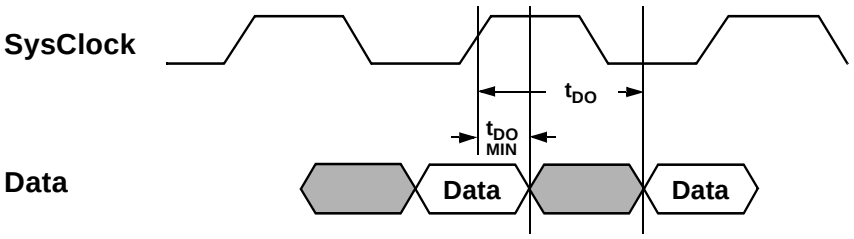


Figure 3 – Output Timing

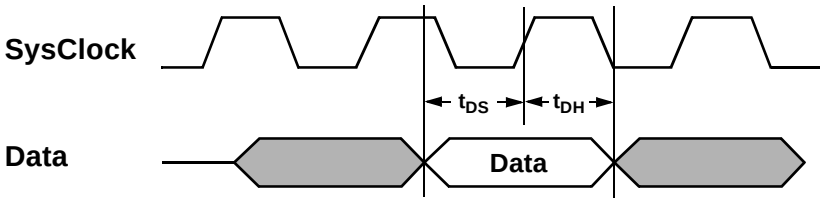


Figure 4 – Input Timing

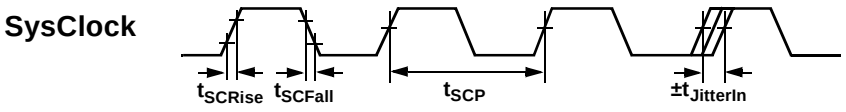


Figure 5 – SysClock Timing

Absolute Maximum Ratings[1]

Symbol	Rating	Range	Units
V_{TERM}	Terminal Voltage with respect to GND	-0.5[2] to 4.6	V
T_{CASE}	Operating Temperature	0 to +85	°C
T_{BIAS}	Case Temperature under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{IN}	DC Input Current	20[3]	mA
I_{OUT}	DC Output Current	50	mA

Notes:
1. Stresses above those listed under "AbsoluteMaximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VIN minimum = -2.0V for pulse width less than 15nS. VIN maximum should not exceed +5.5 Volts.
3. When VIN < 0V or VIN > Vcc.
4. No more than one output should be shorted at one time. Duration of the short should not exceed more than 30 second.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+3.135	+3.465	V
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	$0.2V_{CC}$	V
T_C	Operating Temperature Case (Commercial)	0	+85	°C

DC Characteristics

(VCC = 3.3V ±5%; TCASE = 0°C to +85°C)

Parameter	Sym	Conditions	133 / 150MHz		Units
			Min	Max	
Output Low Voltage	V_{OL1}	I_{OL} = 20 µA		0.1	V
Output High Voltage	V_{OH1}	I_{OL} = 20 µA	Vcc - 0.1		V
Output Low Voltage	V_{OL2}	I_{OL} = 4 mA		0.4	V
Output High Voltage	V_{OH2}	I_{OL} = 4 mA	2.4		V
Input High Voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}		-0.5	$0.2V_{CC}$	V
Input Current	I_{IN1}	V_{IN} = 0V	-20	+20	µA
Input Current	I_{IN2}	V_{IN} = V_{CC}	-20	+20	µA
Input Current	I_{IN3}	V_{IN} = 5.5V	-250	+250	µA
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF

Power Consumption

Parameter	Symbol	Conditions	133MHz, 3.3V		150MHz, 3.3V		Units
			Typ[5]	Max	Typ[5]	Max	
Active Operating Supply Current	I_{CC1}	C_L = 0pF, 150/75MHz, No SysAD activity	TBD	TBD	TBD	TBD	mA
	I_{CC2}	C_L = 50pF, 150/75MHz, R4000 write protocol without FPU operation	1000	1750	1150	1950	mA
	I_{CC3}	C_L = 50pF, 150/75MHz, write re-issue or pipelined writes	1100	2000	1250	2250	mA
Standby Current	I_{SB1}	C_L = 0pF, 150/75MHz		TBD		TBD	mA
	I_{SB1}	C_L = 50pF, 150/75MHz		TBD		TBD	mA

Notes:
5. Typical integer instruction mix and cache miss rates.

AC Characteristics
(V_{CC} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Capacitive Load Deration

Symbol	Parameter	133 / 150MHz		Units
		Minimum	Maximum	
C_{LD}	Load Derate		2	ns/25pF

Clock Parameters

Parameter	Symbol	Test Conditions	133/150MHz		Units
			Min	Max	
SysClock High	t_{SCHigh}	Transition ≤ 5ns	4		ns
SysClock Low	t_{SCLow}	Transition ≤ 5ns	4		ns
SysClock Frequency[6]			33	75	MHz
SysClock Period	t_{SCP}			30	ns
Clock Jitter for SysClock	$t_{JitterIn}$			±250	ps
SysClock Rise Time	t_{SCRise}			5	ns
SysClock Fall Time	t_{SCFall}			5	ns
ModeClock Period	$t_{ModeCKP}$			$256*t_{SCP}$	ns
JTA Clock Period	$t_{JTAGCKP}$			$4*t_{SCP}$	ns

Notes:
6. Operation of the ACT5260 is only guaranteed with the Phase Loop enabled.

System Interface Parameters[7]

Parameter	Symbol	Test Conditions	133MHz		150MHz		Units
			Min	Max	**Min**	Max	
Data Output[8]	t_{DO}	$mode_{14...13}$ = 10 (fastest)	TBD	TBD	TBD	TBD	ns
		$mode_{14...13}$ = 11	TBD	TBD	TBD	TBD	ns
		$mode_{14...13}$ = 00	1.0	8.0	1.0	8.0	ns
		$mode_{14...13}$ = 01 (slowest)	TBD	TBD	TBD	TBD	ns
Data Setup	t_{DS}	t_{RISE} = 5ns	4.0		4.0		ns
Data Hold	t_{DH}	t_{FALL}= 5ns	0		0		ns

Notes:
7. Timmings are are measured from from 1.5V of the clock to 1.5V of the signal.
8. Capacitive load for all output timing is 50pF.

Boot Time Interface Parameters

Parameter	Symbol	Test Conditions	133/150MHz		Units
			Min	Max	
Mode Data Setup	t_{DS}		4		SysClock cycles
Mode Data Hold	t_{DH}		0		SysClock cycles

ACT5260PC Adapter Pinouts

4XXX Signal	PGA Pin	5260 Pin	4XXX Signal	PGA Pin	5260 Pin	4XXX Signal	PGA Pin	5260 Pin
INT0	N2	93	SYSAD45	B17	37	VCC	A13	VCC
INT1	L3	94	SYSAD46	E17	39	VCC	A16	VCC
INT2	K3	95	SYSAD47	F17	43	VCC	B18	VCC
INT3	J3	96	SYSAD48	L2	115	VCC	C1	VCC
INT4	H3	97	SYSAD49	M3	119	VCC	D18	VCC
INT5	F2	98	SYSAD5	C4	8	VCC	F1	VCC
IOIN	T13	NC	SYSAD50	N3	121	VCC	G18	VCC
IOOUT	U12	GND	SYSAD51	R2	125	VCC	H1	VCC
JTCK	H17	49	SYSAD52	T3	129	VCC	J18	VCC
JTDI	G16	48	SYSAD53	U3	131	VCC	K1	VCC
JTDO	F16	47	SYSAD54	T6	135	VCCP	K17	64
JTMS	E16	50	SYSAD55	T7	139	VCC	L18	VCC
MODECLK	B4	46	SYSAD56	T10	141	VCC	M1	VCC
MODEIN	U4	58	SYSAD57	T11	145	VCC	N18	VCC
MSTRCLK	J17	66[1]	SYSAD58	U13	149	VCC	R1	VCC
MSTROUT	P17	NC	SYSAD59	V15	151	VCC	T18	VCC
RCLK0	T17	NC	SYSAD6	B5	12	VCC	U1	VCC
RCLK1	R16	NC	SYSAD60	T15	164	VCC	V3	VCC
SYNCIN	J16	NC	SYSAD61	U17	166	VCC	V6	VCC
SYNCOUT	P16	GND	SYSAD62	N16	170	VCC	V8	VCC
SYSAD0	J2	189	SYSAD63	N17	174	VCC	V10	VCC
SYSAD1	G2	193	SYSAD7	B6	16	VCC	V12	VCC
SYSAD10	C12	26	SYSAD8	B9	18	VCC	V14	VCC
SYSAD11	B14	28	SYSAD9	B11	22	VCC	V17	VCC
SYSAD12	B15	32	SYSADC0	C8	183	VCC	T9	VCC
SYSAD13	C16	36	SYSADC1	G17	187	GND	A3	GND
SYSAD14	D17	38	SYSADC2	T8	175	GND	A6	GND
SYSAD15	E18	42	SYSADC3	L16	179	GND	A8	GND
SYSAD16	K2	114	SYSADC4	B8	184	GND	A10	GND
SYSAD17	M2	118	SYSADC5	H16	188	GND	A12	GND
SYSAD18	P1	120	SYSADC6	U8	176	GND	A14	GND
SYSAD19	P3	124	SYSADC7	L17	180	GND	A17	GND
SYSAD2	E1	197	SYSCMD0	E2	73	GND	A18	GND
SYSAD20	T2	128	SYSCMD1	D3	74	GND	B1	GND
SYSAD21	T4	130	SYSCMD2	B2	75	GND	C18	GND
SYSAD22	U5	134	SYSCMD3	A5	76	GND	D1	GND
SYSAD23	U6	138	SYSCMD4	B7	79	GND	F18	GND
SYSAD24	U9	140	SYSCMD5	C9	80	GND	G1	GND
SYSAD25	U11	144	SYSCMD6	B10	83	GND	H18	GND
SYSAD26	T12	148	SYSCMD7	B12	84	GND	J1	GND
SYSAD27	U14	150	SYSCMD8	C13	85	VSSP	K16	65
SYSAD28	U15	163	SYSCMDP	C14	86	GND	K18	GND
SYSAD29	T16	165	TCLK0	C17	NC	GND	L1	GND
SYSAD3	E3	199	TCLK1	D16	NC	GND	M18	GND
SYSAD30	R17	169	VCCOK	M17	110	GND	N1	GND
SYSAD31	M16	173	CLDRST	T14	109	GND	P18	GND
SYSAD32	H2	190	EXTRQST	U2	107	GND	R18	GND
SYSAD33	G3	194	FAULT	B16	NC	GND	T1	GND
SYSAD34	F3	198	NMI	U7	106	GND	U18	GND
SYSAD35	D2	200	RDRDY	T5	59	GND	V1	GND
SYSAD36	C3	7	RELEASE	V5	63	GND	V2	GND
SYSAD37	B3	9	RESET	U16	108	GND	V4	GND
SYSAD38	C6	13	VALIDOUT	R3	62	GND	V7	GND
SYSAD39	C7	17	VALIDIN	P2	61	GND	V9	GND
SYSAD4	C2	6	WRRDY	C5	60	GND	V11	GND
SYSAD40	C10	19	VCC	A2	VCC	GND	V13	GND
SYSAD41	C11	23	VCC	A4	VCC	GND	V16	GND
SYSAD42	B13	27	NC	A7	NC	GND	V18	GND
SYSAD43	A15	29	VCC	A9	VCC	GND		111[2]
SYSAD44	C15	33	VCC	A11	VCC	NC	U10	NC

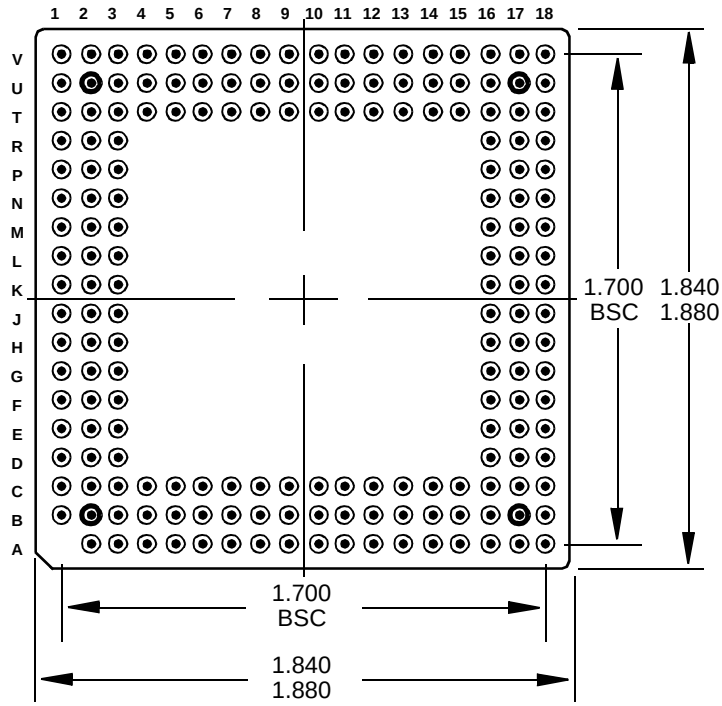
Notes: 1. 5260 pin function SysClk 2. 5260 pin function BigEndian

Ordering Information

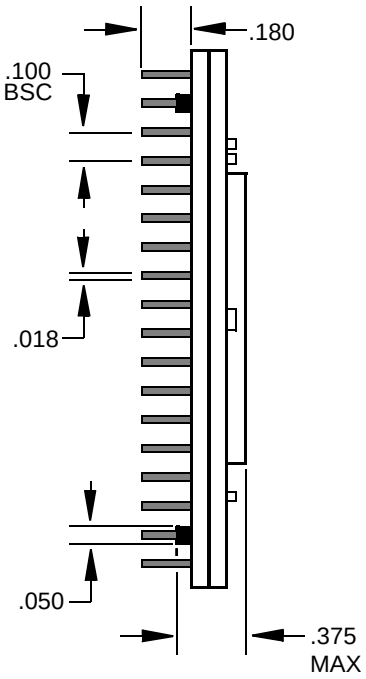
Model Number
ACT5260PC-P10-POD

Package Outline

Bottom View



Side View



Specification subject to change without notice

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