ACT8503
Radiation Hardened & ESD Protected 48-Channel Analog Multiplexer Module

AEROFLEX
CIRCUIT TECHNOLOGY
www.aeroflex.com

Features

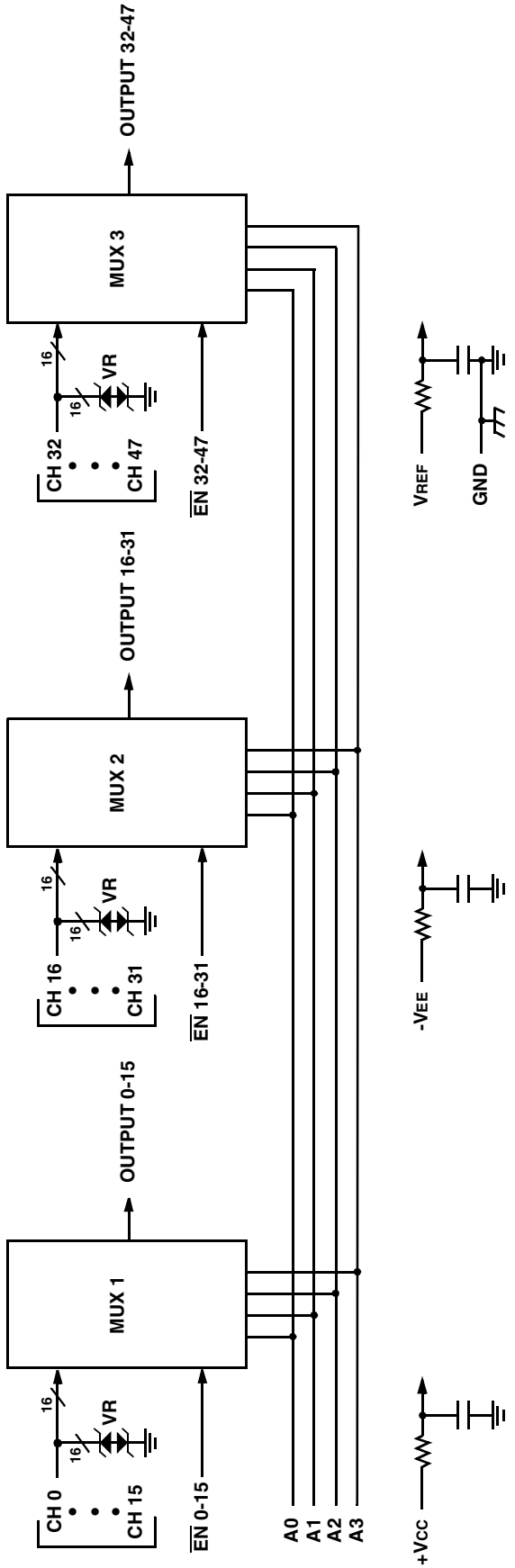
- **Radiation Environment**
  - **Radiation 300K(Si) Total Dose**
  - **No Latch-Up or SEE to 120MeV/cm^2/mg**
- **Full Military Temperature Range**
- **Low Power Consumption < 90mW**
- **48 Channels Provided by three (3) HS-1840RH Multiplexers**
- **One Address Bus (A0 - A3) and Three Enable Lines**
- **All Channel Inputs protected by ±20V Transorbs**
- **Fast Access Time 1500ns**
- **±35V Input Over Voltage Protection (Power On or Off)**
- **Break-Before-Make Switching**
- **High Analog Input Impedance (Power On or Off)**
- **Dielectrically Isolated Device Islands**
- **No Latch-Up**
- **Packaging – Hermetic Ceramic Quad Flat Pack**
  - **96 Leads, 1.32"Sq x .20"Ht Quad Flat Pack**
  - **Typical Weight 15 grams**
- **DESC SMD Pending**

AEROFLEX LABS INC. ISO 9001 CERTIFIED

General Description

Aeroflex's ACT8503 is a radiation hardened, multi-chip 48 channel multiplexer MCM (multi-chip module) with ESD protection for use in space applications. All channel inputs have electrostatic discharge protection.

The ACT8503 has been specifically designed to meet exposure to radiation environments. The multiplexer is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (QFP) and is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the ACT8503 is ideal for demanding military and space applications.



ACT8503 48 Channel Analog MUX Block Diagram

Organization and Application

The ACT8503 consists of three 16 channel muxes arranged as shown in the Block Diagram. The Address Bus and three Enable lines providing for 48 channels addressable by Bus A_0~A_3, in three 16 channel blocks, each block enabled separately. Each block connects the addressed channel to one output.

The ACT8503 design is inherently Radiation Hard due to the HS1840RH Multiplexers as well as Microsemi Corp. Transient Suppressors (Reference Microsemi MicroNotes Series 050 - page 14).

NOTE: It is recommended that all "NC or "no connect pin", be grounded. This eliminates or minimizes any ESD or static buildup.

Absolute Maximum Ratings 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-55 to +150	°C
Supply Voltage +V_{DD} (Pin 44) -V_{EE} (Pin 46) V_{REF} (Pin 48)	 +20 -20 +20	 V V V
Digital Input Overvoltage V_{EN} (Pins 5, 91, 92), V_A (Pins 1, 3, 95, 93)	 < V_R +4 > GND -4	 V V
Analog Input Over Voltage V_S	 ±18	 V

Notes:

1/ All measurements are made with respect to ground.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
+V_{CC}	+15V Power Supply Voltage	+15.0	V
-V_{EE}	-15V Power Supply Voltage	-15.0	V
V_{REF}	Reference Voltage	+5.00	V
V_{AL}	Logic Low Level	+0.8	V
V_{AH}	Logic High Level	+4.0	V

DC Electrical Performance Characteristics 1/

(T_C = -55°C to +125°C, +V_{CC} = +15V, -V_{EE} = -15V, V_{REF} = +5.0V, Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Supply Current	I+	$V_{EN(0-47)}$ = $V_{A(0-3)}$ = 0	0	1.5	mA
	I-	$V_{EN(0-47)}$ = $V_{A(0-3)}$ = 0	-1.5	0	mA
	+I_{SBY}	$V_{EN(0-47)}$ = 4V, $V_{A(0-3)}$ = 0 6/	0	1.5	mA
	-I_{SBY}	$V_{EN(0-47)}$ = 4V, $V_{A(0-3)}$ = 0 6/	-1.5	0	mA
Address Input Current	$I_{AL(0-3)}$	V_A = 0V 1/	-3	3	µA
	$I_{AH(0-3)}$	V_A = 5V 1/	-3	3	µA
Enable Input Current	$I_{ENL(0-47)}$	$V_{EN(0-47)}$ = 0V	-1.5	1.5	µA
	$I_{ENH(0-47)}$	$V_{EN(0-47)}$ = 5V	-1.5	1.5	µA
Positive Input Leakage Current CH0-CH47	+$I_{SOFFOUTPUT(ALL)}$	V_{IN} = +10V, V_{EN} = 4V, output and all unused MUX inputs under test = -10V 2/, 3/	-100	+700	nA

DC Electrical Performance Characteristics 1/ (con't)

(Tc = -55°C to +125°C, +VCC = +15V, -VEE = -15V, VREF = +5.0V, Unless otherwise specified)

Parameter	Symbol	Conditions		Min	Max	Units
Negative Input Leakage Current CH0-CH47	-ISOFFOUTPUT(ALL)	VIN = -10V, VEN = 4V, output and all unused MUX inputs under test = +10V 2/, 3/		-100	+700	nA
Output Leakage Current OUTPUTS (pins 25, 70 & 68)	+IDOFFOUTPUT(ALL)	VOUT = +10V, VEN = 4V, output and all unused MUX inputs under test = -10V 3/, 4/		-100	+100	nA
Output Leakage Current OUTPUTS (pins 25, 70 & 68)	-IDOFFOUTPUT(ALL)	VOUT = -10V, VEN = 4V, output and all unused MUX inputs under test = +10V 3/, 4/		-100	+100	nA
Input Clamped Voltage CH0 - CH47	+VCLMP(0-47)	VEN = 4V, all unused MUX inputs under test are open. 3/	+25°C +125°C -55°C	18.0 18.0 17.5	23.0 23.5 22.5	V V V
Input Clamped Voltage CH0 - CH47	-VCLMP(0-47)		+25°C +125°C -55°C	-23.0 -23.5 -22.5	-18.0 -18.0 -17.5	V V V
Switch ON Resistance OUTPUTS (pins 25, 70 & 68)	$R_{DS(ON)(0-47)_A}$	VIN = +15V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/		500	3000	Ω
	$R_{DS(ON)(0-47)_B}$	VIN = +5V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/		500	3000	Ω
	$R_{DS(ON)(0-47)_C}$	VIN = -5V, VEN = 0.8V, IOUT = +1mA 2/, 3/, 5/		500	3000	Ω

Notes:

1/ Measure inputs sequentially. Ground all unused inputs of the MUX under test. VA is the applied input voltage to the MUXes' address lines A(0-3).

2/ VIN is the applied input voltage to the MUXes' input channel CH0-CH47.

3/ VEN is the applied input voltage to the MUXes' enable line En(0-15), En(16-31) and En(32-47).

4/ VOUT is the applied input voltage to the MUXes' output line OUTPUT(0-15), OUTPUT(16-31) and OUTPUT(32-47).

5/ Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.

6/ If not tested, shall be guaranteed to the specified limits.

Switching Characteristics

(Tc = -55°C to +125°C, VDD = +15V, VEE = -15V, VR = +5.0V, Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Switching Test MUX	t_{ONA}	RL = 10KΩ, CL = 50pF	10	1500	ns
	t_{OFFA}	RL = 10KΩ, CL = 50pF	10	2000	ns
	t_{ONEN}	RL = 1KΩ, CL = 50pF	10	1500	ns
	t_{OFFEN}	RL = 1KΩ, CL = 50pF	10	1000	ns

Truth Table (CH0 – CH15)

A3	A2	A1	A0	EN(0-15)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between CH0-15 and OUTPUT (0-15)

Truth Table (CH16 – CH31)

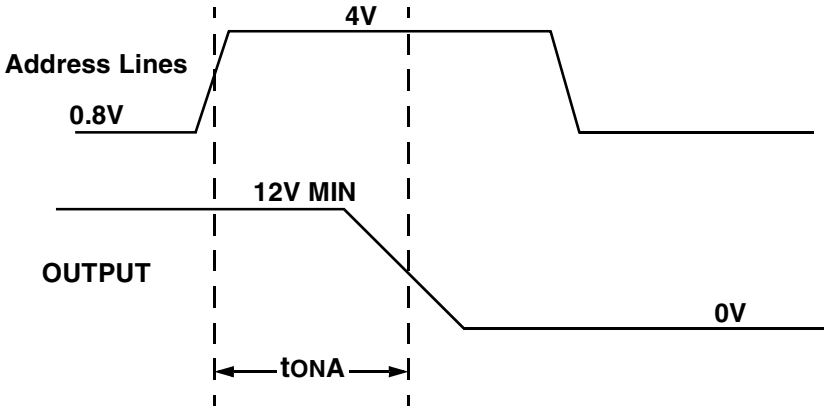
A3	A2	A1	A0	EN(16-31)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

1/ Between CH16-31 and OUTPUT (16-31)

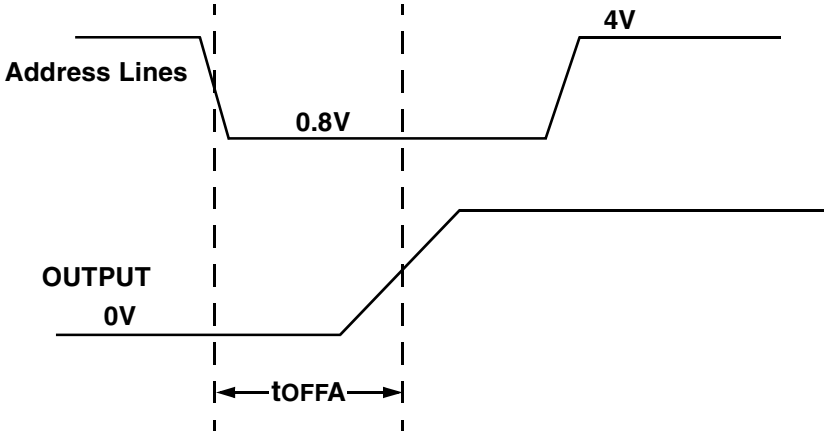
Truth Table (CH32 – CH47)

A3	A2	A1	A0	EN(32-47)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH32
L	L	L	H	L	CH33
L	L	H	L	L	CH34
L	L	H	H	L	CH35
L	H	L	L	L	CH36
L	H	L	H	L	CH37
L	H	H	L	L	CH38
L	H	H	H	L	CH39
H	L	L	L	L	CH40
H	L	L	H	L	CH41
H	L	H	L	L	CH42
H	L	H	H	L	CH43
H	H	L	L	L	CH44
H	H	L	H	L	CH45
H	H	H	L	L	CH46
H	H	H	H	L	CH47

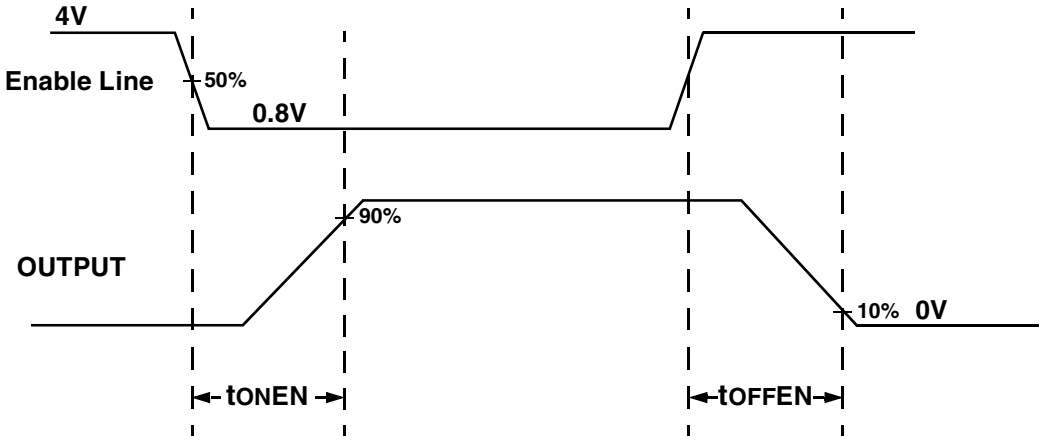
1/ Between CH32-47 and OUTPUT (32-47)



Definition of t_{ONA}



Definition of t_{OFFA}



Definition of t_{ONEN} and t_{OFFEN}

Lead Numbers & Functions

ACT8503 – 96 Leads Ceramic QUAD Flat Pack					
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
1	A_2	33	CH11	65	CH33
2	NC	34	NC	66	CH32
3	A_3	35	CH12	67	NC
4	NC	36	NC	68	Output V(32-47)
5	$\overline{EN}$ 0-15	37	CH13	69	NC
6	NC	38	NC	70	Output V(16-31)
7	CH0	39	CH14	71	GND
8	NC	40	NC	72	GND
9	CH1	41	CH15	73	CH31
10	NC	42	NC	74	CH30
11	CH2	43	NC	75	CH29
12	NC	44	$+V_{CC}$	76	CH28
13	CH3	45	NC	77	CH27
14	NC	46	$-V_{EE}$	78	CH26
15	CH4	47	NC	79	CH25
16	NC	48	V_{REF}	80	CH24
17	CH5	49	NC	81	CH23
18	NC	50	CASE GND	82	CH22
19	CH6	51	CH47	83	CH21
20	NC	52	CH46	84	CH20
21	CH7	53	CH45	85	CH19
22	NC	54	CH44	86	CH18
23	GND	55	CH43	87	CH17
24	GND	56	CH42	88	CH16
25	Output V(0-15)	57	CH41	89	GND
26	NC	58	CH40	90	GND
27	CH8	59	CH39	91	$\overline{EN}$ 32-47
28	NC	60	CH38	92	$\overline{EN}$ 16-31
29	CH9	61	CH37	93	A_0
30	NC	62	CH36	94	NC
31	CH10	63	CH35	95	A_1
32	NC	64	CH34	96	NC

NOTE: It is recommended that all "NC or "no connect pin", be grounded. This eliminates or minimizes any ESD or static buildup.

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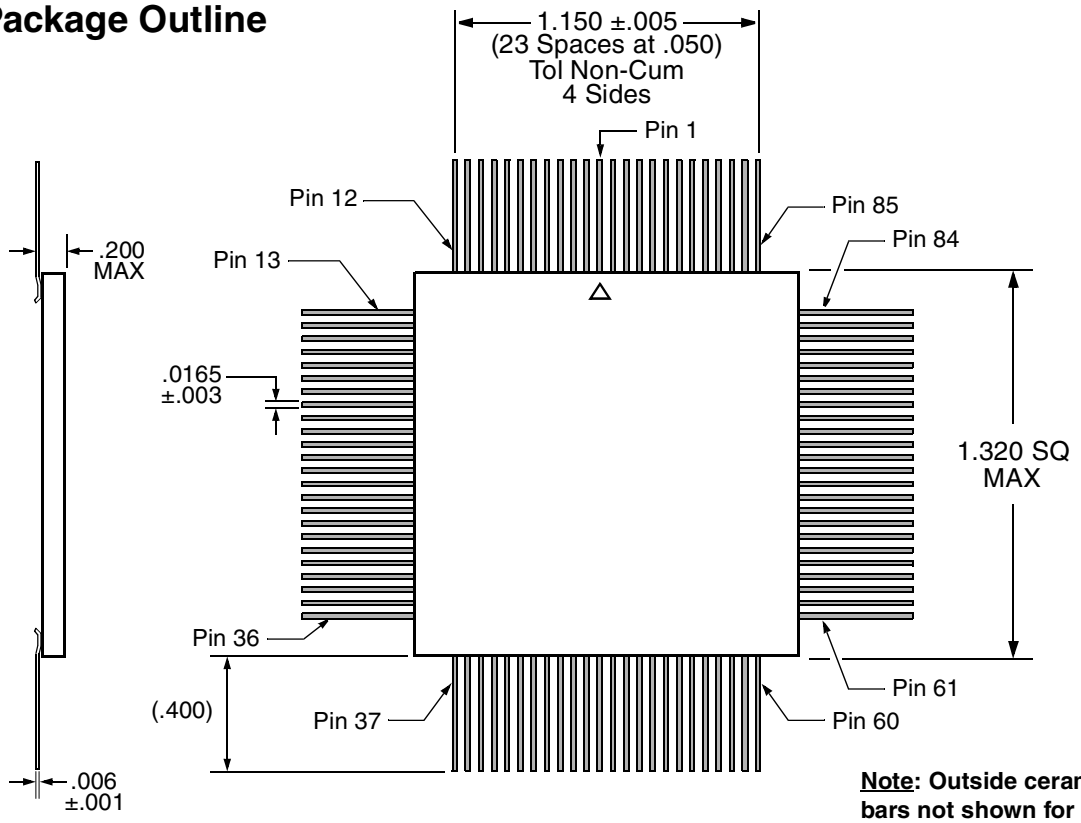
Ordering Information

Model Number	Screening	DESC SMD #	Package
ACT8503-S	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883 IAW MIL-PRF-38534 Class K	Pending	QUAD Flat Pack
ACT8503	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883 IAW MIL-PRF-38534 Class H		
ACT8503-7	Commercial Flow, +25°C testing only	NA	
ACT8503-T	Commercial Flow, -55°C to +125°C testing only		
ACT8503-I	Commercial Flow, -40°C to +85°C testing only		
ACT8503-C	Commercial Flow, -0°C to +70°C testing only		

Flat Package Outline



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details

Specifications subject to change without notice

Aeroflex Circuit Technology
35 South Service Road
Plainview New York 11803
www.aeroflex.com

Telephone: (516) 694-6700
FAX: (516) 694-6715
Toll Free Inquiries: (800) THE-1553
E-Mail: sales-act@aeroflex.com