

## ACTS161MS

Radiation Hardened 4-Bit Synchronous Counter

FN4095  
Rev.0.00  
January 1996

### Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96716 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose >300K RAD (Si)
- Single Event Upset (SEU) Immunity:  $<1 \times 10^{-10}$  Errors/Bit/Day (Typ)
- SEU LET Threshold >100 MEV-cm<sup>2</sup>/mg
- Dose Rate Upset >10<sup>11</sup> RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability >10<sup>12</sup> RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current  $\leq 1\mu\text{A}$  at VOL, VOH
- Fast Propagation Delay 25ns (Max), 16ns (Typ)

### Description

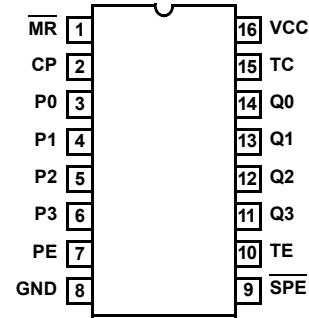
The Intersil ACTS161MS is a Radiation Hardened 4-Bit Binary Synchronous Counter, featuring asynchronous reset and load ahead carry logic. The MR is an active low master reset. SPE is an active low Synchronous Parallel Enable which disables counting and allows data at the preset inputs (P0 - P3) to load the counter. CP is the positive edge clock. TC is the terminal count or carry output. Both TE and PE must be high for counting to occur, but are irrelevant to loading. TE low will keep TC low.

The ACTS161MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

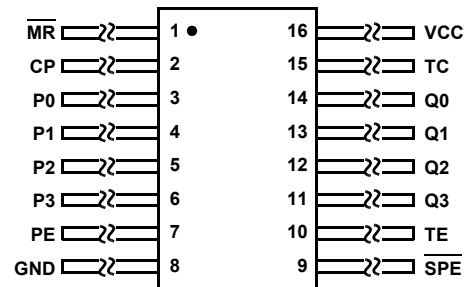
The ACTS161MS is supplied in a 16 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

### Pinouts

16 PIN CERAMIC DUAL-IN-LINE  
MIL-STD-1835, DESIGNATOR CDIP2-T16,  
LEAD FINISH C  
TOP VIEW



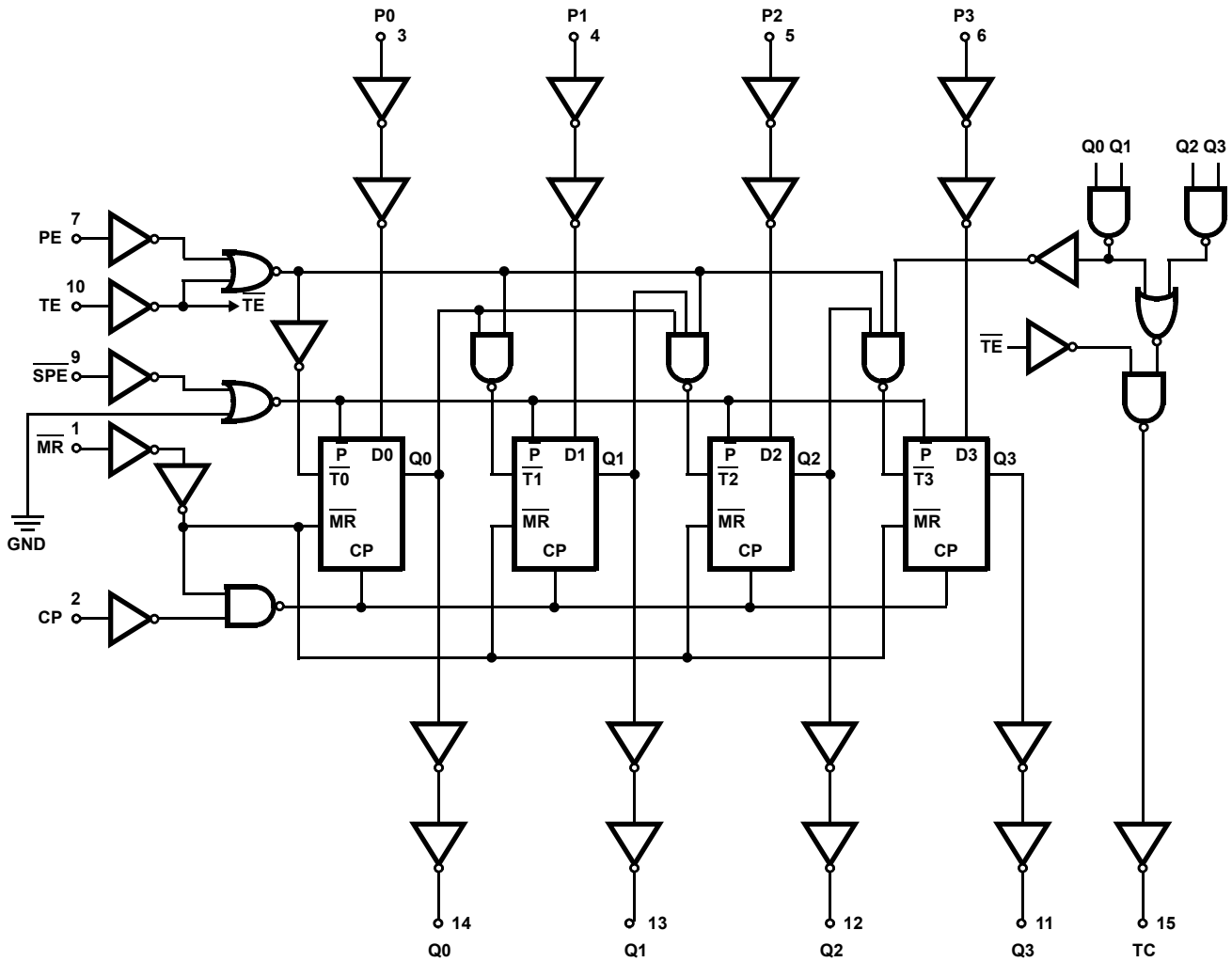
16 PIN CERAMIC FLATPACK  
MIL-STD-1835, DESIGNATOR CDFP4-F16,  
LEAD FINISH C  
TOP VIEW



### Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9671601VEC	-55°C to +125°C	MIL-PRF-38535 Class V	16 Lead SBDIP
5962F9671601VXC	-55°C to +125°C	MIL-PRF-38535 Class V	16 Lead Ceramic Flatpack
ACTS161D/Sample	25°C	Sample	16 Lead SBDIP
ACTS161K/Sample	25°C	Sample	16 Lead Ceramic Flatpack
ACTS161HMSR	25°C	Die	Die

**Functional Diagram**



**TRUTH TABLE**

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{\text{MR}}$	CP	PE	TE	$\overline{\text{SPE}}$	$P_N$	$Q_N$	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H		X	X	l	l	L	L
	H		X	X	l	h	H	(Note 1)
Count	H		h	h	h (Note 3)	X	count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	$q_N$	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	$q_N$	L

H = High Steady State, L = Low Steady State, h = High voltage level one setup time prior to the Low-to-High clock transition, l = Low voltage level one setup time prior to the Low-to-High clock transition, X = Don't Care,  $q_N$  = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition, = Low-to-High Transition.

**NOTES:**

1. The TC output is High when TE is High and the counter is at Terminal Count (HHHH).
2. The High-to-Low transition of PE or TE should only occur while CP is High for conventional operation.
3. The Low-to-High transition of SPE should only occur while CP is High for conventional operation.

### Die Characteristics

**DIE DIMENSIONS:**

88 mils x 88 mils  
 2240mm x 2240mm

**METALLIZATION:**

Type: AlSi  
 Metal 1 Thickness:  $7.125k\text{\AA} \pm 1.125k\text{\AA}$   
 Metal 2 Thickness:  $9k\text{\AA} \pm 1k\text{\AA}$

**GLASSIVATION:**

Type: SiO<sub>2</sub>  
 Thickness:  $8k\text{\AA} \pm 1k\text{\AA}$

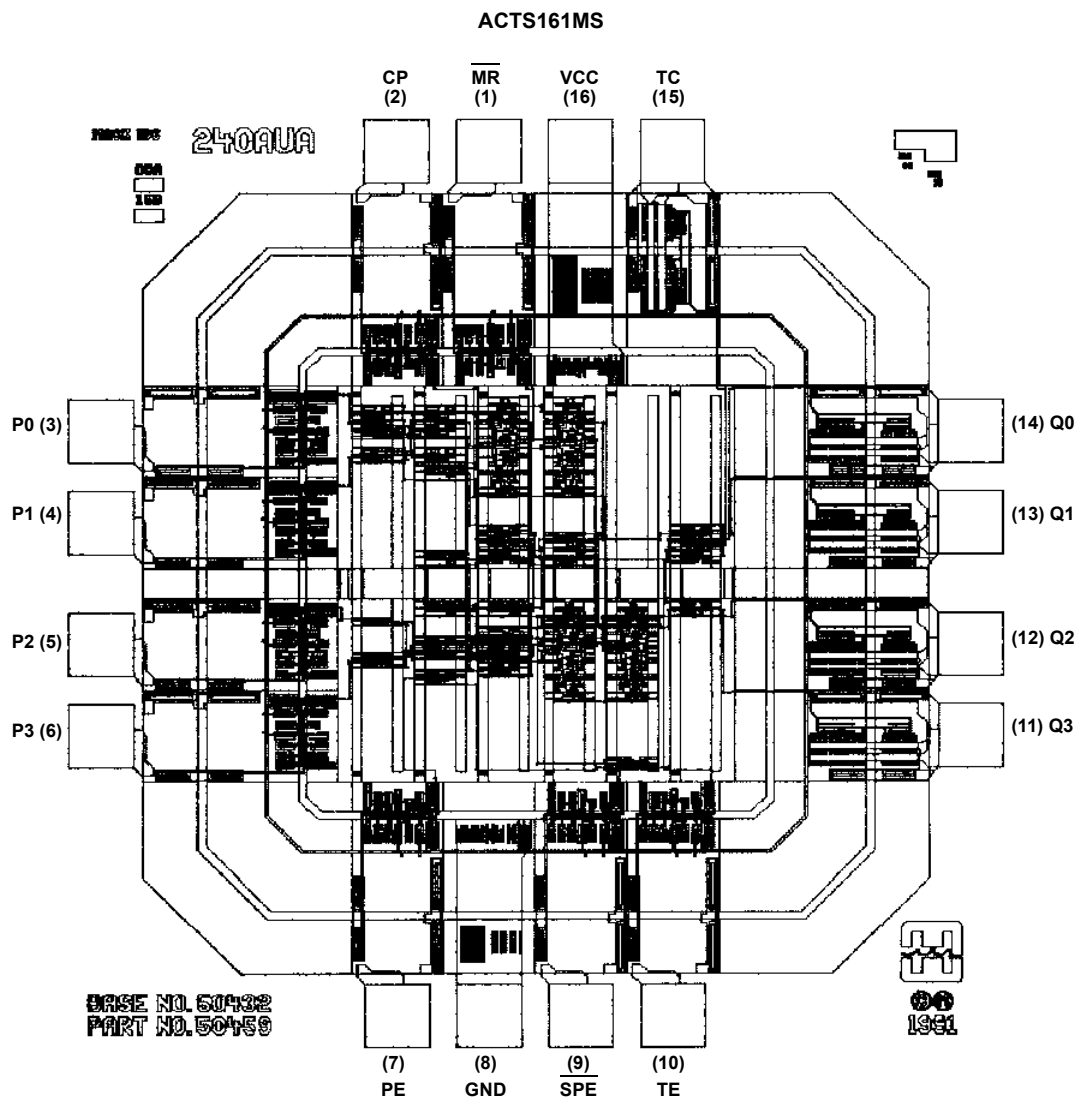
**WORST CASE CURRENT DENSITY:**

$< 2.0 \times 10^5 \text{A/cm}^2$

**BOND PAD SIZE:**

110μm x 110μm  
 4.3 mils x 4.3 mils

### Metalization Mask Layout



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