

ACTS573MS

Radiation Hardened Octal Three-State Transparent Latch

January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96725 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Single Event Upset (SEU) Immunity: <1 x 10⁻¹⁰ Errors/Bit/Day (Typ)

- Latch-Up Free Under Any Conditions
- Military Temperature Range-55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- Input Logic Levels
 - VIL = 0.8V Max
 - VIH = VCC/2 Min
- Input Current \leq 1µA at VOL, VOH

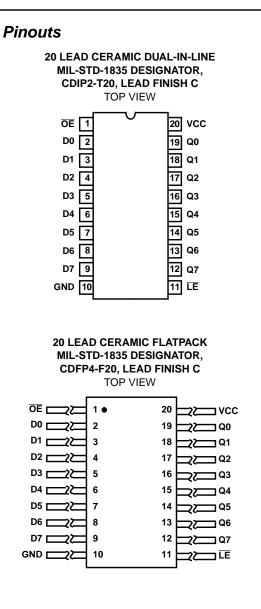
• Fast Propagation Delay 18ns (Max), 12ns (Typ)

Description

The Intersil ACTS573MS is a Radiation Hardened Octal Transparent Latch with an active low output enable. The outputs are transparent to the inputs when the latch enable ($\overline{\text{LE}}$) is High. When the latch goes low the data is latched. The output enable controls the three-state outputs. When the output enable pins ($\overline{\text{OE}}$) are high the output is in a high impedance state. The latch operation is independent of the state of output enable.

The ACTS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

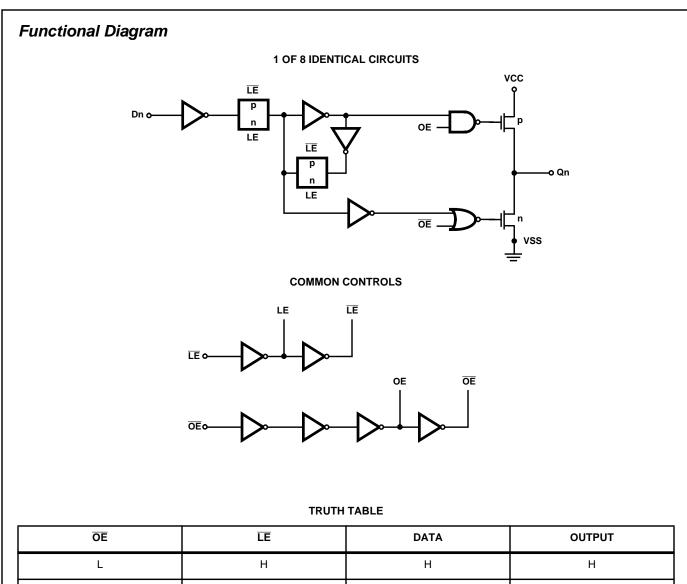
The ACTS573MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line package (D suffix).



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9672501VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9672501VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACTS573D/Sample	25°C	Sample	20 Lead SBDIP
ACTS573K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACTS573HMSR	25°C	Die	Die

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. 1-888-INTERSIL or 321-724-7143 | Copyright © Intersil Corporation 1999



ŌE	LE	DATA	OUTPUT
L	Н	Н	н
L	Н	L	L
L	L	I	L
L	L	h	н
Н	Х	Х	Z

NOTE: L = Low Logic Level, H = High Logic Level, X = Don't Care, Z = High Impedance, I = Low Voltage Level Prior to High-to-Low Latch Enable Transition, h = High Voltage Level Prior to High-to-Low Latch Enable Transition.

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Die Characteristics

DIE DIMENSIONS:

102 mils x 102 mils 2,600mm x 2,600mm

METALLIZATION:

Type: AlSi Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO₂ Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

 $<2.0 \text{ x} 10^5 \text{ A/cm}^2$

BOND PAD SIZE:

> 4.3 mils x 4.3 mils

> 110µm x 110µm

Metallization Mask Layout



