ACTS630MS

Radiation Hardened EDAC (Error Detection and Correction)

FN3204
Rev 1.00
January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96721 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
- SEU LET Threshold>100 MEV-cm^2/mg
- Dose Rate Upset>10^{11} RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability>10^{12} RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range-55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay37ns (Max), 24ns (Typ)

Description

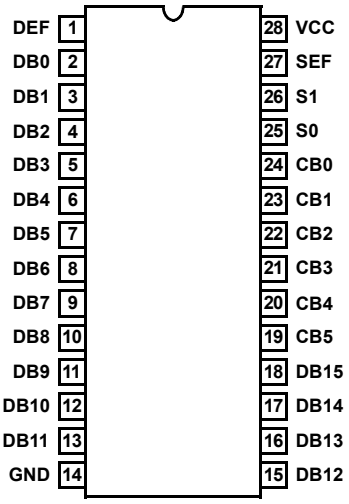
The Intersil ACTS630MS is a Radiation Hardened 16-bit parallel error detection and correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle; during a memory read cycle a 22-bit word is taken form memory and checked for errors. Single bit errors in the data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

The ACTS630MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic Family.

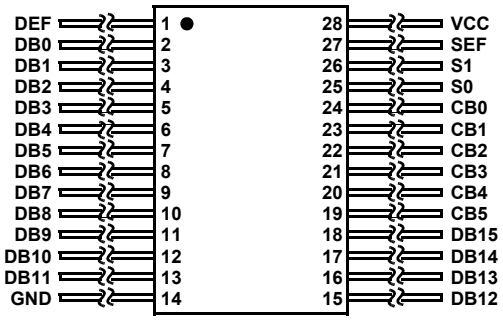
The ACTS630MS is supplied in a 28 lead Ceramic Flatpack (K suffix) or a 28 Lead Ceramic Dual-In-Line Package (D suffix).

Pinouts

28 PIN CERAMIC DUAL-IN-LINE, MIL-STD-1835 DESIGNATOR CDIP-T28, LEAD FINISH C
TOP VIEW



28 PIN CERAMIC FLATPACK, MIL-STD-1835 DESIGNATOR CDFP3-F28, LEAD FINISH C
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9672101VXC	-55°C to +125°C	MIL-PRF-38535 Class V	28 Lead SBDIP
5962F9672101VYC	-55°C to +125°C	MIL-PRF-38535 Class V	28 Lead Ceramic Flatpack
ACTS630D/Sample	25°C	Sample	28 Lead SBDIP
ACTS630K/Sample	25°C	Sample	28 Lead Ceramic Flatpack
ACTS630HMSR	25°C	Die	Die

Function Tables

Control Functions

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECKWORD	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data and Check-word	Input Data	Input Checkword	Low	Low
READ	High	High	Latch and Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word and Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

Check Word Generation

CHECKWORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

NOTE: The six check bits are parity bits derived from the matrix of data bits as indicated by “x” for each bit

Error Syndrome Codes

SYNDROME ERROR CODE	ERROR LOCATIONS																						
	DB																CB						NO ERROR
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Error Functions

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-BIT DATA	6-BIT CHECKWORD	SEF	DEF	
0	0	Low	Low	Not Applicable
1	0	High	Low	Correction
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

Die Characteristics

DIE DIMENSIONS:

171 mils x 159 mils
6.7μm x 6.3μm

METALLIZATION:

Type: Al/Si/
Metal 1 Thickness: 7.125kÅ ±1.125kÅ
Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:

110μm x 110μm
4.3 mils x 4.3 mils

Metallization Mask Layout