RGB to NTSC/PAL Encoder

AD722

FEATURES
Low Cost, Integrated Solution
+5 V Operation
Accepts FSC Clock or Crystal, or 4FSC Clock
Composite Video and Separate Y/C (S-Video) Outputs
Minimal External Components:
No External Filters or Delay Lines Required
Onboard DC Restoration
Accepts Either HSYNC & VSYNC or CSYNC
Phase Lock to External Subcarrier
Drives 75 Ω Reverse-Terminated Loads
Logic Selectable NTSC or PAL Encoding Modes
Compact 16-Pin SOIC

APPLICATIONS
RGB to NTSC or PAL Encoding

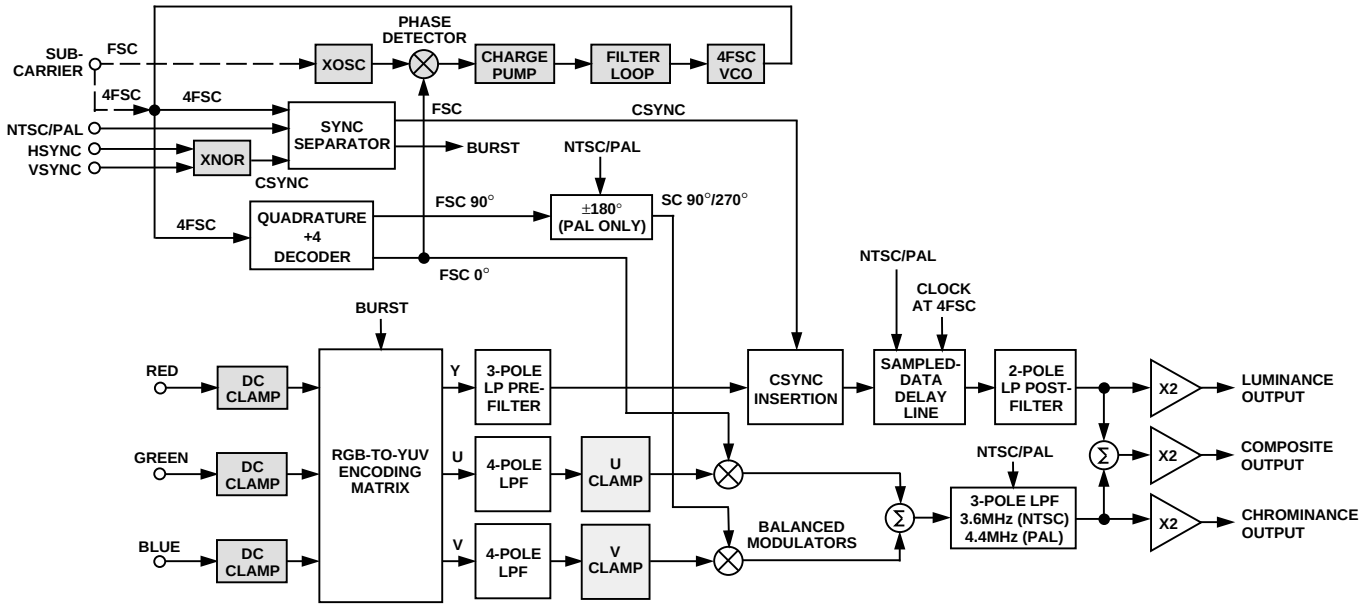
PRODUCT DESCRIPTION
The AD722 is a low cost RGB to NTSC/PAL Encoder that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide composite video output. All three outputs can simultaneously drive 75 Ω, reverse-terminated cables. All logical inputs are CMOS compatible. The chip operates from a single +5 V supply. No external delay lines or filters are required. The AD722 may be powered down when not in use.

The AD722 accepts either FSC or 4FSC clock. When a clock is not available, a low cost parallel-resonant crystal (3.58 MHz (NTSC) or 4.43 MHz (PAL)) and the AD722's on-chip oscillator generate the necessary subcarrier clock. The AD722 also accepts the subcarrier clock from an external video source.

The interface to VGA Controllers and MPEG Video Decoders is simple: an on-chip logic "XNOR" accepts the available vertical (VSYNC) and horizontal sync (HSYNC) signals and creates the composite sync (CSYNC) signal on-chip. If available, the AD722 will also accept a standard CSYNC signal by connecting VSYNC to +5 V and applying CSYNC to HSYNC pin. The AD722 contains decoding logic to identify valid HSYNC pulses for correct burst insertion.

Delays in the U and V chroma filters are matched by an on-chip sampled-data delay line in the Y signal path. To prevent aliasing, a prefilter at 5 MHz is included ahead of the delay line and a post-filter at 5 MHz is added after the delay line to suppress harmonics in the output. These low-pass filters are optimized for minimum pulse overshoot. The overall luma delay, relative to chroma, has been designed to be 170 ns, which precompensates for delays in the filters used in the IF section of a television receiver. This precompensation delay is already present in TV broadcasts. The AD722 comes in a space-saving SOIC and is specified for the 0°C to +70°C commercial temperature range.

FUNCTIONAL BLOCK DIAGRAM



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AD722–SPECIFICATIONS (Unless otherwise noted, V_S = +5, T_A = +25°C, using FSC synchronous clock. All loads are 150 Ω ± 5% at the IC pins. Outputs are measured at the 75 Ω reverse terminated load.)

Parameter	Conditions	Min	Typ	Max	Units
SIGNAL INPUTS (RDIN, GRIN, BLIN)					
Input Amplitude	NTSC			714	mV p-p
	PAL			700	mV p-p
Black Level		0		3	V
Input Resistance[1]	Red, Green, Blue	1			MΩ
Input Capacitance			5		pF
LOGIC INPUTS (SYNC, FSC, ENCD, NTSC)	CMOS Logic Levels				
Logic LO Input Voltage				1	V
Logic HI Input Voltage		4			V
Logic LO Input Current (DC)			<1		µA
Logic HI Input Current (DC)			<1		µA
VIDEO OUTPUTS[2]					
Luminance (LUMA)					
Roll-off @ 5 MHz	NTSC		–10		dB
	PAL		–7		dB
Gain Error		–15	–5	+15	%
Linearity			±0.6		%
Sync Level	NTSC	243	286	329	mV
	PAL		300		mV
DC Black Level			1.3		V
Chrominance (CRMA)					
Bandwidth	NTSC		3.6		MHz
	PAL		4.4		MHz
Color Burst Amplitude	NTSC	170	240	330	mV p-p
	PAL		252		mV
Color Signal to Burst Ratio Error		–15	±3	15	%
Color Burst Width	NTSC		2.51		µs
	PAL		2.28		µs
Phase Error[3]			±3		Degrees
DC Black Level			2.1		V
Chroma Feedthrough	R, G, B = 0		10	40	mV p-p
Chroma/Luma Time Alignment			–140		ns
Composite (COMP)					
Absolute Gain Error		–5	±1	5	%
Differential Gain	With Respect to Chroma		0.5		%
Differential Phase	With Respect to Chroma		2.0		%
DC Black Level			1.6		V
POWER SUPPLIES					
Recommended Supply Range	Single Supply	+4.75		+5.25	V
Quiescent Current—Encode Mode			30	40	mA
Quiescent Current—Power Down			1		mA

NOTES
[1]R, G, and B signals are inputted to an on-chip AC coupling capacitor.
[2]All outputs measured at a 75 Ω reverse-terminated load; voltages at the IC output pins are twice those specified here.
[3]Difference between ideal color-bar phases and the actual values.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_S . . . . . +6 V
Internal Power Dissipation . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTE

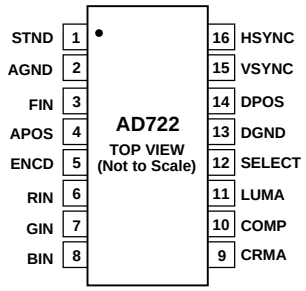
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics: 16-Pin SOIC Package: θ_{JA} = 100°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD722JR-16	0°C to +70°C	16-Pin SOIC	R-16
AD722JR-16-Reel	0°C to +70°C	16-Pin SOIC	R-16
AD722JR-16-Reel7	0°C to +70°C	16-Pin SOIC	R-16

PIN CONFIGURATION
16-Pin Small Outline Package (Wide Body)
(R-16)



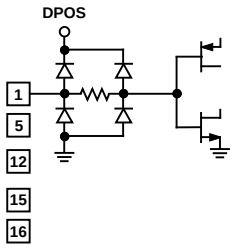
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD722 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

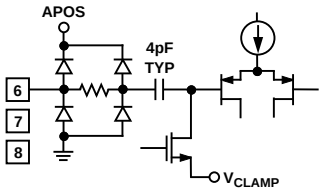
PIN DESCRIPTIONS

Pin	Mnemonic	Description	Equivalent Circuit
1	STND	A Logical HIGH input selects NTSC encoding. A Logical LOW input selects PAL encoding. CMOS Logic Levels.	Circuit A
2	AGND	Analog Ground Connection.	
3	FIN	FSC clock or parallel-resonant crystal, or 4FSC clock input. For NTSC: 3.579 545 MHz or 14.318 180 MHz. For PAL: 4.433 619 MHz or 17.734 480 MHz. CMOS Logic Levels for subcarrier clocks.	Circuit B
4	APOS	Analog Positive Supply (+5 V ± 5%).	
5	ENCD	A Logical HIGH input enables the encode function. A Logical LOW input powers down chip when not in use. CMOS Logic Levels.	Circuit A
6	RIN	Red Component Video Input. 0 to 714 mV for NTSC; 0 to 700 mV for PAL.	Circuit C
7	GIN	Green Component Video Input. 0 to 714 mV for NTSC. 0 to 700 mV for PAL.	Circuit C
8	BIN	Blue Component Video Input. 0 to 714 mV for NTSC. 0 to 700 mV for PAL.	Circuit C
9	CRMA	Chrominance Output (Subcarrier Only).* Approximately 1.8 V peak-to-peak for both NTSC and PAL.	Circuit D
10	COMP	Composite Video Output.* Approximately 2.5 V peak-to-peak for both NTSC and PAL.	Circuit D
11	LUMA	Luminance plus SYNC Output.* Approximately 2 V peak-to-peak for both NTSC and PAL.	Circuit D
12	SELECT	A Logical LOW input selects the FSC operating mode. A Logical HIGH input selects the 4FSC operating mode. CMOS Logic Levels.	Circuit A
13	DGND	Digital Ground Connections.	
14	DPOS	Digital Positive Supply (+5 V ± 5%) .	
15	VSYNC	Vertical Sync Signal (if using external CSYNC set at +5 V).	Circuit A
16	HSYNC	Horizontal Sync Signal (or CSYNC signal).	Circuit A

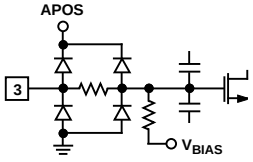
*The Luminance, Chrominance, and Composite Outputs are at twice normal levels for driving 75 Ω reverse-terminated lines.



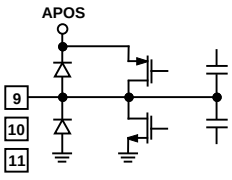
Circuit A



Circuit C



Circuit B



Circuit D

Equivalent Circuits

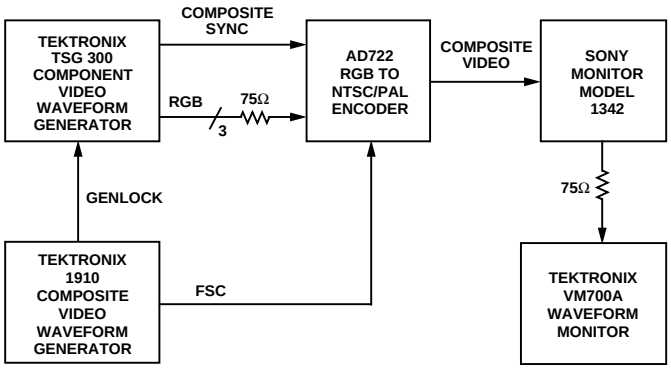


Figure 1. Evaluation Setup

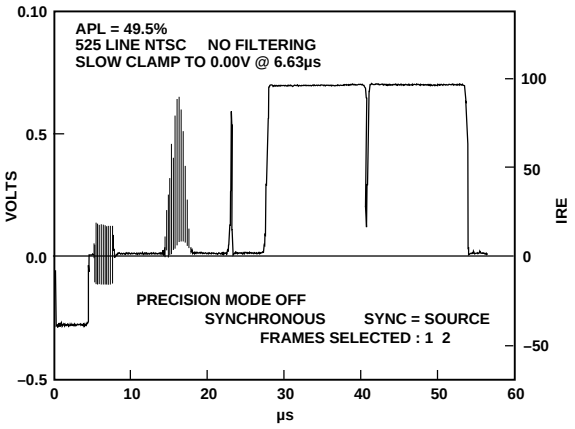


Figure 2. Modulated Pulse and Bar, NTSC

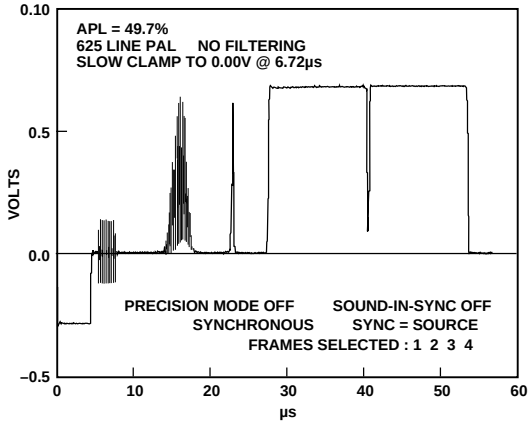


Figure 3. Modulated Pulse and Bar, PAL

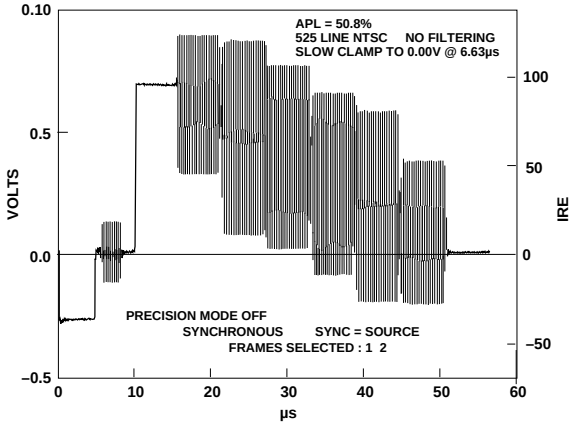


Figure 4. 100% Color Bars, NTSC

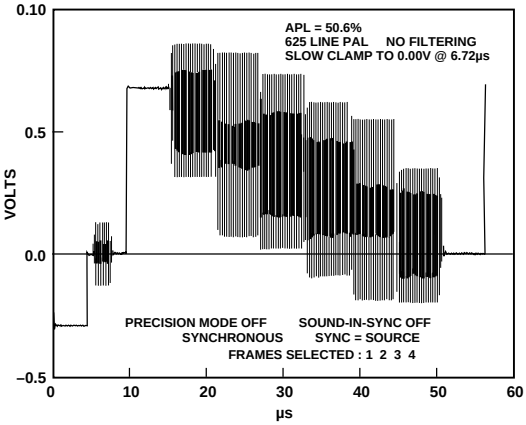


Figure 5. 100% Color Bars, PAL

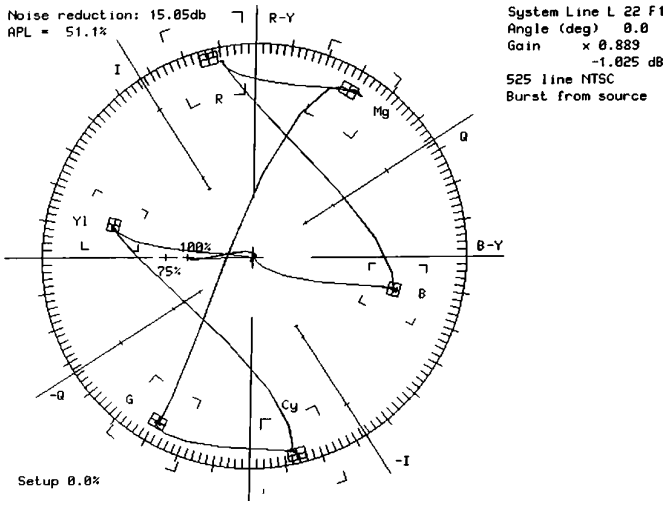


Figure 6. 100% Color Bars on Vector Scope, NTSC

AD722–Typical Characteristics

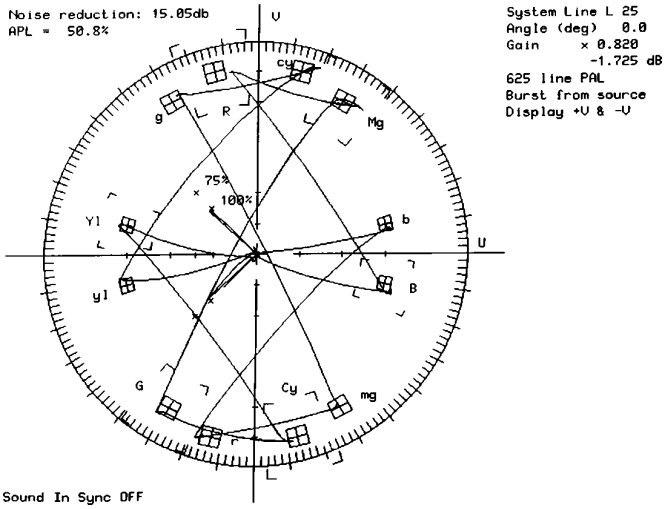


Figure 7. 100% Color Bars on Vector Scope, PAL

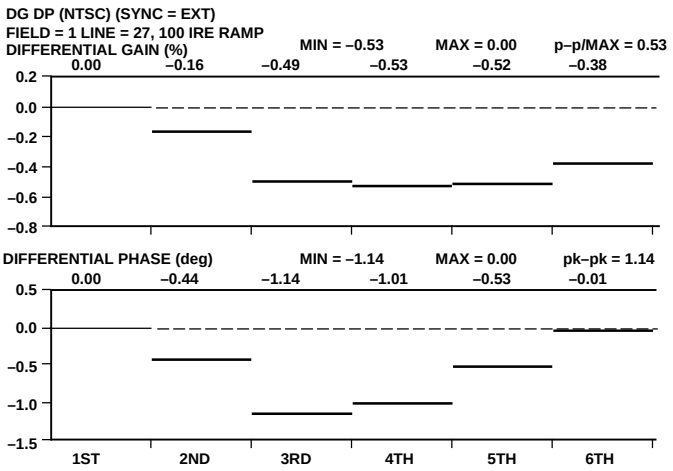


Figure 10. Composite Output Differential Phase and Gain, NTSC

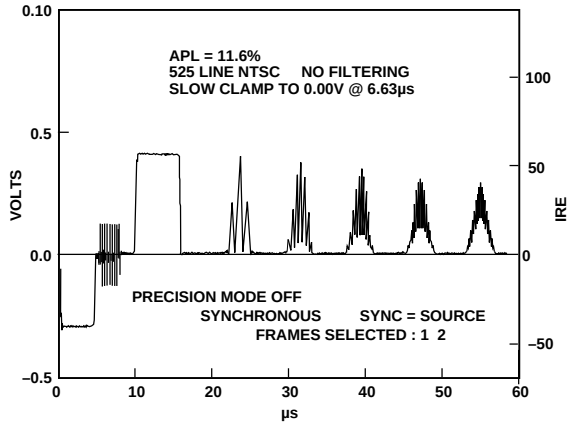


Figure 8. Multipulse, NTSC

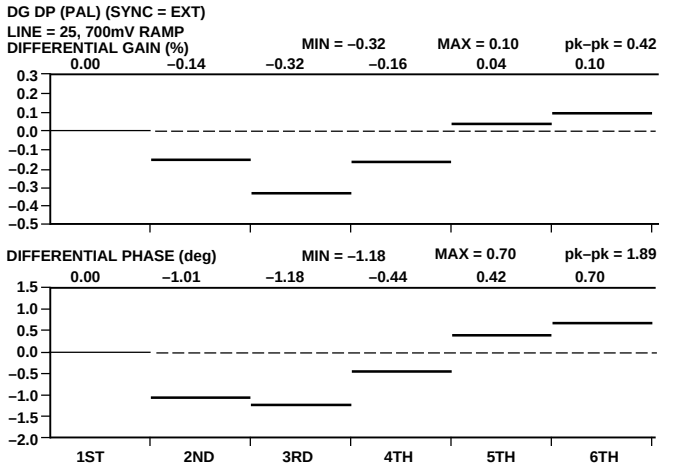


Figure 11. Composite Output Differential Phase and Gain, PAL

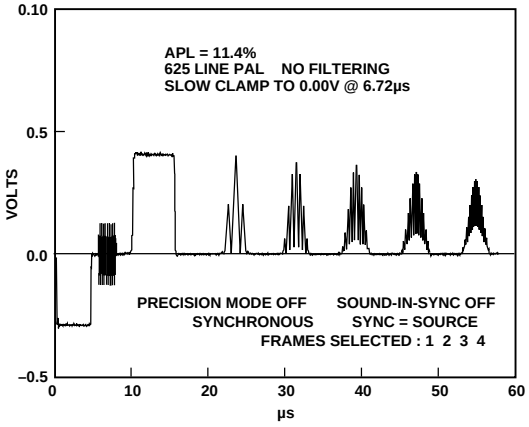


Figure 9. Multipulse, PAL

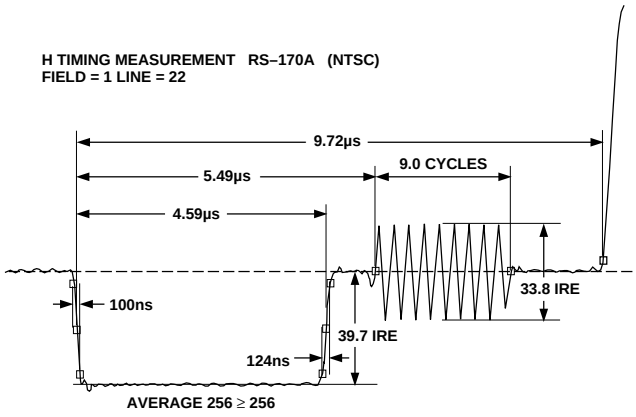


Figure 12. Horizontal Timing, NTSC

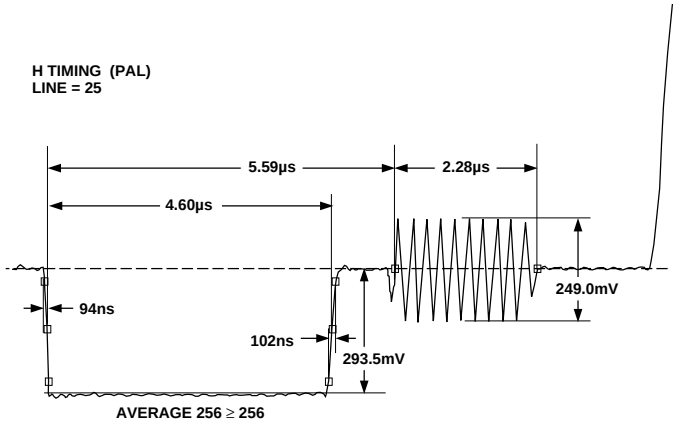


Figure 13. Horizontal Timing, PAL

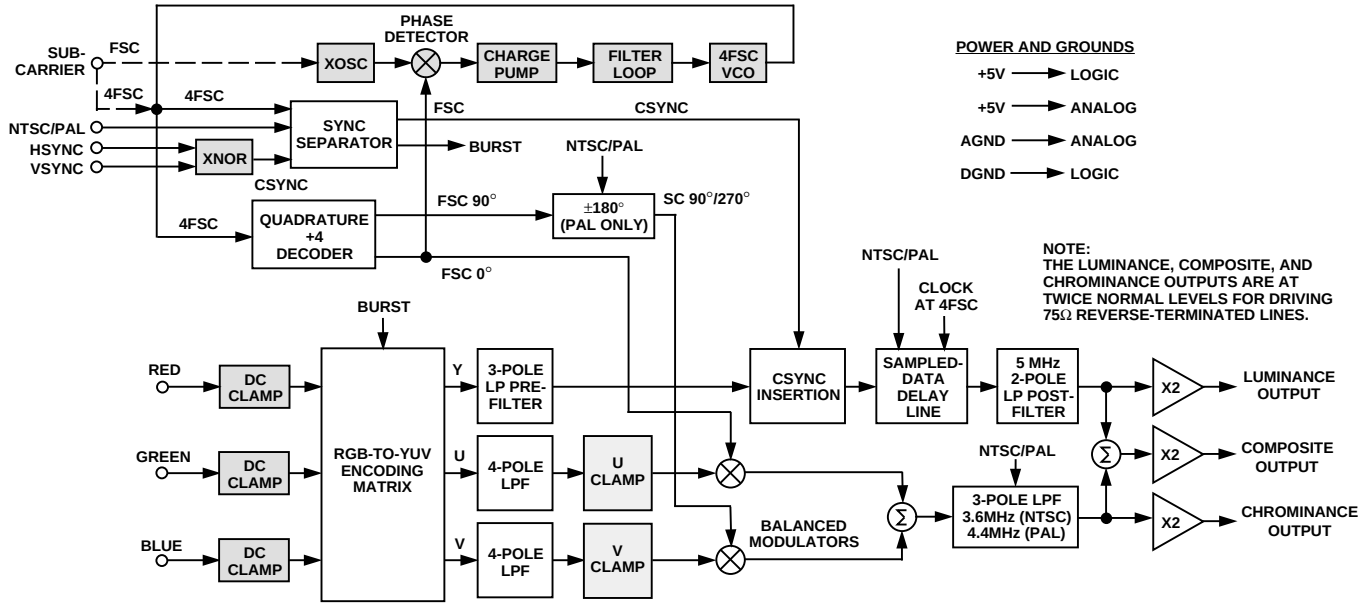


Figure 14. Functional Block Diagram

THEORY OF OPERATION

The AD722 was designed to have three allowable modes of applying a clock via the FIN pin. These are FSC (frequency of subcarrier, 3.579545 MHz for NTSC or 4.433618 MHz for PAL) mode with CMOS clock applied, FSC mode using on-chip crystal oscillator, and 4FSC mode with CMOS clock applied. To use FSC mode SELECT is pulled low and then either a CMOS FSC clock is applied to FIN, or a parallel-resonant crystal and appropriate tuning capacitor is placed between FIN pin and GND to utilize the on-chip oscillator. The on-chip Phase Locked Loop (PLL) is used in these modes to generate an internal 4FSC which is divided to perform the digital clocking as well as to create the quadrature subcarrier signals for the chrominance modulation. In 4FSC mode the PLL is bypassed.

Referring to the AD722 block diagram (Figure 14), the RGB inputs (each 714 mV p-p max for NTSC or 700 mV p-p max for PAL) are ac-coupled and then pass through dc clamps. These clamps allow the user to have a black level which is not at 0 V. The clamps will clamp to a black input signal level between 0 V and 3 V. The clamping occurs just after the falling edge of HSYNC.

The RGB inputs then pass into an analog encoding matrix which creates the luminance ("Y") signal and the chrominance color difference ("U" and "V") signals. The RGB to YUV encoding is performed using the following standard transformation:

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B$$

$$U = 0.493 \times (B–Y)$$

$$V = 0.877 \times (R–Y)$$

After the encoding matrix, the AD722 has two parallel analog paths. The Y (luminance) signal is first passed through a 3-pole 4.85 MHz/6 MHz (NTSC/PAL) Bessel low-pass filter to prevent aliasing in the sampled-data delay line. This first low-pass filter is also where the unclocked analog sync signal is injected into the Y signal (more on the creation of this sync signal to follow). The Y signal then passes through the sampled-data delay line, which is clocked at 4FSC. The delay line was designed to give an overall chrominance to luminance delay of –170 ns. Following the sampled-data delay line is a 5.25 MHz/6.5 MHz (NTSC/PAL) 2-pole low-pass Bessel filter to smooth the reconstructed luminance signal.

The other analog path is the chrominance path which is where the U and V color difference signals are processed. The U and V signals first pass through 4-pole modified Bessel low-pass filters with –3 dB frequencies of 1.2 MHz/1.5 MHz (NTSC/PAL) to prevent aliasing in the modulators. The color burst signal is injected into the U and V channels in these premodulation filters. The U and V signals are then modulated independently by a pair of balanced switching modulators driven in quadrature by the color subcarrier.

The bandwidths of all the on-chip filters are tuned using proprietary auto-tuning circuitry. The basic principle is to match an RC time constant to a reference time period, that time being one cycle of a subcarrier clock. The auto-tuning is done during the vertical blanking interval and has some added hysteresis so that once an acceptable tuning value is reached the part won't toggle between tuning values from field to field. The bandwidths stated in the above discussion are the design target bandwidths for NTSC and PAL.

The AD722's 4FSC clock (either produced by the on-chip PLL or user supplied) drives a digital divide-by-4 circuit to create the quadrature signals for modulation. The reference phase 0° is used for the U signal. In the NTSC mode, the V signal is modulated at 90°, but in PAL mode, the V modulation alternates between 90° and 270° at half the line rate as required by the PAL standard. The outputs of the U and V balanced modulators are summed and passed through a 3-pole low-pass filter with 3.6 MHz/4.4 MHz bandwidths (NTSC/PAL) in order to remove the harmonics generated during the switching modulation.

The filtered chrominance signal is then summed with the filtered luminance signal to create the composite video signal. The separate luminance, chrominance, and composite video signals are amplified by a factor of two in order to drive 75 Ω reverse-terminated lines. The separate luminance and chrominance outputs together are known as S-video. The composite and S-video outputs are simultaneously available.

The two sync inputs HSYNC and VSYNC are fed into an XNOR gate to create a CSYNC signal for the AD722. If the user produces, or has access to, a true composite sync signal, it can be input to the HSYNC pin while the VSYNC pin is held high. In either case the CSYNC signal which is present after the XNOR gate, is used to generate the sync and burst signals which ultimately get injected into the analog signal chain. The unclocked CSYNC signal is sent to a reference cell on the chip which, when CSYNC is low, allows a reference voltage (based on a power supply division) to be injected into the luminance chain. The width of the injected sync is the same as the width of the supplied sync signal.

The CSYNC signal (after the XNOR gate) also goes to the digital section of the AD722 where it is clocked in by a 2FSC clock. The digital section then measures the width of the CSYNC pulses to separate horizontal pulses from vertical equalizing and serration pulses. A burst flag is generated only after valid horizontal sync pulses and is timed from the falling edge of the clocked-in CSYNC signal. In synchronous systems (those in which the subcarrier clock, sync signals, and RGB signals are all synchronous) this will give a fixed burst position relative to the falling edge of the output sync. However, in asynchronous systems the sync to burst position can change line to line by as much as 140 ns (the period of a 2FSC clock cycle) due to the fact that the burst flag is generated from a clocked CSYNC while the sync is injected unclocked. This phenomenon may or may not create visual artifacts in some high-end video systems. The burst flag which is generated goes to the reference cell and allows a reference voltage to be inserted to the U and V low-pass filters.

APPLYING THE AD722

Inputs

RIN, BIN, GIN are analog inputs that should be terminated to ground with 75 Ω in close proximity to the IC. When properly terminated the peak-to-peak voltage for a maximum input level should be 714 mV p-p for NTSC or 700 mV p-p for PAL. The horizontal blanking interval should be the most negative part of each signal.

The signal should be flat during the horizontal blanking interval. Internal circuitry will clamp this level during HSYNC to a reference that is used internally as the black level. The horizontal blanking level at the input pins can range between 0 V and 3 V with respect to the ground level of the AD722.

HSYNC and VSYNC are two logic level inputs that are combined internally to produce a composite sync signal. If a composite sync signal is to be used, it can be input to HSYNC while VSYNC is pulled to logic HI (+5 V).

The form of the input sync signal(s) will determine the form of the composite sync on the composite video (COMP) and luminance (LUMA) outputs. If no equalization or serration pulses are included in the HSYNC input there won't be any in the outputs. Although sync signals without equalization and serration pulses do not technically meet the video standards' specifications, many monitors do not require these pulses in order to display good pictures. The decision whether to include these signals is a system tradeoff between cost and complexity and adhering strictly to the video standards.

The SELECT input is a CMOS logic level that programs the AD722 to use a subcarrier at a 1FSC (LO) frequency or a 4FSC (HI) frequency for the appropriate standard being used. A 4FSC clock is used directly, while a 1FSC input is multiplied up to 4FSC by an internal phase locked loop.

The FIN input can be a logic level clock at either FSC or 4FSC frequency or can be a parallel resonant crystal at 1FSC frequency. An on-chip oscillator will drive the crystal. Most crystals will require a shunt capacitance of between 10 pF and 30 pF for reliable start up and proper frequency of operation.

The NTSC specification calls for a frequency accuracy of ±10 Hz from the nominal subcarrier frequency of 3.579545 MHz. While maintaining this accuracy in a broadcast studio might not be a severe hardship, it can be quite expensive in a low cost consumer application.

The AD722 will operate with subcarrier frequencies that deviate quite far from those specified by the TV standards. However, the monitor will in general not be quite so forgiving. Most monitors can tolerate a subcarrier frequency that deviates several hundred Hz from the nominal standard without any degradation in picture quality. These conditions imply that the subcarrier frequency accuracy is a system specification and not a specification of the AD722 itself.

The STND pin is used to select between NTSC and PAL operation. Various blocks inside the AD722 use this input to program their operation. Most of the more common variants of NTSC and PAL are supported. There are, however, two known specific standards which are not supported. These are NTSC 4.43 and M-PAL.

Basically these two standards use most of the features of the standard that their names imply, but use the subcarrier that is equal to or approximately equal to the frequency of the other standard. Because of the automatic programming of the filters in the chrominance path and other timing considerations, it is not possible to support these standards.

Layout Considerations

The AD722 is an all CMOS mixed signal part. It has separate pins for the analog and digital +5 V and ground power supplies. Both the analog and digital ground pins should be tied to the ground plane by a short, low inductance path. Each power supply pin should be bypassed to ground by a low inductance 0.1 μF capacitor and a larger tantalum capacitor of about 10 μF.

The three analog inputs (RIN, GIN, BIN) should be terminated with 75 Ω to ground close to the respective pins. However, as these are high impedance inputs, they can be in a loop-thru configuration. This technique is used to drive two or more devices with high frequency signals that are separated by some distance. A connection is made to the AD722 with no local termination, and the signals are run to another distant device where the termination for these signals is provided.

The output amplitudes of the AD722 are double that required by the devices that it drives. This compensates for the halving of the signal levels by the required terminations. A 75 Ω series resistor is required close to each AD722 output, while 75 Ω to ground should terminate the far end of each line.

The outputs have a dc bias and must be ac coupled for proper operation. The COMP and LUMA outputs have information down to 30 Hz that must be transmitted. Each output requires a 220 μF series capacitor to work with the 75 Ω resistance to pass these low frequencies. The CRMA signal has information mostly up at the chroma frequency and can use a smaller capacitor if desired, but 220 μF can be used to minimize the number of different components used in the design.

Displaying VGA Output on a TV

The AD722 can be used to convert the analog RGB output from a personal computer's VGA card to the NTSC or PAL television standards. To accomplish this it is important to understand that the AD722 requires interlaced RGB video and clock rates that are consistent with those required by the television standards. In most computers the default output is a noninterlaced RGB signal at a frame rate higher than used by either NTSC or PAL.

Most VGA controllers support a wide variety of output modes that are controlled by altering the contents of internal registers. It is best to consult with the VGA controller manufacturer to determine the exact configuration required to provide an interlaced output at 60 Hz (50 Hz for PAL).

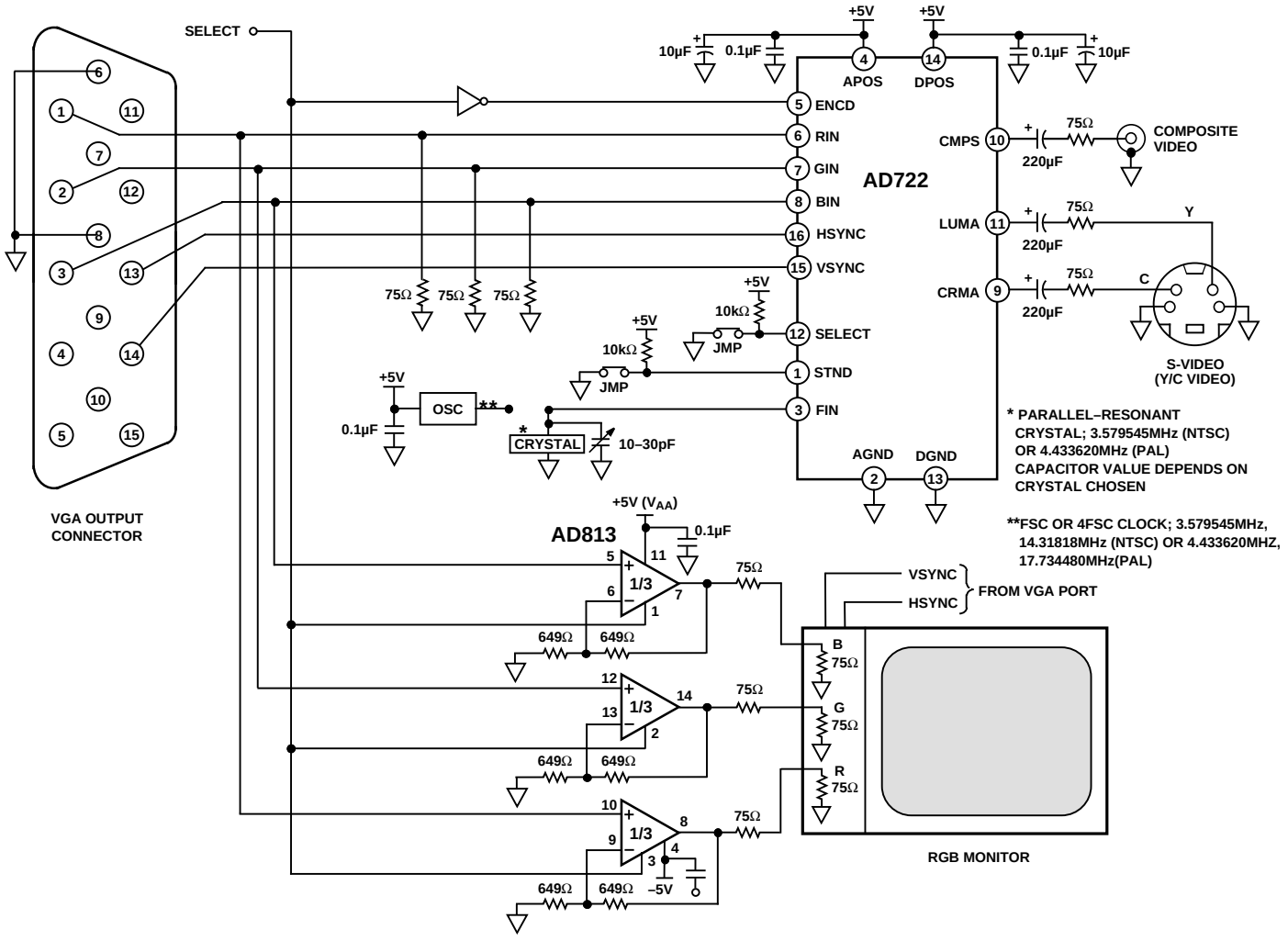


Figure 15. Interfacing the AD722 to the (Interlaced) VGA Port of a PC

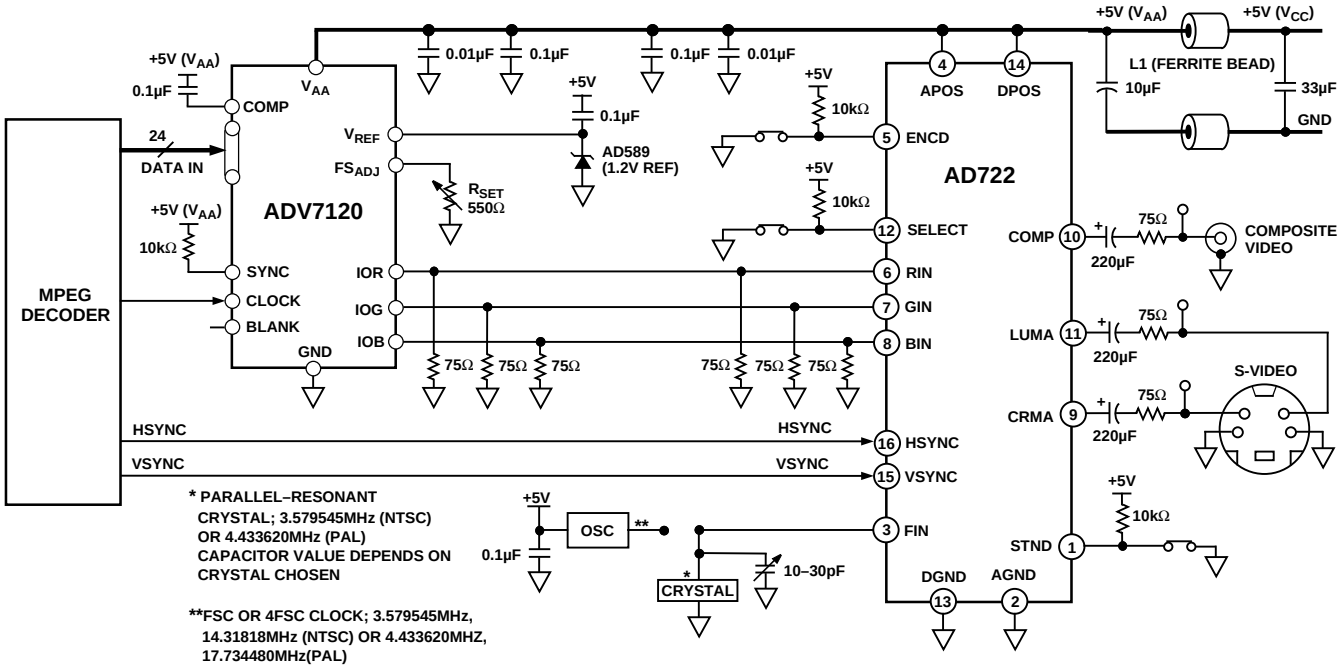


Figure 16. AD722 and ADV7120/ADV7122 Providing MPEG Video Solution

Figure 15 shows a circuit for connection to the VGA port of a PC. The RGB outputs connect directly to the respective inputs of the AD722. These signals should each be terminated to ground with 75 Ω.

The standard 15-pin VGA connector has HSYNC on Pin 13 and VSYNC on Pin 14. These signals also connect directly to the same name signals on the AD722. The FIN signal can be provided by any of the means described elsewhere in the data sheet. For a synchronous NTSC system, the internal 4FSC (14.31818 MHz) clock that drives the VGA controller can be used for FIN on the AD722. This signal is not directly accessible from outside the computer, but it does appear on the VGA card.

If a separate RGB monitor is also to be used, it is not possible to simply connect it to the R, G, and B signals. The monitor provides a termination that would double terminate these signals. The R, G, and B signals should be buffered by three amplifiers with high input impedances. These should be configured for a gain of two, which is normalized by the divide by two termination scheme used for the RGB monitor.

The AD813 is a triple video amplifier that can provide the necessary buffering in a single package. It also provides a disable pin for each amplifier which can be used to disable the drive to the RGB monitor when interlaced video is used (SELECT = LO). When the RGB signals are noninterlaced, setting SELECT HI will enable the AD813 to drive the RGB monitor and disable the encoding function of the AD722 via Pin 5. HSYNC and VSYNC are logic level signals that can drive both the AD722 and RGB monitor in parallel.

AD722 Used with an MPEG Decoder

MPEG decoding of compressed video signals is becoming a more prevalent feature in many PC systems. To display images on the computer monitor, video in RGB format is required. However, to display the images on a TV monitor or to record the images on a VCR, video in composite format is required. Figure 16 shows a schematic for taking the 24-bit wide RGB video from an MPEG decoder and creating both analog RGB video and composite video.

The 24-bit wide RGB video is converted to analog RGB by the ADV7120 (Triple 8-bit video DAC–available in 48-pin TQFP). The analog current outputs from the DAC are terminated to ground at both ends with 75 Ω as called for in the data sheet. These signals directly feed the analog inputs of the AD722. The HSYNC and VSYNC signals from the MPEG Controller are directly applied to the AD722.

If the set of termination resistors closest to the AD722 are removed, an RGB monitor can be connected to these signals and it will provide the required second termination. This scenario is acceptable as long as the RGB monitor is always present and connected. If it is to be removed on occasion, another termination scheme is required.

The AD813 triple video op amp can provide buffering for such applications. Each channel is set for a gain of two while the outputs are back terminated with a series 75 Ω resistor. This provides the proper signal levels at the monitor which terminates the lines with 75 Ω.

AD722 APPLICATION DISCUSSION

Chrominance and Luminance Alignment

Inside the AD722 the chrominance and luminance signals are processed by separate paths. They both are either output separately (Y/C), or they are added together by the composite video amplifier. Although both channels are filtered, the chrominance signal experiences a greater filtering delay due to the higher order of the chrominance path filters. To compensate, a sampled delay line is used in the luminance path.

For baseband video it is desirable for the chrominance and luminance to be accurately aligned with zero offset. However, the situation for modulated RF video is a bit more complicated due to the effects of the IF circuitry used in TV sets.

The IF strips used in TVs delay the chrominance by 170 ns more than the luminance. To compensate for this, transmitted video has the chrominance lead the luminance by 170 ns. The term used for this is chrominance delay, and it is specified as –170 ns, the negative (–) indicating that chrominance leads the luminance. This correction to TV broadcasts was made in the early days of TV and is the standard to this day.

The delay line used in the luminance path of the AD722 creates a –170 ns chrominance delay. This will be realigned by the RF section of a TV when it is used for receiving the signal.

However, for baseband inputs, the chrominance will lead the luminance by a small amount. This will show up as a slight color shadow to the left of objects. The physical offset can be calculated by approximating the active horizontal line time of a TV as 50 µs. Thus, the chrominance offset distance will be the width of the screen times (50 µs/170 ns) or 0.0034. For a 13 inch monitor the screen width is about 10 in. (25 cm), so the offset distance will be 0.034 in. (0.85 mm).

Dot Crawl

There are numerous distortions that are apparent in the presentation of composite NTSC signals on TV monitors. These effects will vary in degree depending on the circuitry used by the monitor to process the signal and on the nature of the image being displayed. It is generally not possible to produce pictures on a composite monitor that are as high quality as those produced by standard quality RGB, VGA monitors.

One well known distortion of composite video images is called dot crawl. It shows up as a moving dot pattern at the interface between two areas of different color. It is caused by the inability of the monitor circuitry to adequately separate the luminance and chrominance signals.

One way to prevent dot crawl is to use a video signal that has separate luminance and chrominance. Such a signal is referred to as S-video or Y/C video. Since the luminance and chrominance are already separated, the monitor does not have to perform this function. The S-Video outputs of the AD722 can be used to create higher quality pictures when there is an S-Video input available on the monitor.

Flicker

In a VGA conversion application, where the software controlled registers are correctly set, there are two techniques that are commonly used by VGA controller manufacturers to generate the interlaced signal. Each of these techniques introduces a unique characteristic into the display created by the AD722. The artifacts described below are not due to the encoder or its encoding algorithm as all encoders will generate the same display when presented with these inputs. They are due to the method used by the controller display chip to convert a noninterlaced output to an interlaced signal. The method used is a feature of the design of the VGA chip and is not programmable.

The first interlacing technique outputs a true interlaced signal with odd and even fields (one each to a frame Figure 17a). This provides the best picture quality when displaying photography, CD video and animation (games, etc.). However, it will introduce a defect commonly referred to as flicker into the display. Flicker is a fundamental defect of all interlaced displays and is caused by the alternating field characteristic of the interlace technique. Consider a one pixel high black line which extends horizontally across a white screen. This line will exist in only one field and will be refreshed at a rate of 30 Hz (25 Hz for PAL). During the time that the other field is being displayed the line will not be displayed. The human eye is capable of detecting this, and the display will be perceived to have a pulsating or flickering black line. This effect is highly content sensitive and is most pronounced in applications in which text and thin horizontal lines are present. In applications such as CD video, photography and animation, portions of objects naturally occur in both odd and even fields and the effect of flicker is imperceptible.

The second technique which is commonly used is to output an odd and even field which are identical (Figure 17b). This ignores the data which naturally occurs in one of the fields. In this case the same one pixel high line mentioned above would either appear as a two pixel high line, (one pixel high in both the odd and even field) or will not appear at all if it is in the data which is ignored by the controller. Which of these cases occurs is dependent on the placement of the line on the screen. This technique provides a stable (i.e., nonflickering) display for all applications, but small text can be difficult to read and lines in drawings (or spreadsheets) can disappear. As above, graphics and animation are not particularly affected although some resolution is lost.

There are methods to dramatically reduce the effect of flicker and maintain high resolution. The most common is to ensure that display data never exists solely in a single line. This can be accomplished by averaging/weighting the contents of successive/multiple noninterlaced lines prior to creating a true interlaced output (Figure 17c). In a sense this provides an output which will lie between the two extremes described above. The weight or percentage of one line that appears in another and the number of lines used are variables that must be considered in developing a system of this type. If this type of signal processing is performed, it must be completed prior to the data being presented to the AD722 for encoding.

Vertical Scaling

In addition to converting the computer generated image from noninterlaced to interlaced format, it is also necessary to scale the image down to fit into NTSC or PAL format. The most common vertical lines/screen for VGA display are 480 and 600 lines. NTSC can only accommodate approximately 400 visible lines/frame (200 per field), PAL can accommodate 576 lines/frame (288 per field). If scaling is not performed, portions of the original image will not appear in the television display.

This line reduction can be performed by merely eliminating every Nth (6th line in converting 480 lines to NSTC or every 25th line in converting 600 lines to PAL). This risks generation of jagged edges and jerky movement. It is best to combine the scaling with the interpolation/averaging technique discussed above to ensure that valuable data is not arbitrarily discarded in the scaling process. Like the flicker reduction technique mentioned above, the line reduction must be accomplished prior to the AD722 encoding operation.

There is a new generation of VGA controllers on the market specifically designed to utilize these techniques to provide a crisp and stable display for both text and graphics oriented applications. In addition these chips rescale the output from the computer to fit correctly on the screen of a television. A list of known devices is available through Analog Devices' Applications group, but the most complete and current information will be available from the manufacturers of graphics controller ICs.

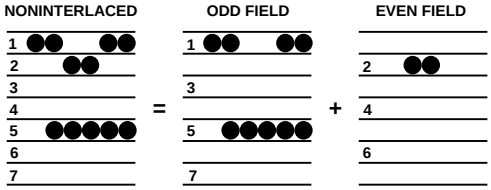
Synchronous vs. Asynchronous Operation

The source of RGB video and synchronization used as an input to the AD722 in some systems is derived from the same clock signal as used for the AD722 subcarrier input (FIN). These systems are said to be operating synchronously. In systems where two different clock sources are used for these signals, the operation is called asynchronous.

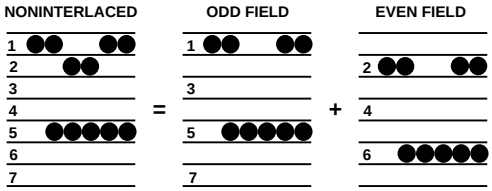
The AD722 supports both synchronous and asynchronous operation, but some minor differences might be noticed between them. These can be caused by some details of the internal circuitry of the AD722.

There is an attempt to process all of the video and synchronization signals totally asynchronous with respect to the subcarrier signal. This was achieved everywhere except for the sampled delay line used in the luminance channel to time align the luminance and chrominance. This delay line uses a signal at twice the subcarrier frequency as its clock.

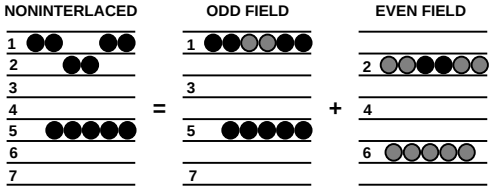
The phasing between the delay line clock and the luminance signal (with inserted composite sync) will be constant during synchronous operation, while the phasing will demonstrate a periodic variation during asynchronous operation. The jitter of the asynchronous video output will be slightly greater due to these periodic phase variations.



a. Conversion of Noninterlace to Interlace



b. Line Doubled Conversion Technique



c. Line Averaging Technique

Figure 17.

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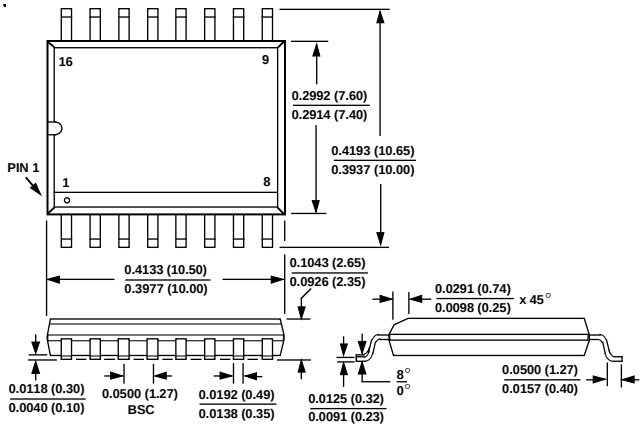
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead SOIC (R-16) (Wide Body)



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