# 3 MSPS, 14-Bit SAR ADC

# AD7484

## FEATURES

**Fast throughput rate: 3 MSPS**
**Wide input bandwidth: 40 MHz**
**No pipeline delays with SAR ADC**
**Excellent dc accuracy performance**
**2 parallel interface modes**
**Low power: 90 mW (full power) and 2.5 mW (nap mode)**
**Standby mode: 2 µA maximum**
**Single 5 V supply operation**
**Internal 2.5 V reference**
**Full-scale overrange mode (using 15th bit)**
**System offset removal via user access offset register**
**Nominal 0 V to 2.5 V input with shifted range capability**
**Pin compatible upgrade of 12-bit AD7482**

## FUNCTIONAL BLOCK DIAGRAM

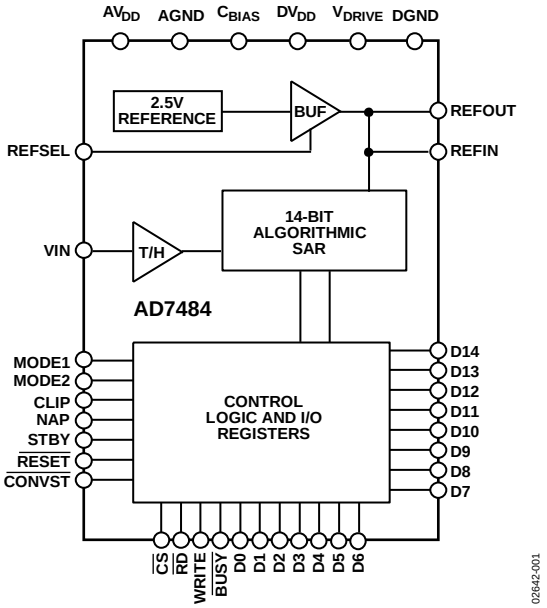


*Figure 1.*

## GENERAL DESCRIPTION

The AD7484 is a 14-bit, high speed, low power, successive approximation ADC. The part features a parallel interface with throughput rates up to 3 MSPS. The part contains a low noise, wide bandwidth track-and-hold that can handle input frequencies in excess of 40 MHz.

The conversion process is a proprietary algorithmic successive approximation technique that results in no pipeline delays. The input signal is sampled, and a conversion is initiated on the falling edge of the $\overline{\text{CONVST}}$ signal. The conversion process is controlled by an internally trimmed oscillator. Interfacing is via standard parallel signal lines, making the part directly compatible with microcontrollers and DSPs.

The AD7484 provides excellent ac and dc performance specifications. Factory trimming ensures high dc accuracy, resulting in very low INL, offset, and gain errors.

The part uses advanced design techniques to achieve very low power dissipation at high throughput rates. Power consumption in the normal mode of operation is 90 mW. There are two power saving modes: a nap mode, which keeps the reference circuitry alive for a quick power-up while consuming 2.5 mW, and a standby mode that reduces power consumption to a mere 10 µW.

The AD7484 features an on-board 2.5 V reference but can also accommodate an externally provided 2.5 V reference source. The nominal analog input range is 0 V to 2.5 V, but an offset shift capability allows this nominal range to be offset by ±200 mV. This allows the user considerable flexibility in setting the bottom end reference point of the signal range, a useful feature when using single-supply op amps.

The AD7484 also provides an 8% overrange capability via a 15th bit. Therefore, if the analog input range strays outside the nominal range by up to 8%, the user can still accurately resolve the signal by using the 15th bit.

The AD7484 is powered by a 4.75 V to 5.25 V supply. The part also provides a $V_{DRIVE}$ pin that allows the user to set the voltage levels for the digital interface lines. The range for this $V_{DRIVE}$ pin is 2.7 V to 5.25 V. The part is housed in a 48-lead LQFP package and is specified over a −40°C to +85°C temperature range.

**Rev. C**


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# SPECIFICATIONS

$AV_{DD}/DV_{DD}$ = 5 V ± 5%, AGND = DGND = 0 V, $V_{REF}$ = external, $f_{SAMPLE}$ = 3 MSPS; all specifications $T_{MIN}$ to $T_{MAX}$ and valid for $V_{DRIVE}$ = 2.7 V to 5.25 V, unless otherwise noted. Operating temperature range is −40°C to +85°C.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE[1, 2] | | | | | |
| Signal-to-Noise + Distortion (SINAD)[3] | 76.5 | | | dB | $f_{IN}$ = 1 MHz |
| | | 78 | | dB | $f_{IN}$ = 1 MHz |
| | | 79 | | dB | $f_{IN}$ = 1 MHz, extended input |
| | | 77 | | dB | $f_{IN}$ = 1 MHz, internal reference |
| Total Harmonic Distortion (THD)[3] | | | −90 | dB | |
| | | −95 | | dB | |
| | | −92 | | dB | Internal reference |
| Peak Harmonic or Spurious Noise (SFDR)[3] | | | −90 | dB | |
| Intermodulation Distortion (IMD)[3] | | | | | |
| Second Order Terms | | −96 | | dB | $f_{IN1}$ = 95.053 kHz, $f_{IN2}$ = 105.329 kHz |
| Third Order Terms | | −94 | | dB | |
| Aperture Delay | | 10 | | ns | |
| Full Power Bandwidth | | 40 | | MHz | @ 3 dB |
| | | 3.5 | | MHz | @ 0.1 dB |
| DC ACCURACY | | | | | |
| Resolution | 14 | | | Bits | |
| Integral Nonlinearity[3] | | ±0.5 | ±1 | LSB | |
| Differential Nonlinearity[3] | | ±0.3 | ±0.75 | LSB | Guaranteed no missed codes to 14 bits |
| Offset Error[3] | | | ±6 | LSB | |
| | | | 0.036 | %FSR | |
| Gain Error[3] | | | ±6 | LSB | |
| | | | 0.036 | %FSR | |
| ANALOG INPUT | | | | | |
| Input Voltage | −200 | | | mV | |
| | | | +2.7 | V | |
| DC Leakage Current | | | ±1 | µA | $V_{IN}$ from 0 V to 2.7 V |
| | | ±2 | | µA | $V_{IN}$ = −200 mV |
| Input Capacitance[4] | | 35 | | pF | |
| REFERENCE INPUT/OUTPUT | | | | | |
| Input Voltage, $V_{REFIN}$ | | +2.5 | | V | ± 1% for specified performance |
| Input DC Leakage Current, $V_{REFIN}$ | | | ±1 | µA | |
| Input Capacitance, $V_{REFIN}$[4] | | 25 | | pF | |
| Input Current, $V_{REFIN}$ | | 220 | | µA | External reference |
| Output Voltage, $V_{REFOUT}$ | | +2.5 | | V | |
| Error @ 25°C, $V_{REFOUT}$ | | ±50 | | mV | |
| Error $T_{MIN}$ to $T_{MAX}$, $V_{REFOUT}$ | | | ±100 | mV | |
| Output Impedance, $V_{REFOUT}$ | | 1 | | Ω | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | $V_{DRIVE}$ −1 | | | V | |
| Input Low Voltage, $V_{INL}$ | | | 0.4 | V | |
| Input Current, $I_{IN}$ | | | ±1 | μA | |
| Input Capacitance, $C_{IN}$[4] | | | 10 | pF | |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | 0.7 × $V_{DRIVE}$ | | | V | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | |
| Floating State Leakage Current | | | ±10 | μA | |
| Floating State Output Capacitance[4] | | | 10 | pF | |
| Output Coding | Straight (Natural) Binary | | | | |
| CONVERSION RATE | | | | | |
| Conversion Time | | | 300 | ns | |
| Track-and-Hold Acquisition Time ($t_{ACQ}$) | | | 70 | ns | Sine wave input |
| | | | 70 | ns | Full-scale step input |
| Throughput Rate | | | 2.5 | MSPS | Parallel Mode 1 |
| | | | 3 | MSPS | Parallel Mode 2 |
| POWER REQUIREMENTS | | | | | |
| $V_{DD}$ | | 5 | | V | ± 5% |
| $V_{DRIVE}$ | 2.7 | | 5.25 | V | |
| $I_{DD}$ | | | | | |
| Normal Mode (Static) | | | 13 | mA | $\overline{CS}$ and $\overline{RD}$ = Logic 1 |
| Normal Mode (Operational) | | | 20 | mA | |
| Nap Mode | | | 0.5 | mA | |
| Standby Mode | | 0.5 | 2 | μA | |
| Power Dissipation | | | | | |
| Normal Mode (Operational) | | | 100 | mW | |
| Nap Mode | | | 2.5 | mW | |
| Standby Mode[5] | | | 10 | μW | |

[1] SINAD figures quoted include external analog input circuit noise contribution of approximately 1 dB.
[2] See the Typical Performance Characteristics section for analog input circuits used.
[3] See the Terminology section.
[4] Sample tested @ 25°C to ensure compliance.
[5] Digital input levels at DGND or $V_{DRIVE}$.

## TIMING CHARACTERISTICS

$AV_{DD}/DV_{DD}$ = 5 V ± 5%, AGND = DGND = 0 V, $V_{REF}$ = external; all specifications $T_{MIN}$ to $T_{MAX}$ and valid for $V_{DRIVE}$ = 2.7 V to 5.25 V, unless otherwise noted.

**Table 2.**

| Parameter[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DATA READ | | | | | |
| Conversion Time | $t_{CONV}$ | | | 300 | ns |
| Quiet Time Before Conversion Start | $t_{QUIET}$ | 100 | | | ns |
| $\overline{CONVST}$ Pulse Width | $t_1$ | 5 | | 100 | ns |
| $\overline{CONVST}$ Falling Edge to $\overline{BUSY}$ Falling Edge | $t_2$ | | | 20 | ns |
| $\overline{CS}$ Falling Edge to $\overline{RD}$ Falling Edge | $t_3$ | 0 | | | ns |
| Data Access Time | $t_4$ | | | 25 | ns |
| $\overline{CONVST}$ Falling Edge to New Data Valid | $t_5$ | | | 30 | ns |
| $\overline{BUSY}$ Rising Edge to New Data Valid | $t_6$ | | | 5 | ns |
| Bus Relinquish Time | $t_7$ | | 10 | | ns |
| $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge | $t_8$ | 0 | | | ns |
| $\overline{CS}$ Pulse Width | $t_{14}$ | 30 | | | ns |
| $\overline{RD}$ Pulse Width | $t_{15}$ | 30 | | | ns |
| DATA WRITE | | | | | |
| WRITE Pulse Width | $t_9$ | 5 | | | ns |
| Data Setup Time | $t_{10}$ | 2 | | | ns |
| Data Hold Time | $t_{11}$ | 6 | | | ns |
| $\overline{CS}$ Falling Edge to WRITE Falling Edge | $t_{12}$ | 5 | | | ns |
| WRITE Falling Edge to $\overline{CS}$ Rising Edge | $t_{13}$ | 0 | | | ns |

[1]All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $AV_{DD}$ to AGND | −0.3 V to +7 V |
| $DV_{DD}$ to DGND | −0.3 V to +7 V |
| $V_{DRIVE}$ to DGND | −0.3 V to +7 V |
| Analog Input Voltage to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| Digital Input Voltage to DGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| REFIN to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supply Pins | ±10 mA |
| Operating Temperature Range | −40°C to +85°C |
| Commercial | |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance | 50°C/W |
| $\theta_{JC}$ Thermal Impedance | 10°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD | 1 kV |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

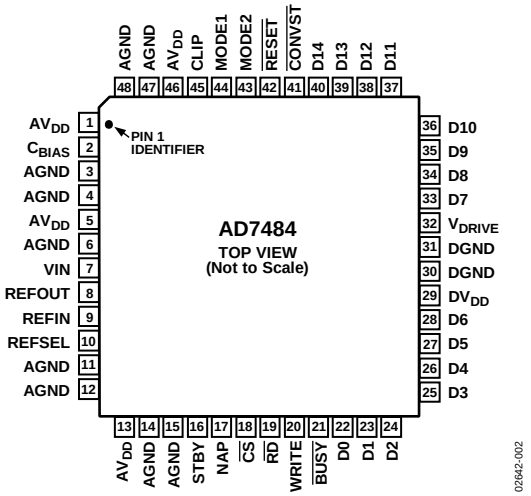


*Figure 2. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 5, 13, 46 | $AV_{DD}$ | Positive Power Supply for Analog Circuitry. |
| 2 | $C_{BIAS}$ | Decoupling Pin for Internal Bias Voltage. A 1 nF capacitor should be placed between this pin and AGND. |
| 3, 4, 6, 11, 12, 14, 15, 47, 48 | AGND | Power Supply Ground for Analog Circuitry. |
| 7 | VIN | Analog Input. Single ended analog input channel. |
| 8 | REFOUT | Reference Output. REFOUT connects to the output of the internal 2.5 V reference buffer. A 470 nF capacitor must be placed between this pin and AGND. |
| 9 | REFIN | Reference Input. A 470 nF capacitor must be placed between this pin and AGND. When using an external voltage reference source, the reference voltage should be applied to this pin. |
| 10 | REFSEL | Reference Decoupling Pin. When using the internal reference, a 1 nF capacitor must be connected from this pin to AGND. When using an external reference source, this pin should be connected directly to AGND. |
| 16 | STBY | Standby Logic Input. When this pin is logic high, the device is placed in standby mode. See the Power Saving section for further details. |
| 17 | NAP | Nap Logic Input. When this pin is logic high, the device is placed in a very low power mode. See the Power Saving section for further details. |
| 18 | $\overline{CS}$ | Chip Select Logic Input. This pin is used in conjunction with $\overline{RD}$ to access the conversion result. The data bus is brought out of three-state and the current contents of the output register driven onto the data lines following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ is also used in conjunction with WRITE to perform a write to the offset register. $\overline{CS}$ can be hardwired permanently low. |
| 19 | $\overline{RD}$ | Read Logic Input. Used in conjunction with $\overline{CS}$ to access the conversion result. |
| 20 | WRITE | Write Logic Input. Used in conjunction with $\overline{CS}$ to write data to the offset register. When the desired offset word has been placed on the data bus, the WRITE line should be pulsed high. It is the falling edge of this pulse that latches the word into the offset register. |
| 21 | $\overline{BUSY}$ | Busy Logic Output. This pin indicates the status of the conversion process. The $\overline{BUSY}$ signal goes low after the falling edge of $\overline{CONVST}$ and stays low for the duration of the conversion. In Parallel Mode 1, the $\overline{BUSY}$ signal returns high when the conversion result has been latched into the output register. In Parallel Mode 2, the $\overline{BUSY}$ signal returns high as soon as the conversion has been completed, but the conversion result does not get latched into the output register until the falling edge of the next $\overline{CONVST}$ pulse. |
| 22 to 28, 33 to 39 | D0 to D13 | Data I/O Bits. D13 is MSB. These are three-state pins that are controlled by $\overline{CS}$, $\overline{RD}$, and WRITE. The operating voltage level for these pins is determined by the $V_{DRIVE}$ input. |
| 29 | $DV_{DD}$ | Positive Power Supply for Digital Circuitry. |
| 30, 31 | DGND | Ground Reference for Digital Circuitry. |
| 32 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface logic of the device operates. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 40 | D14 | Data Output Bit for Overranging. If the overrange feature is not used, this pin should be pulled to DGND via a 100 kΩ resistor. |
| 41 | $\overline{\text{CONVST}}$ | Convert Start Logic Input. A conversion is initiated on the falling edge of the $\overline{\text{CONVST}}$ signal. The input track-and-hold amplifier goes from track mode to hold mode, and the conversion process commences. |
| 42 | $\overline{\text{RESET}}$ | Reset Logic Input. An active low reset pulse must be applied to this pin after power-up to ensure correct operation. A falling edge on this pin resets the internal state machine and terminates a conversion that may be in progress. The contents of the offset register will also be cleared on this edge. Holding this pin low keeps the part in a reset state. |
| 43 | MODE2 | Operating Mode Logic Input. See Table 8 for details. |
| 44 | MODE1 | Operating Mode Logic Input. See Table 8 for details. |
| 45 | CLIP | Logic Input. A logic high on this pin enables output clipping. In this mode, any input voltage that is greater than positive full scale or less than negative full scale will be clipped to all 1s or all 0s, respectively. Further details are given in the Offset/Overrange section. |

# TYPICAL PERFORMANCE CHARACTERISTICS

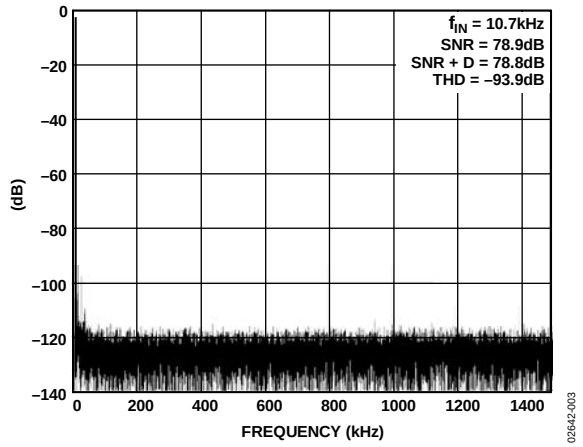


*Figure 3. 64 k FFT Plot with 10 kHz Input Tone*

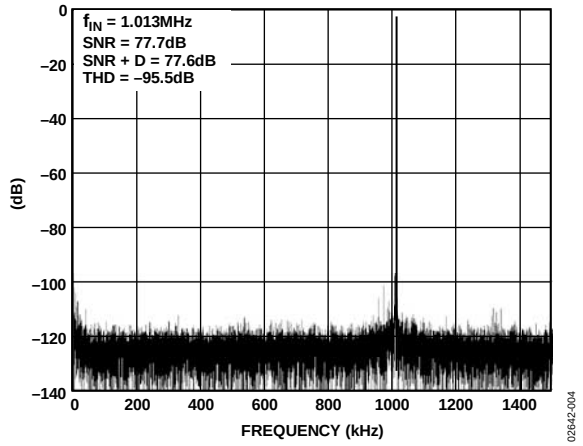


*Figure 4. 64 k FFT Plot with 1 MHz Input Tone*

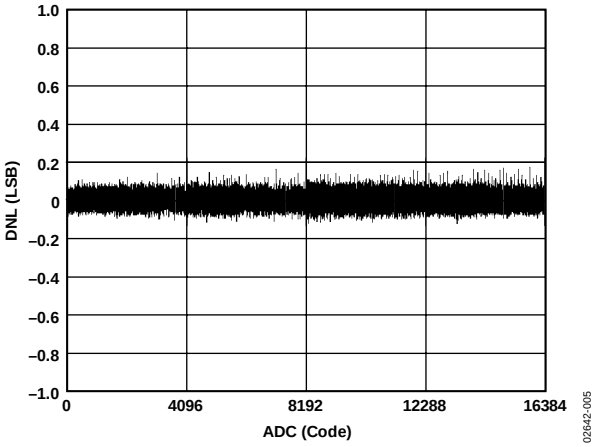


*Figure 5. Typical DNL*

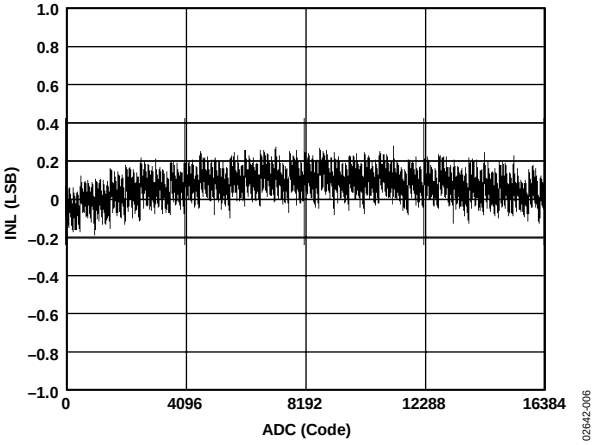


*Figure 6. Typical INL*

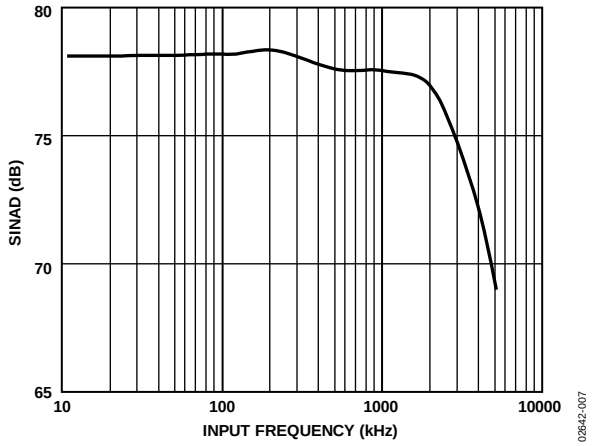


*Figure 7. SINAD vs. Input Tone (AD8021 Input Circuit)*

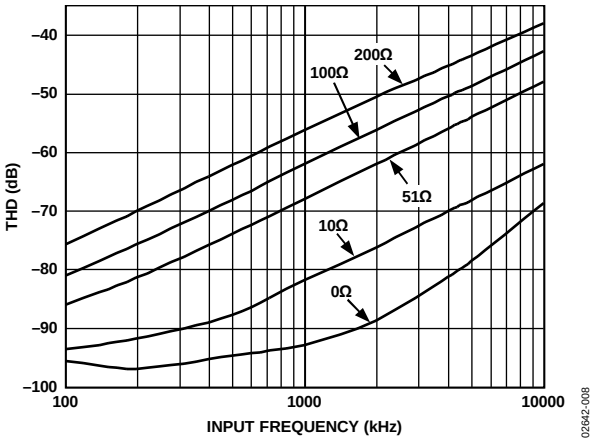


*Figure 8. THD vs. Input Tone for Different Input Resistances*

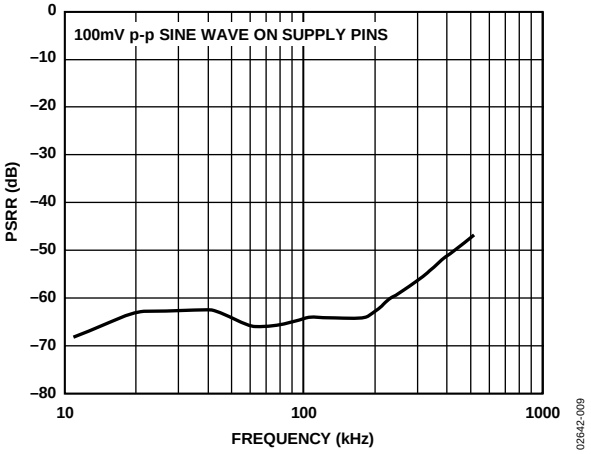


*Figure 9. PSRR Without Decoupling*

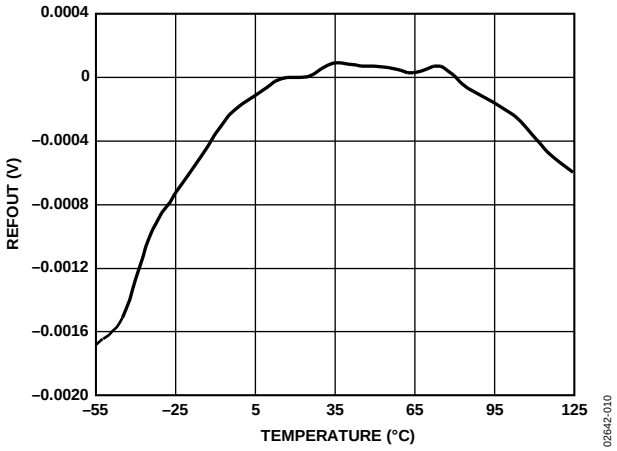


*Figure 10. Reference Error*

# TERMINOLOGY

**Integral Nonlinearity**
The integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

**Differential Nonlinearity**
The differential nonlinearity is the difference between the measured and ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**
The offset error is the deviation of the first code transition (00…000) to (00…001) from the ideal, that is, AGND + 0.5 LSB.

**Gain Error**
The gain error is the deviation of the last code transition (111…110) to (111…111) from the ideal, that is, $V_{REF}$ − 1.5 LSB, after the offset error has been adjusted out.

**Track-and-Hold Acquisition Time**
The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track-and-hold returns to track mode).

**Signal-to-Noise + Distortion (SINAD) Ratio**
The SINAD ratio is the measured ratio of signal-to-noise + distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}Noise + Distortion = (6.02N + 1.76)\text{dB}$$

Therefore, this is 86.04 dB for a 14-bit converter.

**Total Harmonic Distortion (THD)**
The THD is the ratio of the rms sum of the harmonics to the fundamental. It is defined as

$$THD\,(\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through the sixth harmonics.

**Peak Harmonic or Spurious Noise**
The peak harmonic or spurious noise is the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. The value of this specification is usually determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Intermodulation Distortion**
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), whereas the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7484 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, whereas the third order terms are usually at a frequency close to the input frequencies. As a result, the second order and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

# CIRCUIT DESCRIPTION

## CONVERTER OPERATION

The AD7484 is a 14-bit algorithmic successive approximation ADC based around a capacitive DAC. It provides the user with track-and-hold, reference, an ADC, and versatile interface logic functions on a single chip. The normal analog input signal range that the AD7484 can convert is 0 V to 2.5 V. By using the offset and overrange features on the ADC, the AD7484 can convert analog input signals from −200 mV to +2.7 V while operating from a single 5 V supply. The part requires a 2.5 V reference, which can be provided from the internal reference or an external reference source. Figure 11 shows a simplified schematic of the ADC. The control logic, SAR, and capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back to a balanced condition.

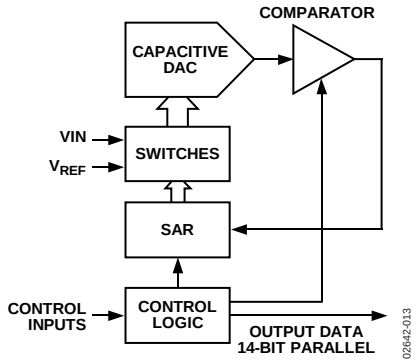


*Figure 11. Simplified Block Diagram of the AD7484*

Conversion is initiated on the AD7484 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the track-and-hold goes from track mode to hold mode and the conversion sequence is started. Conversion time for the part is 300 ns. Figure 12 shows the ADC during conversion. When conversion starts, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The ADC then runs through its successive-approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.

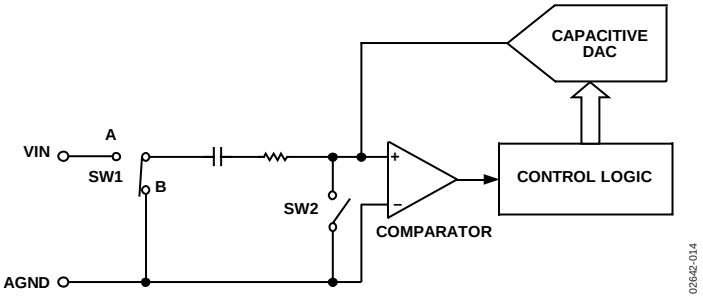


*Figure 12. ADC Conversion Phase*

At the end of conversion, the track-and-hold returns to track mode and the acquisition time begins. The track-and-hold acquisition time is 70 ns. Figure 13 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition, and the sampling capacitor acquires the signal on $V_{IN}$.

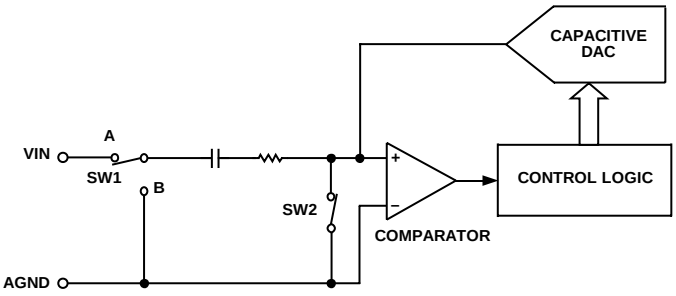


*Figure 13. ADC Acquisition Phase*

## ANALOG INPUT

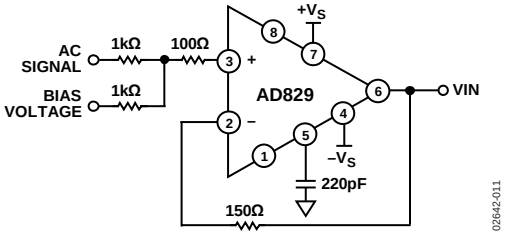


*Figure 14. Analog Input Circuit Used for 10 kHz Input Tone*

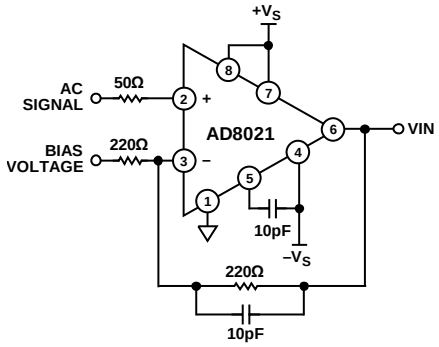


*Figure 15. Analog Input Circuit Used for 1 MHz Input Tone*

Figure 14 shows the analog input circuit used to obtain the data for the fast fourier transfer (FFT) plot shown in Figure 3. The circuit uses the AD829 op amp as the input buffer. A bipolar analog signal is applied and biased up with a stable, low noise dc voltage connected to the labeled terminal, as shown in Figure 11. A 220 pF compensation capacitor is connected between Pin 5 of the AD829 and the analog ground plane. The AD829 is supplied with +12 V and −12 V supplies. The supply pins are decoupled as close to the device as possible with both a 0.1 µF and a 10 µF capacitor connected to each pin. In each case, the 0.1 µF capacitor should be the closer of the two caps to the device. More information on the AD829 is available at www.analog.com.

For higher input bandwidth applications, the AD8021 op amp (also available as a dual AD8022 op amp) is the recommended choice to drive the AD7484. Figure 15 shows the analog input circuit used to obtain the data for the FFT plot shown in Figure 4. A bipolar analog signal is applied to the terminal and biased up with a stable, low noise dc voltage connected, as shown in Figure 12. A 10 pF compensation capacitor is connected between Pin 5 of the AD8021 and the negative supply. The AD8021 is supplied with +12 V and −12 V supplies. The supply pins are decoupled as close to the device as possible, with both a 0.1 µF and a 10 µF capacitor connected to each pin. In each case, the 0.1 µF capacitor should be the closer of the two caps to the device. The AD8021 logic reference pin is tied to analog ground, and the $\overline{\text{DISABLE}}$ pin is tied to the positive supply. Detailed information on the AD8021 is available at www.analog.com.

## ADC TRANSFER FUNCTION

The output coding of the AD7484 is straight binary. The designed code transitions occur midway between the successive integer LSB values, that is, 1/2 LSB, 3/2 LSB, and so on. The LSB size is $V_{REF}$/16,384. The nominal transfer characteristic for the AD7484 is shown in Figure 16. This transfer characteristic may be shifted as detailed in the Offset/Overrange section.

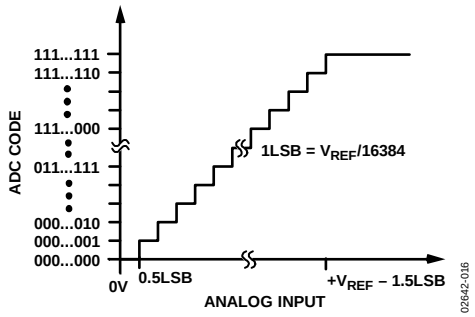


*Figure 16. AD7484 Transfer Characteristic*

## POWER SAVING

The AD7484 uses advanced design techniques to achieve very low power dissipation at high throughput rates. In addition, the AD7484 features two power saving modes, nap and standby. These modes are selected by bringing either the NAP pin or the STBY pin to a logic high, respectively.

When operating the AD7484 in normal fully powered mode, the current consumption is 18 mA during conversion and the quiescent current is 12 mA. Operating at a throughput rate of 1 MSPS, the conversion time of 300 ns contributes 27 mW to the overall power dissipation.

(300 ns/1 µs) × (5 V × 18 mA) = 27 mW

For the remaining 700 ns of the cycle, the AD7484 dissipates 42 mW of power.

(700 ns/1 µs) × (5 V × 12 mA) = 42 mW

Therefore, the power dissipated during each cycle is

27 mW + 42 mW = 69 mW

Figure 17 shows the AD7484 conversion sequence operating in normal mode.

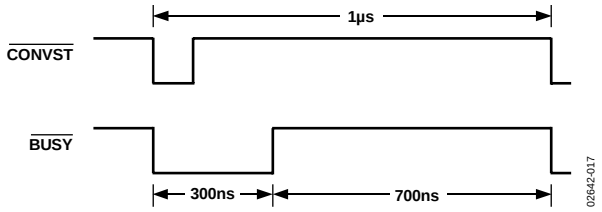


*Figure 17. Normal Mode Power Dissipation*

In nap mode, almost all of the internal circuitry is powered down. In this mode, the power dissipation is reduced to 2.5 mW. When using an external reference, there must be a minimum of 300 ns from exiting nap mode to initiating a conversion. This is necessary to allow the internal circuitry to settle after power-up and for the track-and-hold to properly acquire the analog input signal. The internal reference cannot be used in conjunction with the nap mode.

If the AD7484 is put into nap mode after each conversion, the average power dissipation is reduced, but the throughput rate is limited by the power-up time. Using the AD7484 with a throughput rate of 500 kSPS while placing the part in nap mode after each conversion results in average power dissipation as follows:

The power-up phase contributes

(300 ns/2 µs) × (5 V × 12 mA) = 9 mW

The conversion phase contributes

(300 ns/2 µs) × (5 V × 18 mA) = 13.5 mW

While in nap mode for the rest of the cycle, the AD7484 dissipates only 1.75 mW of power.

(1400 ns/2 µs) × (5 V × 0.5 mA) = 1.75 mW

Therefore, the power dissipated during each cycle is

9 mW + 13.5 mW + 1.75 mW = 24.25 mW

Figure 18 shows the AD7484 conversion sequence when the part is put into nap mode after each conversion.

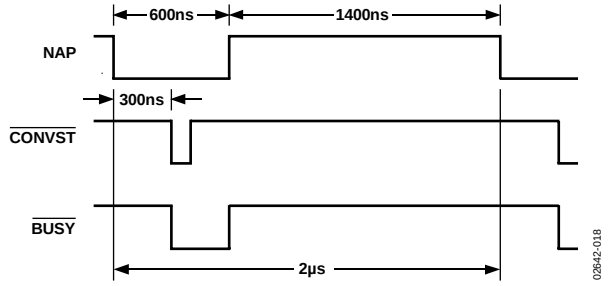


*Figure 18. Nap Mode Power Dissipation*

Figure 19 and Figure 20 show a typical graphical representation of power vs. throughput for the AD7484 when in normal mode and nap mode, respectively.

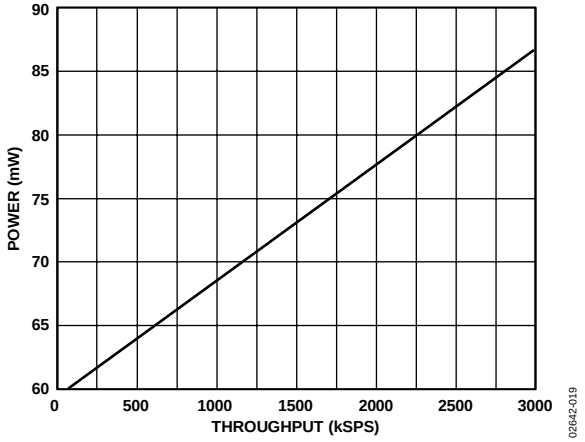


*Figure 19. Normal Mode, Power vs. Throughput*

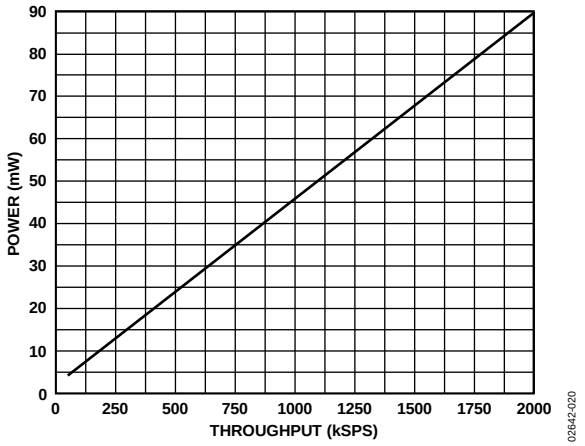


*Figure 20. Nap Mode, Power vs. Throughput*

In standby mode, all internal circuitry is powered down and the power consumption of the AD7484 is reduced to 10 µW. The power-up time necessary before a conversion can be initiated is longer because more of the internal circuitry has been powered down. In using the internal reference of the AD7484, the ADC must be brought out of standby mode 500 ms before a conversion is initiated. Initiating a conversion before the required power-up time has elapsed results in incorrect conversion data. If an external reference source is used and kept powered up while the AD7484 is in standby mode, the power-up time required is reduced to 80 µs.

## OFFSET/OVERRANGE

The AD7484 provides a ±8% overrange capability as well as a programmable offset register. The overrange capability is achieved by the use of a 15th bit (D14) and the CLIP input. If the CLIP input is at logic high and the contents of the offset register are 0, then the AD7484 operates as a normal 14-bit ADC. If the input voltage is greater than the full-scale voltage, the data output from the ADC is all 1s. Similarly, if the input voltage is lower than the zero-scale voltage, the data output from the ADC is all 0s. In this case, D14 acts as an overrange indicator. It is set to 1 if the analog input voltage is outside the nominal 0 V to 2.5 V range.

The default contents of the offset register are 0. If the offset register contains any value other than 0, the contents of the register are added to the SAR result at the end of conversion. This has the effect of shifting the transfer function of the ADC as shown in Figure 21 and Figure 22. However, it should be noted that with the CLIP input set to logic high, the maximum and minimum codes that the AD7484 can output are 0x3FFF and 0x0000, respectively. Further details are given in Table 5 and Table 6.

Figure 21 shows the effect of writing a positive value to the offset register. For example, if the contents of the offset register contained the value 1024, then the value of the analog input voltage for which the ADC transitions from reading all 0s to 000…001 (the bottom reference point) is

0.5 LSB − (1024 LSB) = −156.326 mV

The analog input voltage for which the ADC reads full-scale (0x3FFF) in this example is

2.5 − 1.5 LSB − (1024 LSB) = 2.34352 V

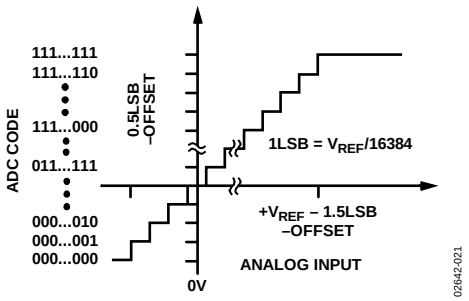


*Figure 21. Transfer Characteristic with Positive Offset*

The effect of writing a negative value to the offset register is shown in Figure 22. If a value of −512 is written to the offset register, the bottom end reference point occurs at

0.5 LSB − (−512 LSB) = 78.20 mW

Following this, the analog input voltage needed to produce a full-scale (0x3FFF) result from the ADC is

2.5 V − 1.5 LSB − (−512 LSB) = 2.5779 V

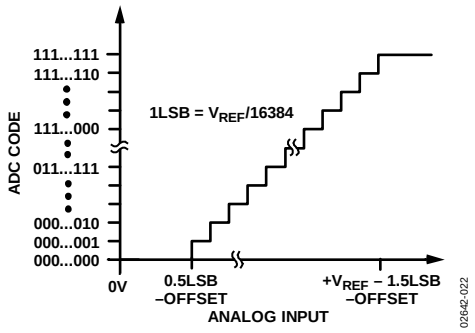


*Figure 22. Transfer Characteristic with Negative Offset*

Table 5 shows the expected ADC result for a given analog input voltage with different offset values and with CLIP tied to logic high. The combined advantages of the offset and overrange features of the AD7484 are shown in Table 6. Table 6 shows the same range of analog input and offset values as Table 5 but with the clipping feature disabled.

**Table 5. Clipping Enabled (CLIP = 1)**

| | ADC DATA, D[0:13] | | | |
|---|---|---|---|---|
| **Offset VIN** | **−512** | **0** | **+1024** | **D14** |
| −200 mV | 0 | 0 | 0 | 1 1 1 |
| −156.3 mV | 0 | 0 | 0 | 1 1 0 |
| 0 V | 0 | 0 | 1024 | 1 0 0 |
| +78.2 mV | 0 | 512 | 1536 | 0 0 0 |
| +2.3434 V | 14,846 | 15,358 | 16,383 | 0 0 0 |
| +2.5 V | 15,871 | 16,383 | 16,383 | 0 0 1 |
| +2.5782 V | 16,383 | 16,383 | 16,383 | 0 1 1 |
| +2.7 V | 16,383 | 16,383 | 16,383 | 1 1 1 |

**Table 6. Clipping Disabled (CLIP = 0)**

| | ADC DATA, D[0:14] | | |
|---|---|---|---|
| **Offset VIN** | **−512** | **0** | **+1024** |
| −200 mV | −1823 | −1311 | −287 |
| −156.3 mV | −1536 | −1024 | 0 |
| 0 V | −512 | 0 | 1024 |
| +78.2 mV | 0 | 512 | 1536 |
| +2.3434 V | 14,846 | 15,358 | 16,382 |
| +2.5 V | 15,872 | 16,384 | 17,408 |
| +2.5782 V | 16,384 | 16,896 | 17,920 |
| +2.7 V | 17,183 | 17,695 | 18,719 |

If the CLIP input is at logic low, the overrange indicator is disabled and the AD7484 can achieve output codes outside the nominal 14-bit range of 0 to 16,383 (see Table 6). D14 acts as an indicator that the ADC is outside this nominal range. If the ADC is outside this nominal range on the negative side, the ADC outputs a twos complement code and if the ADC is outside the range on the positive side, the ADC outputs a straight binary code as normal. If D14 is Logic 1, D13 indicates if the ADC is out of range on the positive or negative side. If DB13 is Logic 1, the ADC is outside the nominal range on the negative side and the output code is a 15-bit twos complement number (a negative number). If D13 is Logic 0, the ADC is outside the nominal range on the positive side and the output code is a 15-bit straight binary code (see Table 7).

**Table 7. DB14, DB13 Decoding, CLIP = 0**

| DB14 | DB13 | Output Coding |
|---|---|---|
| 0 | 0 | Straight binary–inside nominal range |
| 0 | 1 | Straight binary–inside nominal range |
| 1 | 0 | Straight binary–outside nominal range |
| 1 | 1 | Twos complement–outside nominal range |

Values from −1310 to +1310 can be written to the offset register. These values correspond to an offset of ±200 mV. A write to the offset register is performed by writing a 13-bit word to the part, as detailed in the Parallel Interface section. The 12 LSBs of the 15-bit word contain the offset value, whereas the 3 MSBs must be set to 0. Failure to write 0s to the 3 MSBs may result in the incorrect operation of the device.

## PARALLEL INTERFACE

The AD7484 features two parallel interfacing modes. These modes are selected by the mode pins (see Table 8).

**Table 8. Operating Modes**

| Operating Mode | Mode 2 | Mode 1 |
|---|---|---|
| Do Not Use | 0 | 0 |
| Parallel Mode 1 | 0 | 1 |
| Parallel Mode 2 | 1 | 0 |
| Do Not Use | 1 | 1 |

In Parallel Mode 1, the data in the output register is updated on the rising edge of $\overline{BUSY}$ at the end of a conversion and is available for reading almost immediately afterwards. Using this mode, throughput rates of up to 2.5 MSPS can be achieved. This mode is to be used if the conversion data is required immediately after the conversion is completed. An example where this may be of use is if the AD7484 is operating at much lower throughput rates in conjunction with the nap mode (for power saving reasons), and the input signal is being compared with set limits within the DSP or other controller. If the limits are exceeded, the ADC is brought immediately into full power operation and commences sampling at full speed. Figure 31 shows a timing diagram for the AD7484 operating in Parallel Mode 1 with both $\overline{CS}$ and $\overline{RD}$ tied low.

In Parallel Mode 2, the data in the output register is not updated until the next falling edge of $\overline{CONVST}$. This mode can be used where a single sample delay is not vital to the system operation, and conversion speeds of greater than 2.5 MSPS are desired. For example, this may occur in a system where a large amount of samples are taken at high speed before an FFT is performed for frequency analysis of the input signal. Figure 32 shows a timing diagram for the AD7484 operating in Parallel Mode 2 with both $\overline{CS}$ and $\overline{RD}$ tied low.

Data must not be read from the AD7484 while a conversion is taking place. For this reason, if operating the AD7484 at throughput speeds greater than 2.5 MSPS, it is necessary to tie both the $\overline{CS}$ pin and $\overline{RD}$ pin on the AD7484 low and use a buffer on the data lines. This situation may also arise in the case where a read operation cannot be completed in the time after the end of one conversion and the start of the quiet period before the next conversion.

The maximum slew rate at the input of the ADC must be limited to 500 V/µs while $\overline{BUSY}$ is low to avoid corrupting the ongoing conversion. In any multiplexed application where the channel is switched during conversion, this is to happen as soon as possible after the $\overline{BUSY}$ falling edge.

### Reading Data from the AD7484

Data is read from the part via a 15-bit parallel data bus with the standard $\overline{CS}$ and $\overline{RD}$ signals. The $\overline{CS}$ and $\overline{RD}$ signals are internally gated to enable the conversion result onto the data bus. The data lines D0 to D14 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low. Therefore, $\overline{CS}$ can be permanently tied logic low if required, and the $\overline{RD}$ signal used to access the conversion result. Figure 29 shows a timing specification called $t_{QUIET}$. This is the amount of time that must be left after any data bus activity before the next conversion is initiated.

### Writing to the AD7484

The AD7484 features a user accessible offset register. This allows the bottom of the transfer function to be shifted by ±200 mV. This feature is explained in more detail in the Offset/Overrange section.

To write to the offset register, a 15-bit word is written to the AD7484 with the 12 LSBs containing the offset value in twos complement format. The 3 MSBs must be set to 0. The offset value must be within the range −1310 to +1310, corresponding to an offset from −200 mV to +200 mV. The value written to the offset register is stored and used until power is removed from the device, or the device is reset. The value stored may be updated at any time between conversions by another write to the device. Table 9 shows some examples of offset register values and their effective offset voltage. Figure 30 shows a timing diagram for writing to the AD7484.

**Table 9. Offset Register Examples**

| Code (Decimal) | D14 to D12 | D11 to D0 (Twos Complement) | Offset (mV) |
|---|---|---|---|
| −1310 | 000 | 1010 1110 0010 | −200 |
| −512 | 000 | 1110 0000 0000 | −78.12 |
| +256 | 000 | 0001 0000 0000 | +39.06 |
| +1310 | 000 | 0101 0001 1110 | +200 |

### Driving the $\overline{CONVST}$ Pin

To achieve the specified performance from the AD7484, the $\overline{CONVST}$ pin must be driven from a low jitter source. Because the falling edge on the $\overline{CONVST}$ pin determines the sampling instant, any jitter that may exist on this edge appears as noise when the analog input signal contains high frequency components. The relationship between the analog input frequency ($f_{IN}$), timing jitter ($t_j$), and resulting SNR is given by

$$SNR_{JITTER}\,(\text{dB}) = 10\log\frac{1}{(2\pi\times f_{IN}\times t_j)^2}$$

For example, if the desired SNR due to jitter is 100 dB with a maximum full-scale analog input frequency of 1.5 MHz, ignoring all other noise sources, the result is an allowable jitter on the $\overline{CONVST}$ falling edge of 1.06 ps. For a 14-bit converter (ideal SNR = 86.04 dB), the allowable jitter is greater than 1.06 ps, but due consider-ation must be given to the design of the $\overline{CONVST}$ circuitry to achieve 14-bit performance with large analog input frequencies.

### Typical Connection

Figure 23 shows a typical connection diagram for the AD7484 operating in Parallel Mode 1. Conversion is initiated by a falling edge on $\overline{CONVST}$. When $\overline{CONVST}$ goes low, the $\overline{BUSY}$ signal goes low, and at the end of conversion, the rising edge of $\overline{BUSY}$ is used to activate an interrupt service routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated to read the 14 data bits (15 bits if using the overrange feature).

In Figure 23, the $V_{DRIVE}$ pin is tied to $DV_{DD}$, which results in logic output levels being either 0 V or $DV_{DD}$. The voltage applied to $V_{DRIVE}$ controls the voltage value of the output logic signals. For example, if $DV_{DD}$ is supplied by a 5 V supply and $V_{DRIVE}$ is supplied by a 3 V supply, the logic output levels are either 0 V or 3 V. This feature allows the AD7484 to interface to 3 V devices while still enabling the ADC to process signals at a 5 V supply.

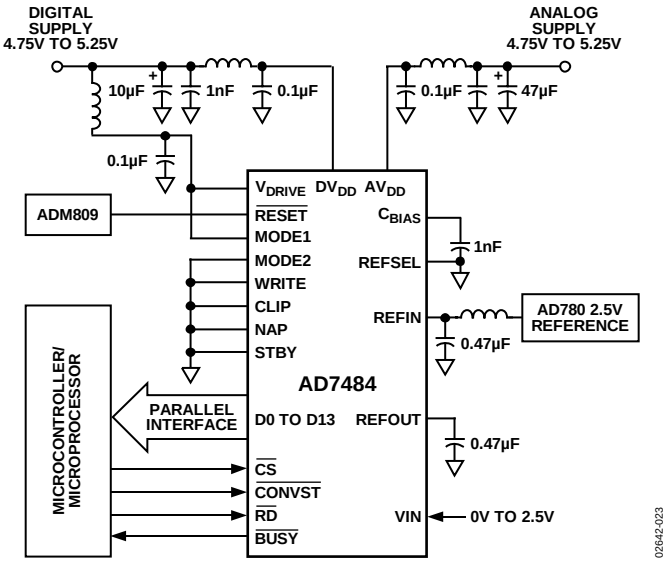


*Figure 23. Typical Connection Diagram*

## BOARD LAYOUT AND GROUNDING

For optimum performance from the AD7484, it is recommended that a PCB with a minimum of three layers be used. One of these layers, preferably the middle layer, should be as complete a ground plane as possible to give the best shielding. The board should be designed in such a way that the analog and digital circuitry is separated and confined to certain areas of the board. This practice, along with not running digital and analog lines close together, helps to avoid coupling digital noise onto analog lines.

The power supply lines to the AD7484 are to be approximately 3 mm wide to provide low impedance paths and reduce the effects of glitches on the power supply lines. It is vital that good decoupling also be present. A combination of ferrites and decoupling capacitors should be used, as shown in Figure 23.The decoupling capacitors are to be as close to the supply pins as possible. This is made easier by the use of multilayer boards. The signal traces from the AD7484 pins can be run on the top layer, while the decoupling capacitors and ferrites can be mounted on the bottom layer where the power traces exist. The ground plane between the top and bottom planes provides excellent shielding.

Figure 24 to Figure 28 show a sample layout of the board area immediately surrounding the AD7484. Pin 1 is the bottom left corner of the device. The black area in each figure indicates the ground plane present on the middle layer. Figure 24 shows the top layer where the AD7484 is mounted with vias to the bottom routing layer highlighted. Figure 25 shows the bottom layer silkscreen where the decoupling components are soldered directly beneath the device. Figure 26 shows the top and bottom routing layers overlaid. Figure 27 shows the bottom layer where the power routing is with the same vias highlighted. Figure 28 shows the silkscreen overlaid on the solder pads for the decoupling components, which are C1 to C6: 100 nF, C7 to C8: 470 nF, C9: 1 nF, and L1 to L4: Meggit-Sigma Chip Ferrite Beads (BMB2A0600RS2).

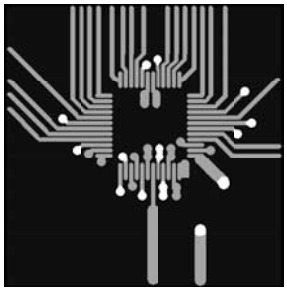


*Figure 24. Top Layer Routing*

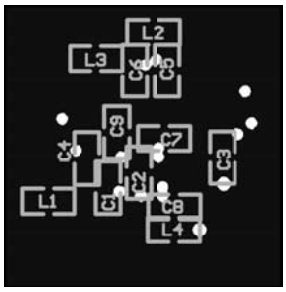


*Figure 25. Bottom Layer Silkscreen*

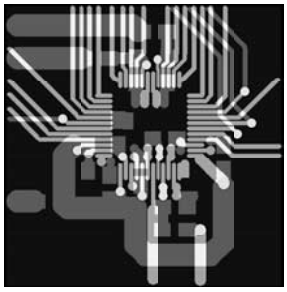


*Figure 26. Top and Bottom Routing Layers*

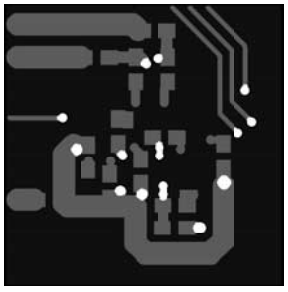


*Figure 27. Bottom Layer Routing*

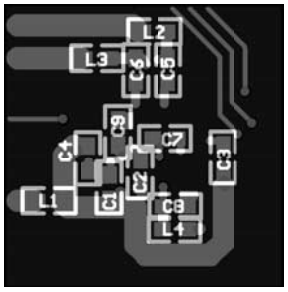


*Figure 28. Silkscreen and Bottom Layer Routing*

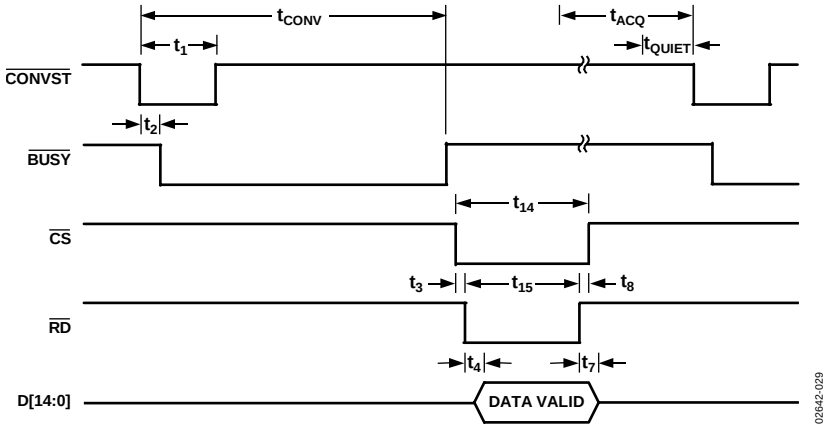


*Figure 29. Parallel Mode READ Cycle*

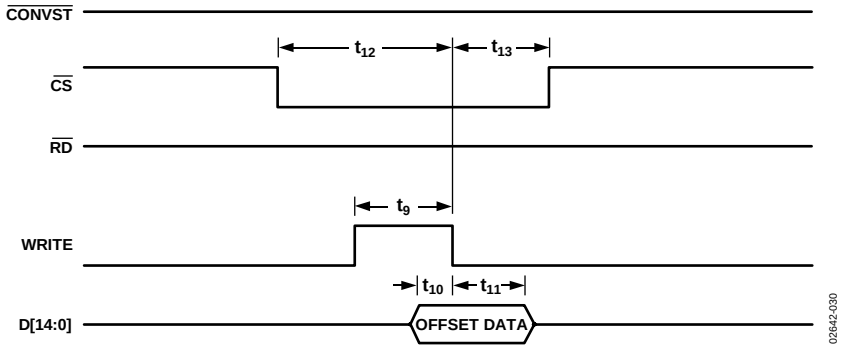


*Figure 30. Parallel Mode WRITE Cycle*

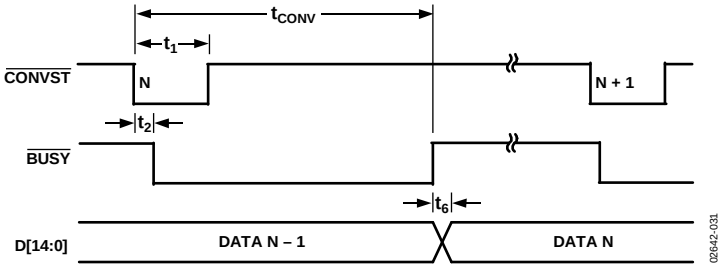


*Figure 31. Parallel Mode 1 READ Cycle*

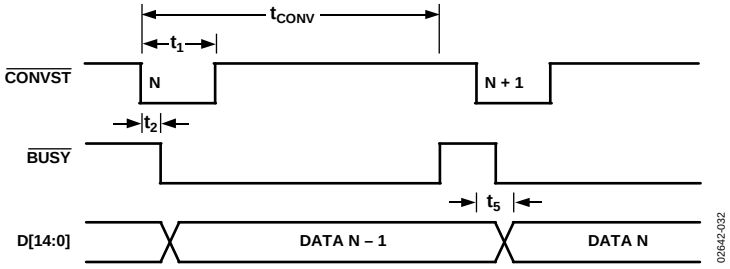


*Figure 32. Parallel Mode 2 READ Cycle*

# OUTLINE DIMENSIONS

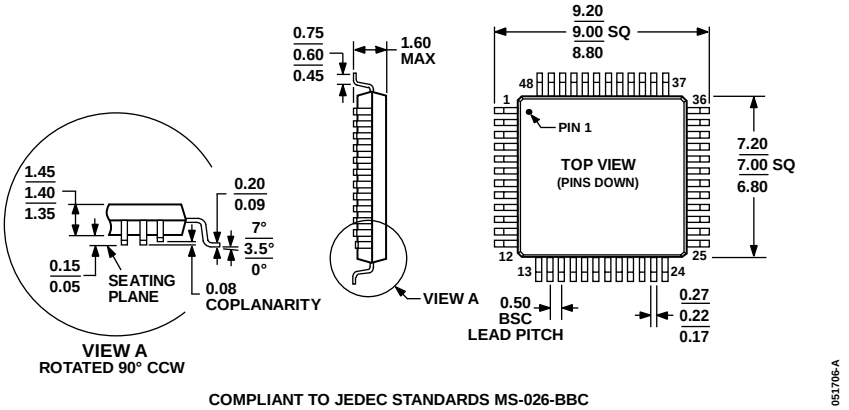


*Figure 33. 48-Lead Plastic Quad Flatpack (LQFP)*
*[ST-48]*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7484BSTZ | −40°C to +85°C | 48-Lead Plastic Quad Flatpack Package (LQFP) | ST-48 |
| EVAL-AD7484CBZ | | Evaluation Board[2] | |
| EVAL-CONTROLBRD2Z | | Controller Board[3] | |

[1] Z = RoHS Compliant Part.
[2] This can be used as a standalone evaluation board or in conjunction with the controller board for evaluation/demonstration purposes.
[3] This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

# NOTES