High Gain Bandwidth Product, Precision *Fast FET*™ Op Amp

Data Sheet **AD8067**

FEATURES

FET input amplifier: 0.6 pA input bias current
Stable for gains ≥8
High speed
  54 MHz, −3 dB bandwidth (G = +10)
  640 V/µs slew rate
Low noise
  6.6 nV/√Hz
  0.6 fA/√Hz
Low offset voltage (1.0 mV max)
Wide supply voltage range: 5 V to 24 V
No phase reversal
Low input capacitance
Single-supply and rail-to-rail output
Excellent distortion specs: SFDR 95 dBc @ 1 MHz
High common-mode rejection ratio: −106 dB
Low power: 6.5 mA typical supply current
Low cost
Small packaging: SOT-23-5

APPLICATIONS

Photodiode preamplifiers
Precision high gain amplifiers
High gain, high bandwidth composite amplifiers

CONNECTION DIAGRAM (TOP VIEW)

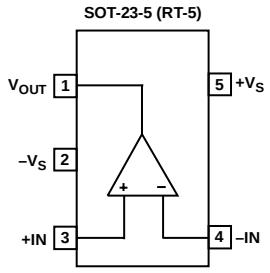

Figure 1.

GENERAL DESCRIPTION

The AD8067 *FastFET* amp is a voltage feedback amplifier with FET inputs offering wide bandwidth (54 MHz @ G = +10) and high slew rate (640 V/µs). The AD8067 is fabricated in a proprietary, dielectrically isolated eXtra Fast Complementary Bipolar process (XFCB) that enables high speed, low power, and high performance FET input amplifiers.

The AD8067 is designed to work in applications that require high speed and low input bias current, such as fast photodiode preamplifiers. As required by photodiode applications, the laser trimmed AD8067 has excellent dc voltage offset (1.0 mV max) and drift (15 µV/°C max).

The FET input bias current (5 pA max) and low voltage noise (6.6 nV/√Hz) also contribute to making it appropriate for precision applications. With a wide supply voltage range (5 V to 24 V) and rail-to-rail output, the AD8067 is well suited for a variety of applications that require wide dynamic range and low distortion.

The AD8067 amplifier is available in a SOT-23-5 package and is rated to operate over the industrial temperature range of –40°C to +85°C.

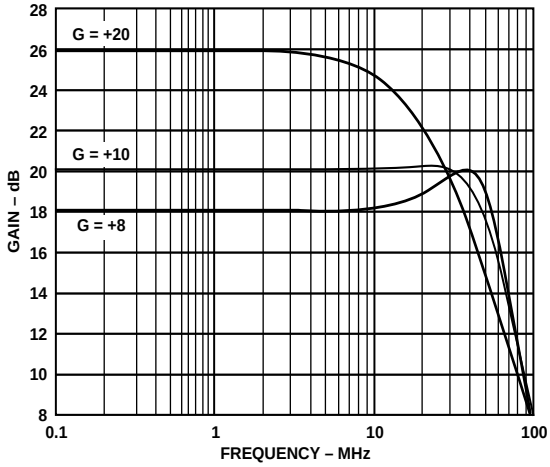

Figure 2. Small Signal Frequency Response

Rev. B

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TABLE OF CONTENTS

REVISION HISTORY

4/12—Rev. A to Rev. B

Changes to Basic Frequency Response Section ... 13
Changes to Figure 54 Caption ... 19
Changes to Figure 55 Caption ... 20
Updated Outline Dimensions ... 22
Changes to Ordering Guide ... 22

5/06—Rev. 0 to Rev. A

Changes to Figure 51 ... 18
Changes to Figure 54 ... 19
Changes to Figure 57 ... 21
Updated Outline Dimensions ... 22
Changes to Ordering Guide ... 22

11/02—Revision 0: Initial Version

SPECIFICATIONS FOR ±5 V

V_S = ±5 V (@ T_A = +25°C, G = +10, R_F = R_L =1 kΩ, unless otherwise noted.)

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p	39	54		MHz
	V_O = 2 V p-p		54		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		8		MHz
Output Overdrive Recovery Time (Pos/Neg)	V_I = ±0.6 V		115/190		ns
Slew Rate	V_O = 5 V step	500	640		V/µs
Settling Time to 0.1%	V_O = 5 V step		27		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, 2 V p-p		95		dBc
	f_C = 1 MHz, 8 V p-p		84		dBc
	f_C = 5 MHz, 2 V p-p		82		dBc
	f_C = 1 MHz, 2 V p-p, R_L = 150 Ω		72		dBc
Input Voltage Noise	f = 10 kHz		6.6		nV/√Hz
Input Current Noise	f = 10 kHz		0.6		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.2	1.0	mV
Input Offset Voltage Drift			1	15	µV/°C
Input Bias Current			0.6	5	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			0.2	1	pA
	T_{MIN} to T_{MAX}		1		pA
Open-Loop Gain	V_O = ±3 V	103	119		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000||1.5		GΩ||pF
Differential Input Impedance			1000||2.5		GΩ||pF
Input Common-Mode Voltage Range		−5.0		2.0	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −1 V to +1 V	−85	−106		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	−4.86 to +4.83	−4.92 to +4.92		V
	R_L = 150 Ω		−4.67 to +4.72		V
Output Current	SFDR > 60 dBc, f = 1 MHz		30		mA
Short Circuit Current			105		mA
Capacitive Load Drive	30% overshoot		120		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current			6.5	6.8	mA
Power Supply Rejection Ratio (PSRR)		−90	−109		dB

SPECIFICATIONS FOR +5 V

V_S = +5 V (@ T_A = +25°C, G = +10, R_L = R_F = 1 kΩ, unless otherwise noted.)

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p	36	54		MHz
	V_O = 2 V p-p		54		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		8		MHz
Output Overdrive Recovery Time (Pos/Neg)	V_I = +0.6 V		150/200		ns
Slew Rate	V_O = 3 V step	390	490		V/µs
Settling Time to 0.1%	V_O = 2 V step		25		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, 2 V p-p		86		dBc
	f_C = 1 MHz, 4 V p-p		74		dBc
	f_C = 5 MHz, 2 V p-p		60		dBc
	f_C = 1 MHz, 2 V p-p, R_L = 150 Ω		72		dBc
Input Voltage Noise	f = 10 kHz		6.6		nV/√Hz
Input Current Noise	f = 10 kHz		0.6		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.2	1.0	mV
Input Offset Voltage Drift			1	15	µV/°C
Input Bias Current			0.5	5	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			0.1	1	pA
Open-Loop Gain	V_O = 0.5 V to 4.5 V	100	117		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000||2.3		GΩ||pF
Differential Input Impedance			1000||2.5		GΩ||pF
Input Common-Mode Voltage Range		0		2.0	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0.5 V to 1.5 V	−81	−98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	0.07 to 4.89	0.03 to 4.94		V
	R_L =150 Ω		0.08 to 4.83		V
Output Current	SFDR > 60 dBc, f = 1 MHz		22		mA
Short Circuit Current			95		mA
Capacitive Load Drive	30% overshoot		120		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current			6.4	6.7	mA
Power Supply Rejection Ratio (PSRR)		−87	−103		dB

SPECIFICATIONS FOR ±12 V

V_S = ±12 V (@ T_A = +25°C, G = +10, R_L = R_F = 1 kΩ, unless otherwise noted.)

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.2 V p-p	39	54		MHz
	V_O = 2 V p-p		53		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		8		MHz
Output Overdrive Recovery Time (Pos/Neg)	V_I = ±1.5 V		75/180		ns
Slew Rate	V_O = 5 V step	500	640		V/µs
Settling Time to 0.1%	V_O = 5 V step		27		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, 2 V p-p		92		dBc
	f_C = 1 MHz, 20 V p-p		84		dBc
	f_C = 5 MHz, 2 V p-p		74		dBc
	f_C = 1 MHz, 2 V p-p, R_L = 150 Ω		72		dBc
Input Voltage Noise	f = 10 kHz		6.6		nV/√Hz
Input Current Noise	f = 10 kHz		0.6		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.2	1.0	mV
Input Offset Voltage Drift			1	15	µV/°C
Input Bias Current			1.0	5	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			0.2	1	pA
Open-Loop Gain	V_O = ±10 V	107	119		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000||1.5		GΩ||pF
Differential Input Impedance			1000||2.5		GΩ||pF
Input Common-Mode Voltage Range		−12.0		+9.0	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −1 V to +1 V	−89	−108		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	−11.70 to +11.70	−11.85 to +11.84		V
	R_L = 500 Ω		−11.31 to +11.73		V
Output Current	SFDR > 60 dBc, f = 1 MHz		26		mA
Short Circuit Current			125		mA
Capacitive Load Drive	30% overshoot		120		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current			6.6	7.0	mA
Power Supply Rejection Ratio (PSRR)		−86	−97		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	V_{EE} – 0.5 V to V_{CC} + 0.5 V
Differential Input Voltage	1.8 V
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The associated raise in junction temperature (T_J) on the die limits the maximum safe power dissipation in the AD8067 package. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8067. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package. RMS output voltages should be considered.

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

If R_L is referenced to V_{S-} as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply:

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation effectively, reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the SOT-23-5 (180°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

It should be noted that for every 10°C rise in temperature, I_B approximately doubles (see Figure 22).

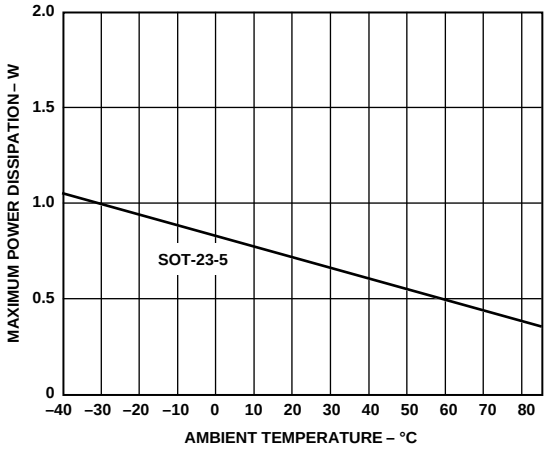

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: V_S = ±5 V (@ T_A = +25°C, G = +10, R_L = R_F = 1 kΩ, unless otherwise noted.)

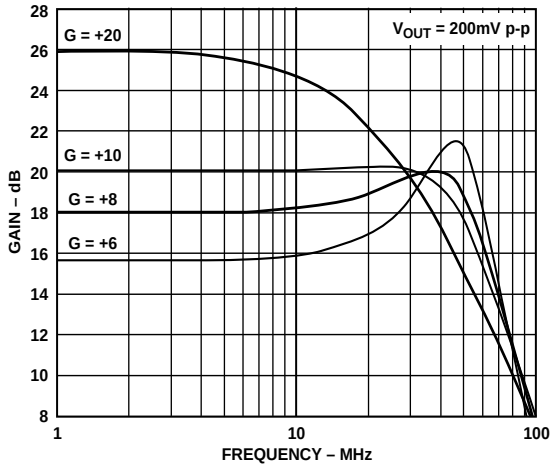

Figure 4. Small Signal Frequency Response for Various Gains

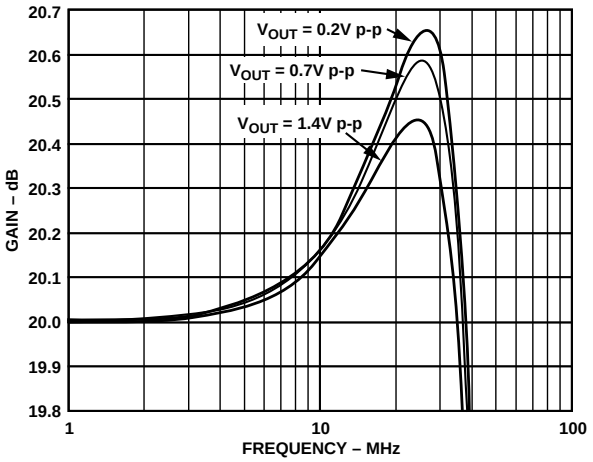

Figure 7. 0.1 dB Flatness Frequency Response

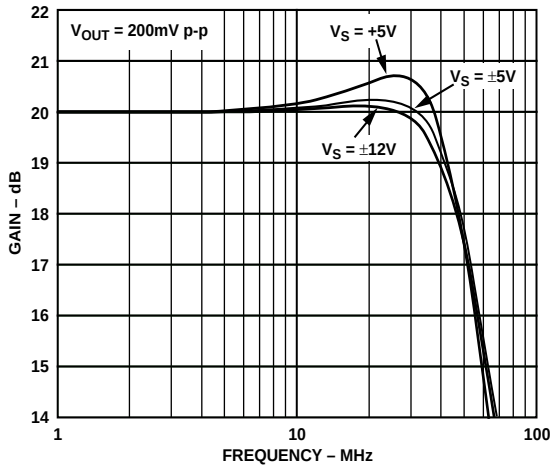

Figure 5. Small Signal Frequency Response for Various Supplies

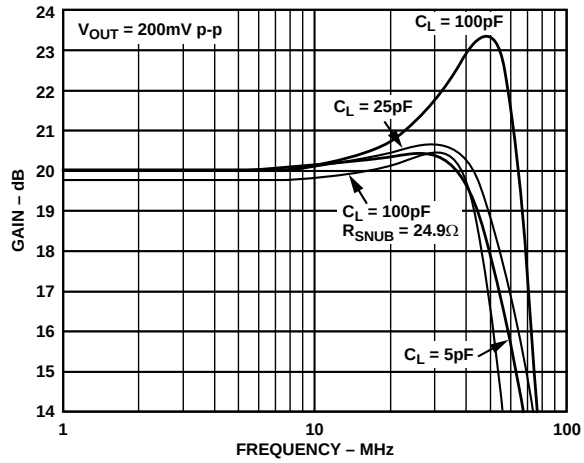

Figure 8. Small Signal Frequency Response for Various C_{LOAD}

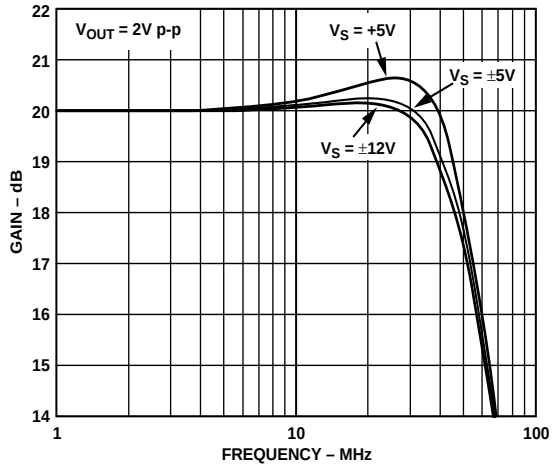

Figure 6. Large Signal Frequency Response for Various Supplies

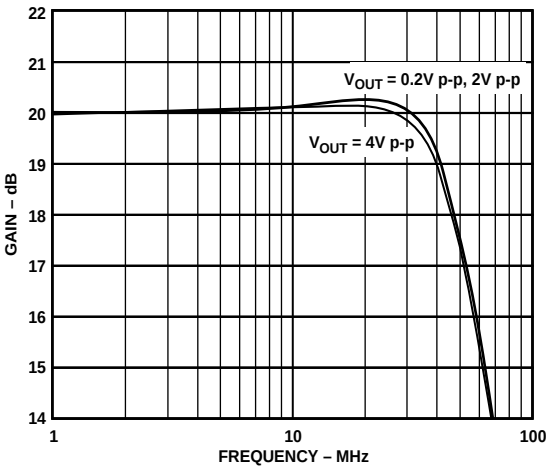

Figure 9. Frequency Response for Various Output Amplitudes

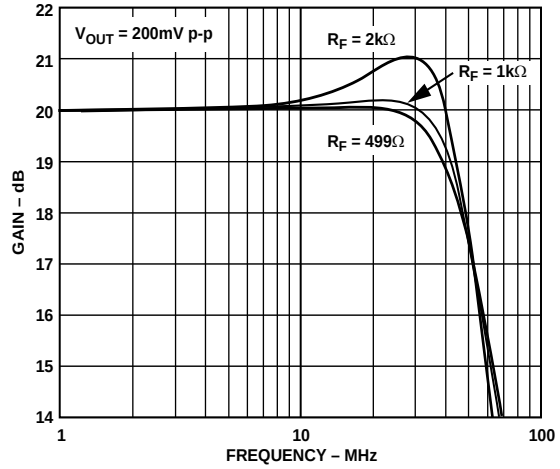

Figure 10. Small Signal Frequency Response for Various R_F

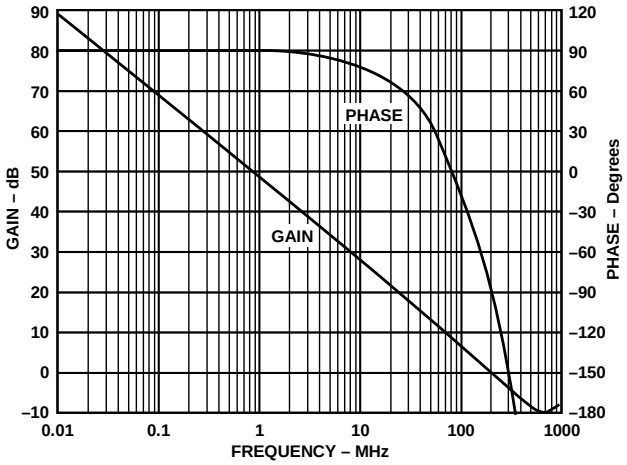

Figure 13. Open-Loop Gain and Phase

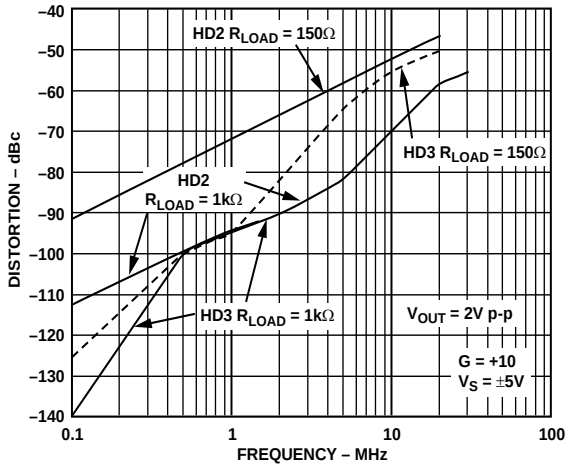

Figure 11. Distortion vs. Frequency for Various Loads

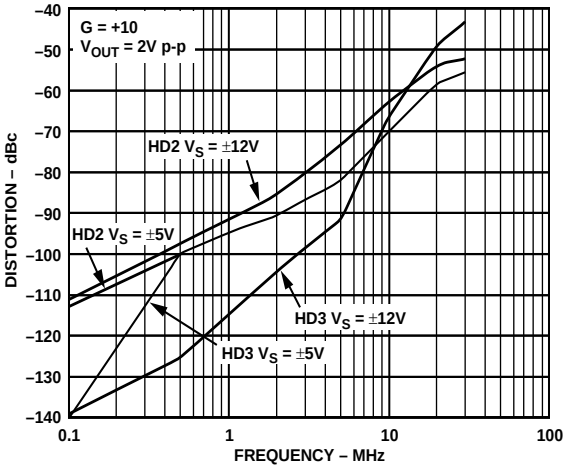

Figure 14. Distortion vs. Frequency for Various Supplies

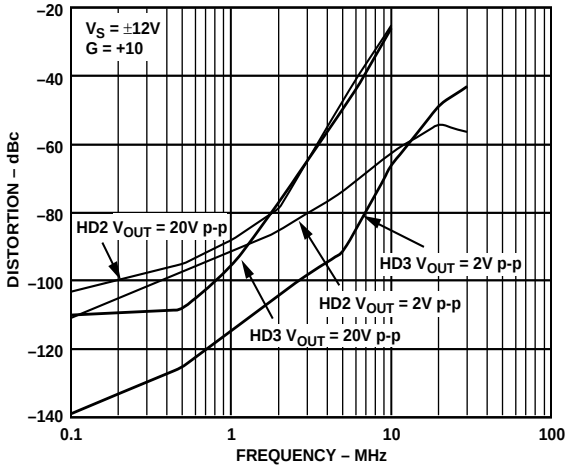

Figure 12. Distortion vs. Frequency for Various Amplitudes

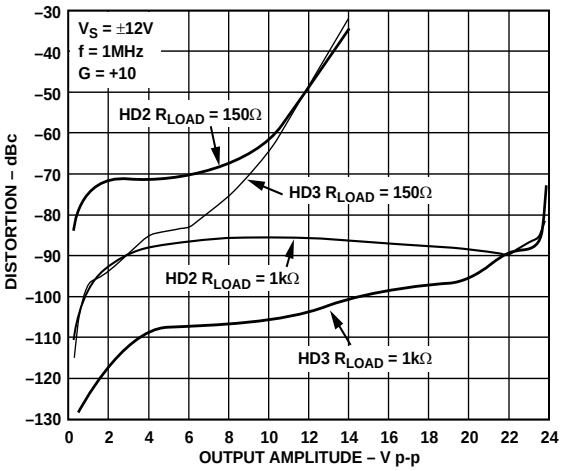

Figure 15. Distortion vs. Output Amplitude for Various Loads

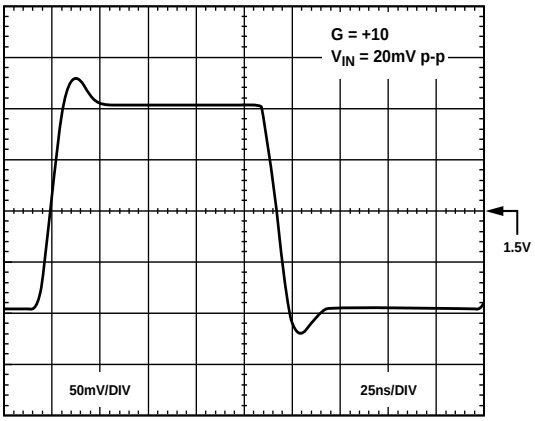

Figure 16. Small Signal Transient Response 5 V Supply

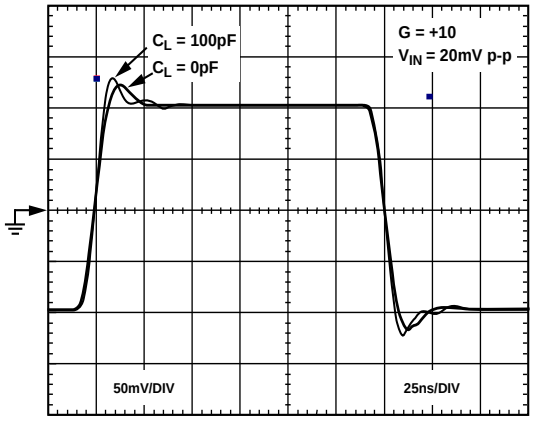

Figure 19. Small Signal Transient Response ± 5 V Supply

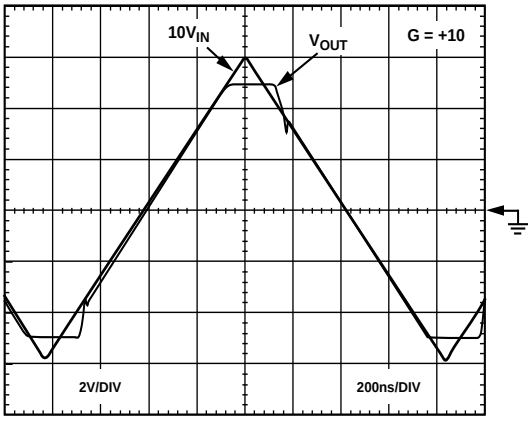

Figure 17. Output Overdrive Recovery

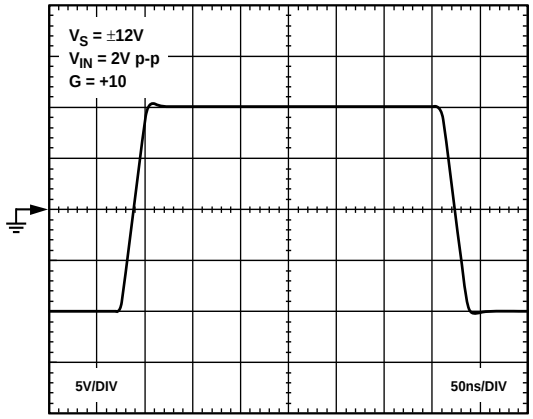

Figure 20. Large Signal Transient Response

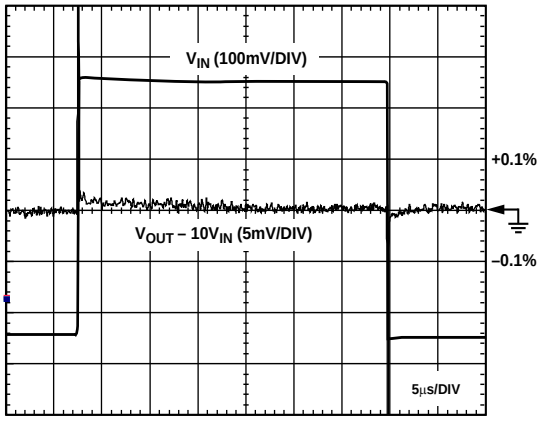

Figure 18. Long-Term Settling Time

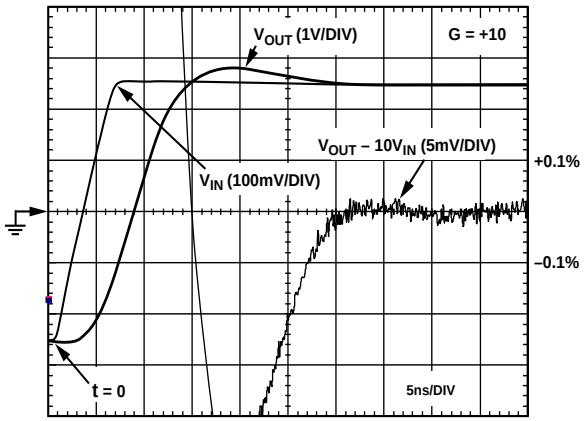

Figure 21. 0.1% Short-Term Settling Time

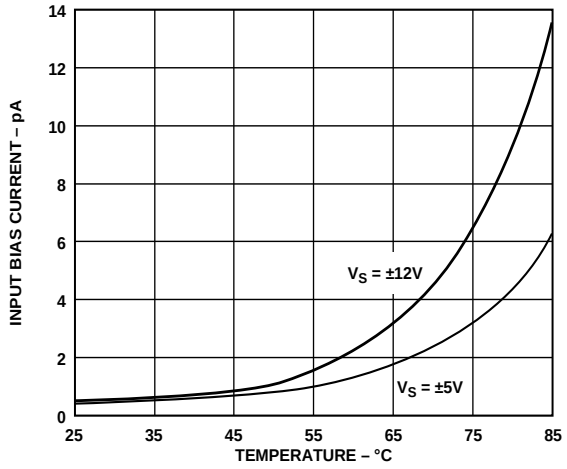

Figure 22. Input Bias Current vs. Temperature

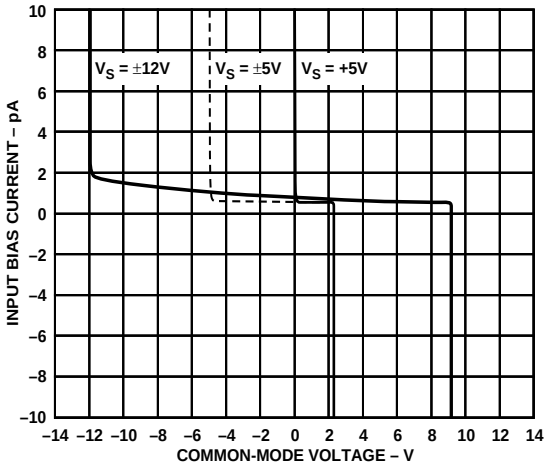

Figure 25. Input Bias Current vs. Common-Mode Voltage

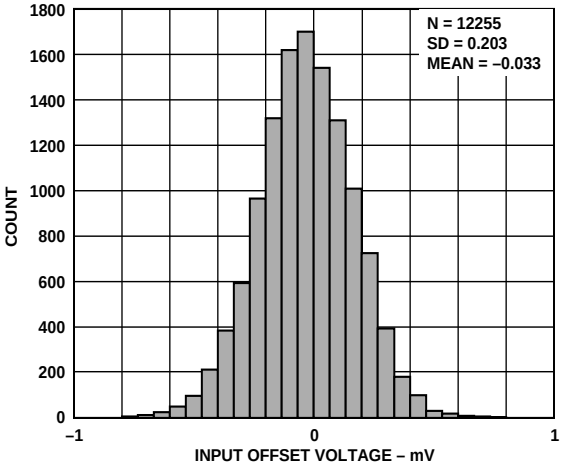

Figure 23. Input Offset Voltage Histogram

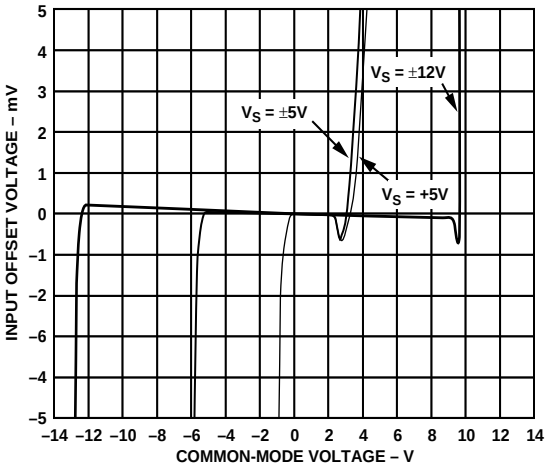

Figure 26. Input Offset Voltage vs. Common-Mode Voltage

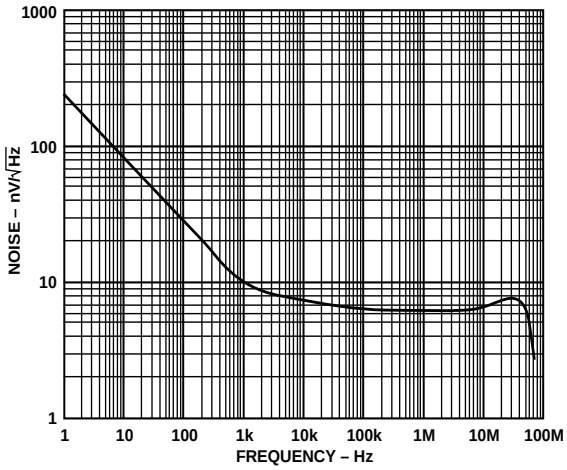

Figure 24. Voltage Noise

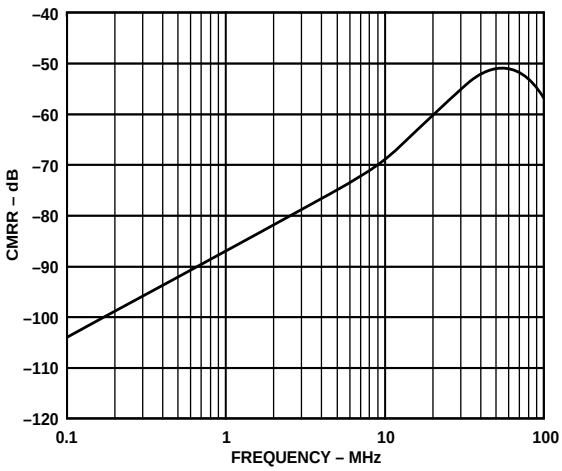

Figure 27. CMRR vs. Frequency

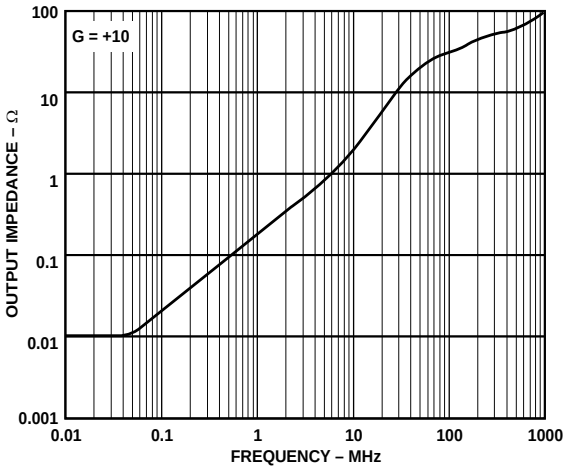

Figure 28. Output Impedance vs. Frequency

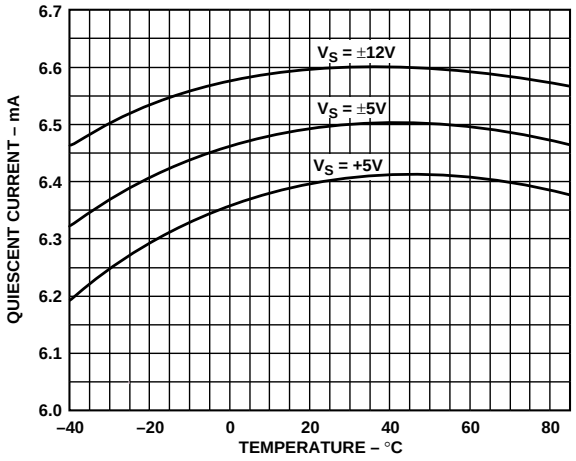

Figure 31. Quiescent Current vs. Temperature for Various Supply Voltages

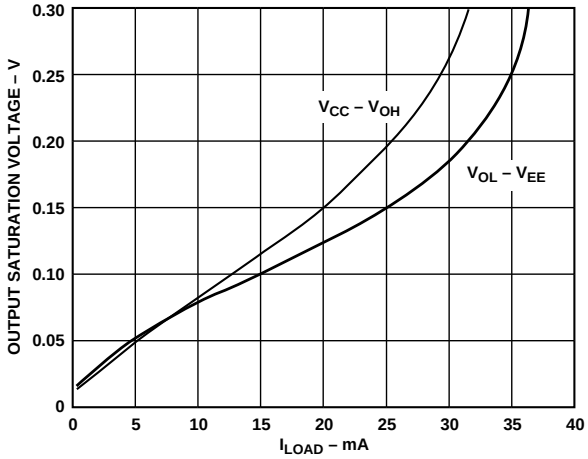

Figure 29. Output Saturation Voltage vs. Output Load Current

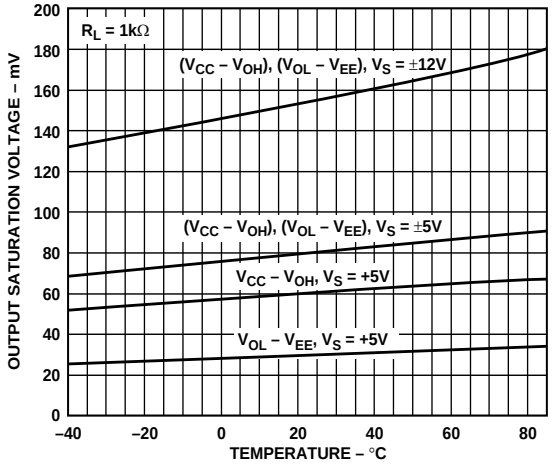

Figure 32. Output Saturation Voltage vs. Temperature

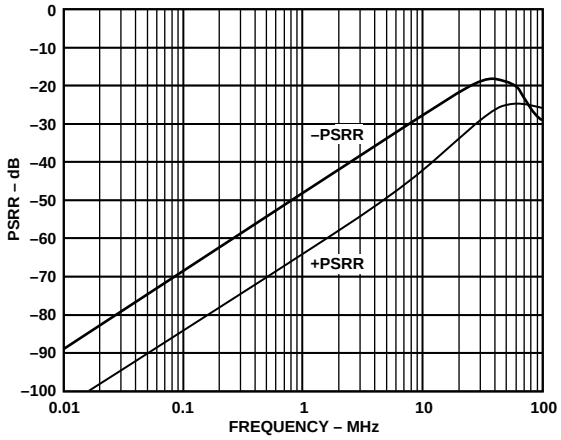

Figure 30. PSRR vs. Frequency

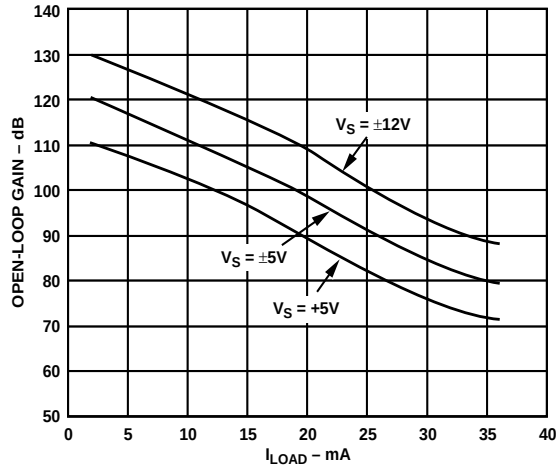

Figure 33. Open-Loop Gain vs. Load Current for Various Supplies

TEST CIRCUITS

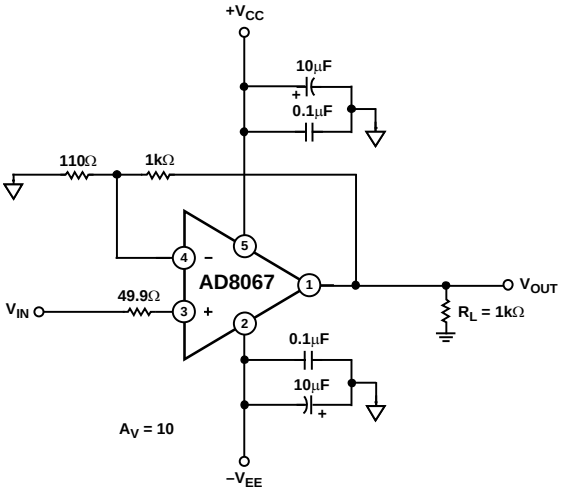

Figure 34. Standard Test Circuit

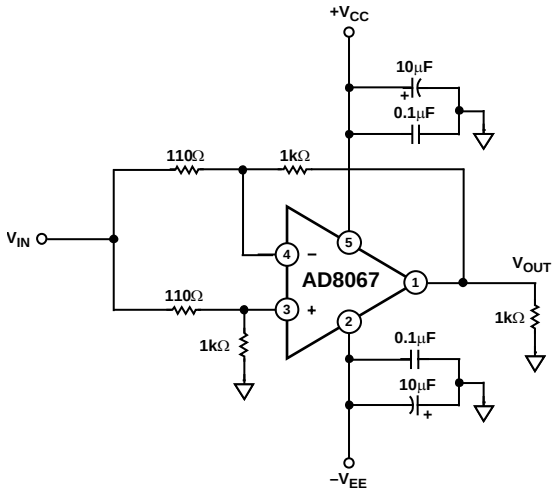

Figure 37. CMRR Test Circuit

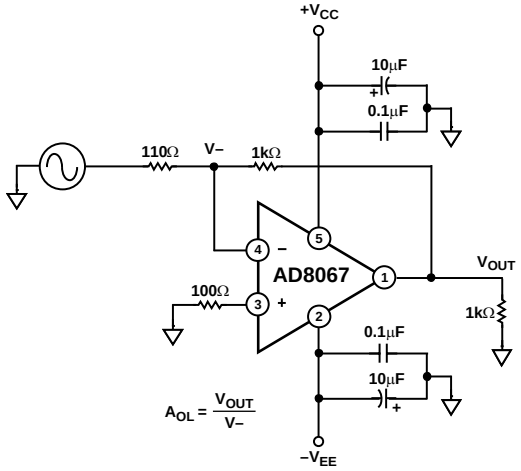

Figure 35. Open-Loop Gain Test Circuit

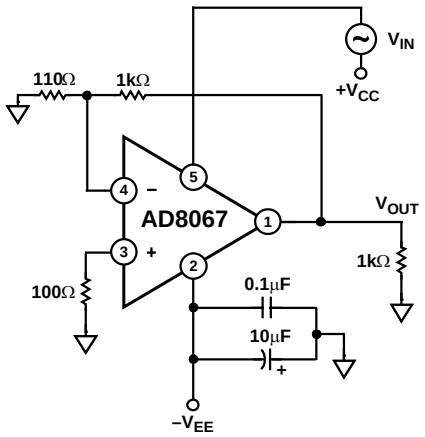

Figure 38. Positive PSRR Test Circuit

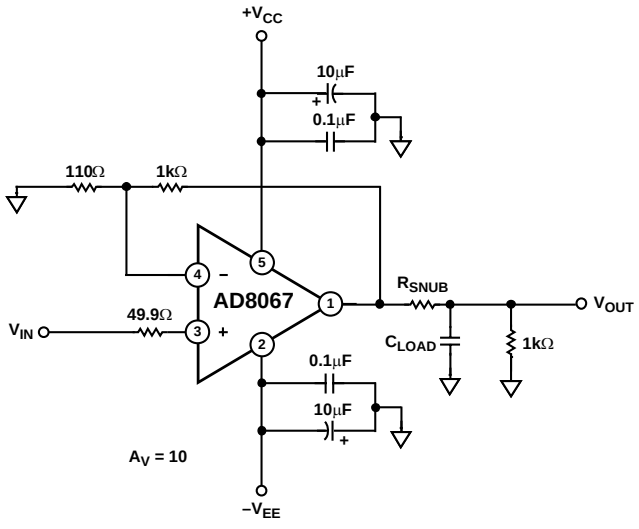

Figure 36. Test Circuit for Capacitive Load

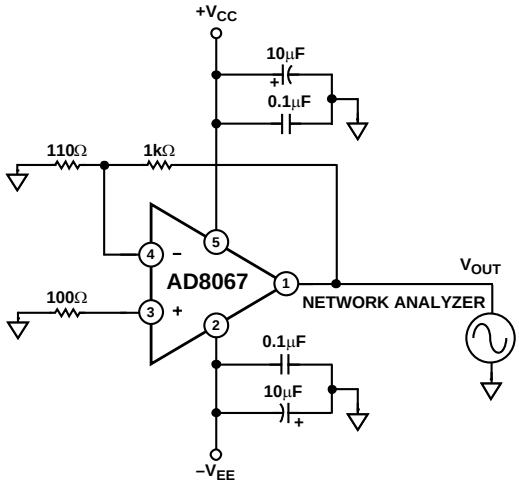

Figure 39. Output Impedance Test Circuit

THEORY OF OPERATION

The AD8067 is a low noise, wideband, voltage feedback operational amplifier that combines a precision JFET input stage with Analog Devices' dielectrically isolated eXtra Fast Complementary Bipolar (XFCB) process BJTs. Operating supply voltages range from 5 V to 24 V. The amplifier features a patented rail-to-rail output stage capable of driving within 0.25 V of either power supply while sourcing or sinking 30 mA. The JFET input, composed of N-channel devices, has a common-mode input range that includes the negative supply rail and extends to 3 V below the positive supply. In addition, the potential for phase reversal behavior was eliminated for all input voltages within the power supplies.

The combination of low noise, dc precision, and high bandwidth makes the AD8067 uniquely suited for wideband, very high input impedance, high gain buffer applications. It is also useful in wideband transimpedance applications, such as a photodiode interface, that require very low input currents and dc precision.

BASIC FREQUENCY RESPONSE

The AD8067's typical open-loop response (see Figure 41) shows a phase margin of 60° at a gain of +10. Typical configurations for noninverting and inverting voltage gain applications are shown in Figure 40 and Figure 42.

The closed-loop frequency response of a basic noninverting gain configuration can be approximated by:

$$Closed\ Loop{-}3\ dB\ Frequency = (GBP) \times \frac{R_G}{(R_F + R_G)}$$

$$DC\ Gain = R_F/R_G + 1$$

GBP is the gain bandwidth product of the amplifier. Typical GBP for the AD8067 is 300 MHz. See Table 5 for the recommended values for R_G and R_F.

$$Noninverting\ Configuration\ Noise\ Gain = \frac{R_F}{R_G} + 1$$

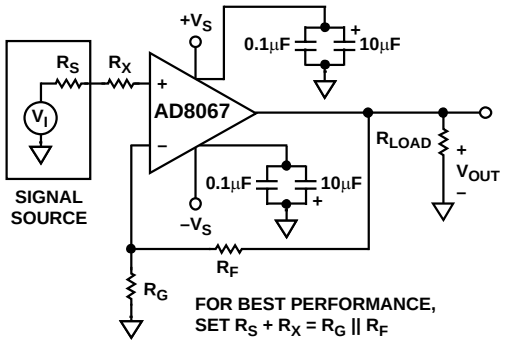

Figure 40. Noninverting Gain Configuration

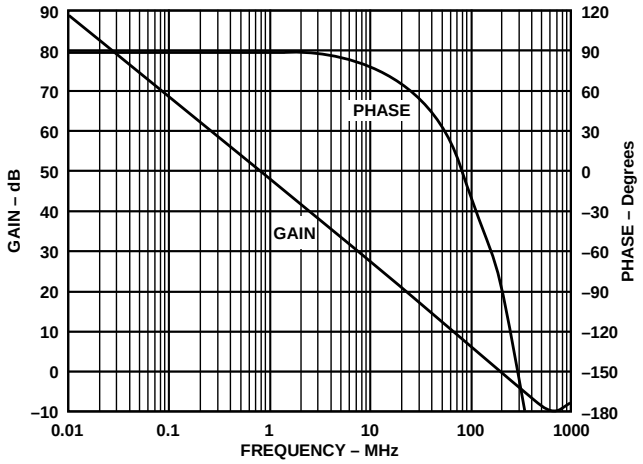

Figure 41. Open-Loop Frequency Response

The bandwidth formula only holds true when the phase margin of the application approaches 90°, which it will in high gain configurations. The bandwidth of the AD8067 used in a G = +10 buffer is 54 MHz, considerably faster than the 30 MHz predicted by the closed loop –3 dB frequency equation. This extended bandwidth is due to the phase margin being at 60° instead of 90°. Gains lower than +10 show an increased amount of peaking, as shown in Figure 4. For gains lower than +7, use the AD8065, a unity gain stable JFET input op amp with a unity gain bandwidth of 145 MHz, or refer to the Applications section for using the AD8067 in a lower gain configuration.

Table 5. Recommended Values of R_G and R_F

Gain	R_G (Ω)	R_F (kΩ)	BW (MHz)
10	110	1	54
20	49.9	1	15
50	20	1	6
100	10	1	3

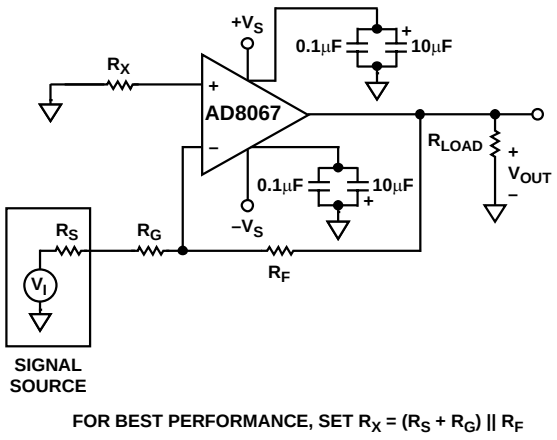

Figure 42. Inverting Gain Configuration

For inverting voltage gain applications, the source impedance of the input signal must be considered because it sets the application's noise gain as well as the apparent closed-loop gain. The basic frequency equation for inverting applications is

$$Closed\text{-}Loop\ -3\ dB\ Frequency = (GBP) \times \frac{R_G + R_S}{R_F + R_G + R_S}$$

$$DC\ Gain = -\frac{R_F}{R_G + R_S}$$

where GBP is the gain bandwidth product of the amplifier, and R_S is the signal source resistance.

$$Inverting\ Configuration\ Noise\ Gain = \frac{R_F + R_G + R_S}{R_G + R_S}$$

It is important that the noise gain for inverting applications be kept above 6 for stability reasons. If the signal source driving the inverter is another amplifier, take care that the driving amplifier shows low output impedance through the frequency span of the expected closed-loop bandwidth of the AD8067.

RESISTOR SELECTION FOR WIDEBAND OPERATION

Voltage feedback amplifiers can use a wide range of resistor values to set their gain. Proper design of the application's feedback network requires consideration of the following issues:

- Poles formed by the amplifier's input capacitances with the resistances seen at the amplifier's input terminals
- Effects of mismatched source impedances
- Resistor value impact on the application's output voltage noise
- Amplifier loading effects

The AD8067 has common-mode input capacitances (C_M) of 1.5 pF and a differential input capacitance (C_D) of 2.5 pF. This is illustrated in Figure 43. The source impedance driving the positive input of a noninverting buffer forms a pole primarily with the amplifier's common-mode input capacitance as well as any parasitic capacitance due to the board layout (C_{PAR}). This limits the obtainable bandwidth. For G = +10 buffers, this bandwidth limit becomes apparent for source impedances >1 kΩ.

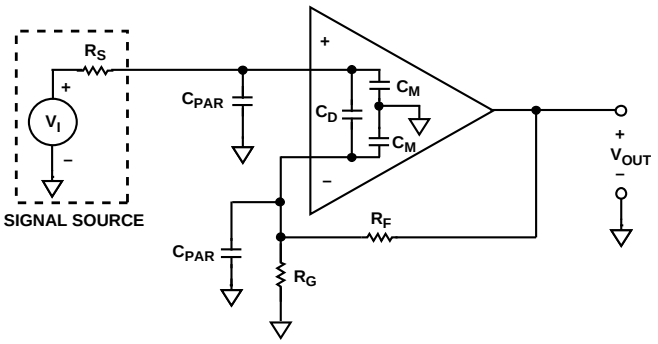

Figure 43. Input and Board Capacitances

There is a pole in the feedback loop response formed by the source impedance seen by the amplifier's negative input ($R_G \,||\, R_F$) and the sum of the amplifier's differential input capacitance, common-mode input capacitance, and any board parasitic capacitance. This decreases the loop phase margin and can cause stability problems, that is, unacceptable peaking and ringing in the response. To avoid this problem, it is recommended that the resistance at the AD8067's negative input be kept below 200 Ω for all wideband voltage gain applications.

Matching the impedances at the inputs of the AD8067 is also recommended for wideband voltage gain applications. This minimizes nonlinear common-mode capacitive effects that can significantly degrade settling time and distortion performance.

The AD8067 has a low input voltage noise of 6.6 nV/√Hz. Source resistances greater than 500 Ω at either input terminal notably increases the apparent referred-to-input (RTI) voltage noise of the application.

The amplifier must supply output current to its feedback network, as well as to the identified load. For instance, the load resistance presented to the amplifier in Figure 40 is $R_{LOAD} \,||\, (R_F + R_G)$. For an R_{LOAD} of 100 Ω, R_F of 1 kΩ, and R_G of 100 Ω, the amplifier is driving a total load resistance of about 92 Ω. This becomes more of an issue as R_F decreases. The AD8067 is rated to provide 30 mA of low distortion output current. Heavy output drive requirements also increase the part's power dissipation and should be taken into account.

DC ERROR CALCULATIONS

Figure 44 illustrates the primary dc errors associated with a voltage feedback amplifier. For both inverting and noninverting configurations:

$$Output\ Voltage\ Error\ due\ to\ V_{OS} = V_{OS}\left(\frac{R_G + R_F}{R_G}\right)$$

$$Output\ Voltage\ Error\ due\ to\ I_B = I_{B+} \times R_S\left(\frac{R_F + R_G}{R_G}\right) - I_{B-} \times R_F$$

Total error is the sum of the two.

DC common-mode and power supply effects can be added by modeling the total V_{OS} with the expression:

$$V_{OS}(tot) = V_{OS}(nom) + \frac{\Delta V_S}{PSR} + \frac{\Delta V_{CM}}{CMR}$$

where:

V_{OS} *(nom)* is the offset voltage specified at nominal conditions (1 mV max).

ΔV_S is the change in power supply voltage from nominal conditions.

PSR is power supply rejection (90 dB minimum).

ΔV_{CM} is the change in common-mode voltage from nominal test conditions.

CMR is the common-mode rejection (85 dB minimum for the AD8067).

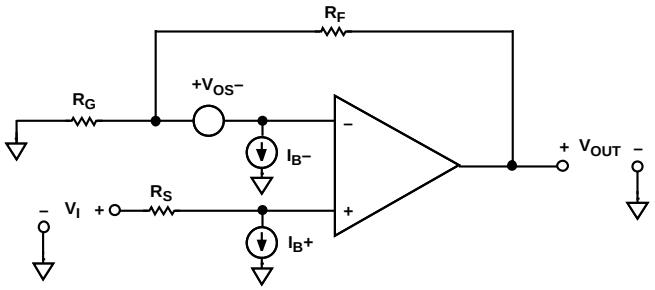

Figure 44. Op Amp DC Error Sources

INPUT AND OUTPUT OVERLOAD BEHAVIOR

A simplified schematic of the AD8067 input stage is shown in Figure 45. This shows the cascoded N-channel JFET input pair, the ESD and other protection diodes, and the auxiliary NPN input stage that eliminates phase inversion behavior.

When the common-mode input voltage to the amplifier is driven to within approximately 3 V of the positive power supply, the input JFET's bias current turns off, and the bias of the NPN pair turns on, taking over control of the amplifier. The NPN differential pair now sets the amplifier's offset, and the input bias current is now in the range of several tens of microamps. This behavior is illustrated in Figure 25 and Figure 26. Normal operation resumes when the common-mode voltage goes below the 3 V from the positive supply threshold.

The output transistors have circuitry included to limit the extent of their saturation when the output is overdriven. This improves output recovery time. A plot of the output recovery time for the AD8067 used as a G = +10 buffer is shown in Figure 17.

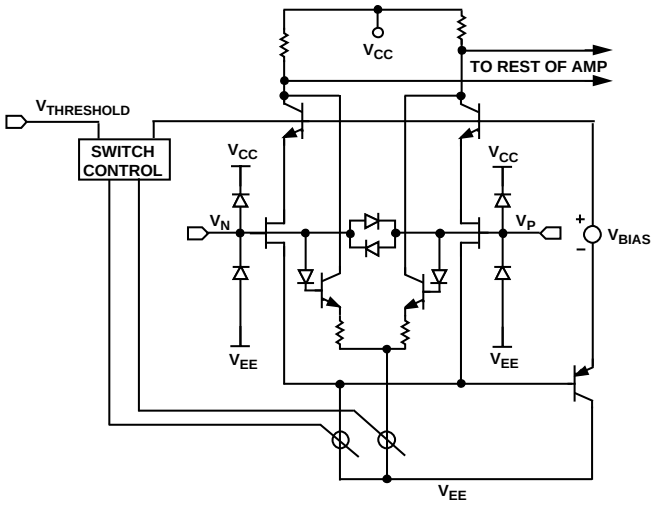

Figure 45. Simplified Input Schematic

INPUT PROTECTION

The inputs of the AD8067 are protected with back-to-back diodes between the input terminals as well as ESD diodes to either power supply. The result is an input stage with picoamp level input currents that can withstand 2 kV ESD events (human body model) with no degradation.

Excessive power dissipation through the protection devices destroys or degrades the performance of the amplifier. Differential voltages greater than 0.7 V result in an input current of approximately $(|V_+ - V_-| - 0.7\ V)/(R_I + R_G)$, where R_I and R_G are the resistors (see Figure 46). For input voltages beyond the positive supply, the input current is about $(V_I - V_{CC} - 0.7\ V)/R_I$. For input voltages beyond the negative supply, the input current is about $(V_I - V_{EE} + 0.7\ V)/R_I$. For any of these conditions, R_I should be sized to limit the resulting input current to 50 mA or less.

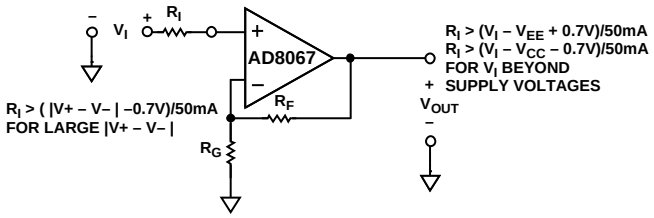

Figure 46. Current Limiting Resistor

CAPACITIVE LOAD DRIVE

Capacitive load introduces a pole in the amplifier loop response due to the finite output impedance of the amplifier. This can cause excessive peaking and ringing in the response. The AD8067 with a gain of +10 handles up to a 30 pF capacitive load without an excessive amount of peaking (see Figure 8). If greater capacitive load drive is required, consider inserting a small resistor in series with the load (24.9 Ω is a good value to start with). Capacitive load drive capability also increases as the gain of the amplifier increases.

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

Layout

In extremely low input bias current amplifier applications, stray leakage current paths must be kept to a minimum. Any voltage differential between the amplifier inputs and nearby traces sets up a leakage path through the PCB. Consider a 1 V signal and 100 GΩ to ground present at the input of the amplifier. The resultant leakage current is 10 pA; this is 10× the input bias current of the amplifier. Poor PCB layout, contamination, and the board material can create large leakage currents. Common contaminants on boards are skin oils, moisture, solder flux, and cleaning agents. Therefore, it is imperative that the board be thoroughly cleaned and the board surface be free of contaminants to fully take advantage of the AD8067's low input bias currents.

To significantly reduce leakage paths, a guard-ring/shield around the inputs should be used. The guard-ring circles the input pins and is driven to the same potential as the input signal, thereby reducing the potential difference between pins. For the guard ring to be completely effective, it must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above, and below, using a multilayer board (see Figure 47). The SOT-23-5 package presents a challenge in keeping the leakage paths to a minimum. The pin spacing is very tight, so extra care must be used when constructing the guard ring (see Figure 48 for recommended guard-ring construction).

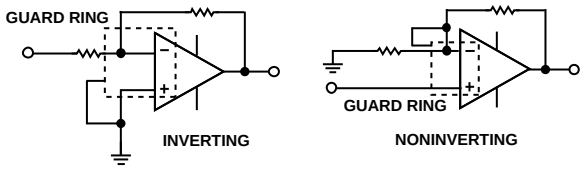

Figure 47. Guard-Ring Configurations

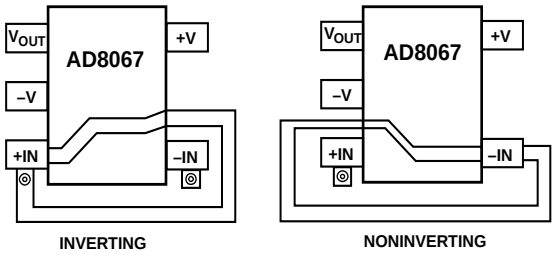

Figure 48. Guard-Ring Layout SOT-23-5

Grounding

To minimize parasitic inductances and ground loops in high speed, densely populated boards, a ground plane layer is critical. Understanding where the current flows in a circuit is critical in the implementation of high speed circuit design. The length of the current path is directly proportional to the magnitude of the parasitic inductances and thus the high frequency impedance of the path. Fast current changes in an inductive ground return creates unwanted noise and ringing.

The length of the high frequency bypass capacitor leads is critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Because load currents flow from supplies as well as ground, the load should be placed at the same physical location as the bypass capacitor ground. For large values of capacitors, which are intended to be effective at lower frequencies, the current return path length is less critical.

Power Supply Bypassing

Power supply pins are actually inputs and care must be taken to provide a clean, low noise dc voltage source to these inputs. The bypass capacitors have two functions:

- Provide a low impedance path for unwanted frequencies from the supply inputs to ground, thereby reducing the effect of noise on the supply lines
- Provide localized charge storage—this is usually accomplished with larger electrolytic capacitors

Decoupling methods are designed to minimize the bypassing impedance at all frequencies. This can be accomplished with a combination of capacitors in parallel to ground. Good quality ceramic chip capacitors (X7R or NPO) should be used and always kept as close to the amplifier package as possible. A parallel combination of a 0.1 μF ceramic and a 10 μF electrolytic, covers a wide range of rejection for unwanted noise. The 10 μF capacitor is less critical for high frequency bypassing, and in most cases, one per supply line is sufficient.

APPLICATIONS

WIDEBAND PHOTODIODE PREAMP

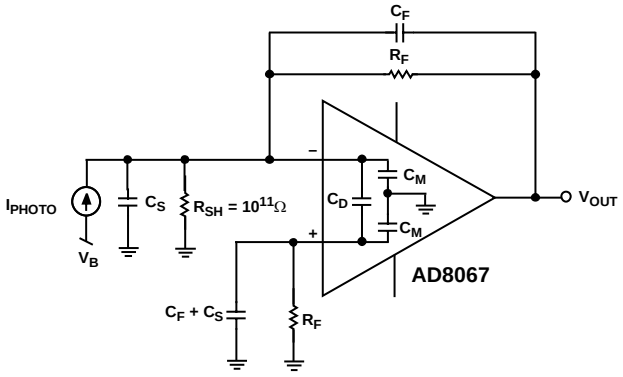

Figure 49. Wideband Photodiode Preamp

Figure 49 shows an I/V converter with an electrical model of a photodiode.

The basic transfer function is

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F}$$

where I_{PHOTO} is the output current of the photodiode, and the parallel combination of R_F and C_F sets the signal bandwidth.

The stable bandwidth attainable with this preamp is a function of R_F, the gain bandwidth product of the amplifier, and the total capacitance at the amplifier's summing junction, including C_S and the amplifier input capacitance. R_F and the total capacitance produce a pole in the amplifier's loop transmission that can result in peaking and instability. Adding C_F creates a zero in the loop transmission that compensates for the pole's effect and reduces the signal bandwidth. It can be shown that the signal bandwidth resulting in a 45° phase margin ($f_{(45)}$) is defined by

$$f_{(45)} = \sqrt{\frac{GBP}{2\pi \times R_F \times C_S}}$$

GBP is the unit gain bandwidth product, R_F is the feedback resistance, and C_S is the total capacitance at the amplifier summing junction (amplifier + photodiode + board parasitics).

The value of C_F that produces $f_{(45)}$ can be shown to be

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times GBP}}$$

The frequency response in this case shows about 2 dB of peaking and 15% overshoot. Doubling C_F and cutting the bandwidth in half results in a flat frequency response, with about 5% transient overshoot.

The preamp's output noise over frequency is shown in Figure 50.

Table 6. RMS Noise Contributions of Photodiode Preamp

Contributor	Expression	RMS Noise (μV)[1]
$R_F \times 2$	$\sqrt{2 \times 4kT \times R_F \times f2 \times 1.57}$	152
Amp to f1	$V_{NOISE} \times \sqrt{f1}$	4.3
Amp (f2 – f1)	$V_{NOISE} \times \sqrt{\frac{(C_S + C_M + C_F + 2C_D)}{C_F}} \times \sqrt{f2 - f1}$	96
Amp (Past f2)	$V_{NOISE} \times \frac{(C_S + C_M + C_F + 2C_D)}{C_F} \times \sqrt{f3 \times 1.57}$	684
	RSS Total	708

[1] RMS noise with R_F = 50 kΩ, C_S = 0.67 pF, C_F = 0.33 pF, C_M = 1.5 pF, and C_D = 2.5 pF.

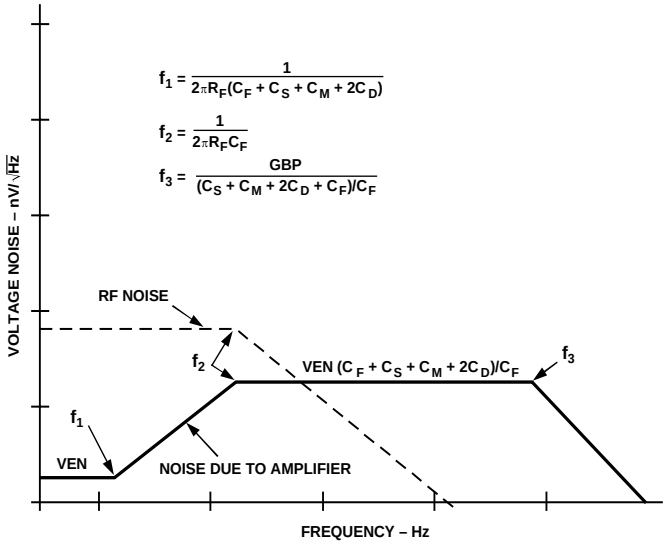

Figure 50. Photodiode Voltage Noise Contributions

Figure 51 shows the AD8067 configured as a transimpedance photodiode amplifier. The amplifier is used in conjunction with a JDS uniphase photodiode detector. This amplifier has a bandwidth of 9.6 MHz, as shown in Figure 52, and is verified by the design equations shown in Figure 50.

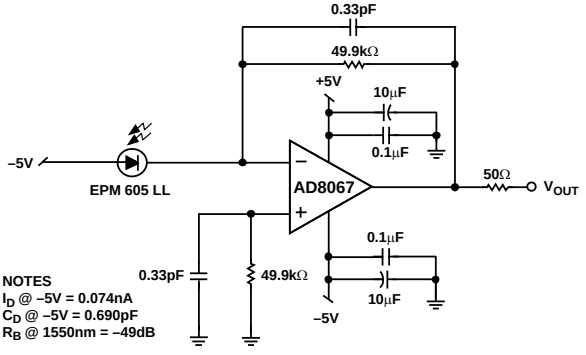

Figure 51. Photodiode Preamplifier

Test data for the preamp is shown in Figure 52 and Figure 53.

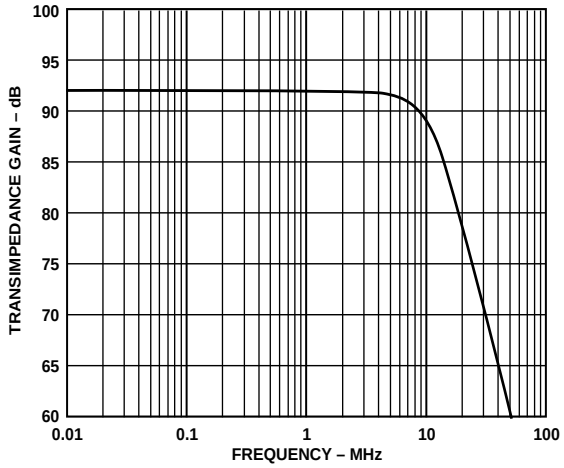

Figure 52. Photodiode Preamplifier Frequency Response

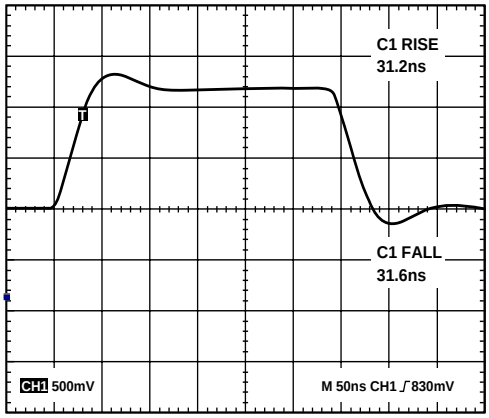

Figure 53. Photodiode Preamplifier Pulse Response

USING THE AD8067 AT GAINS OF LESS THAN 8

A common technique used to stabilize de-compensated amplifiers is to increase the noise gain, independent of the signal gain. The AD8067 can be used in applications where the signal gain is less than 8, if proper care is taken to ensure that the noise gain of the amplifier is set to at least the recommended minimum signal gain of 8 (see Figure 54).

The signal and noise gain equations for a noninverting amplifier are:

$$Signal\ Gain = 1 + \frac{R3}{R1}$$

$$Noise\ Gain = 1 + \frac{R3}{R1}$$

The addition of resistor *R*2 modifies the noise gain equation. Note the signal gain equation has not changed.

$$Noise\ Gain = 1 + \frac{R3}{R1 \,||\, R2}$$

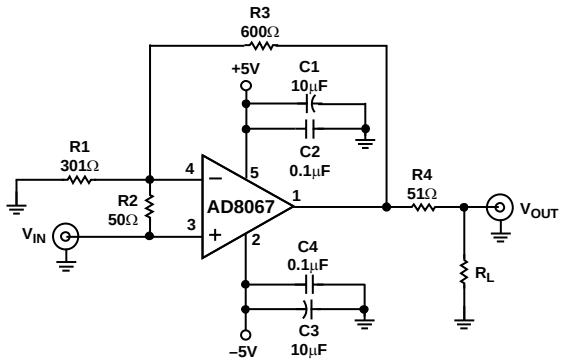

Figure 54. Gain = 3 Schematics

This technique allows the designer to use the AD8067 in gain configurations of less than 8. The drawback to this type of compensation is that the input noise and offset voltages are also amplified by the value of the noise gain. In addition, the distortion performance is degraded. To avoid excessive overshoot and ringing when driving a capacitive load, the AD8067 should be buffered by a small series resistor; in this case, a 51 Ω resistor was used.

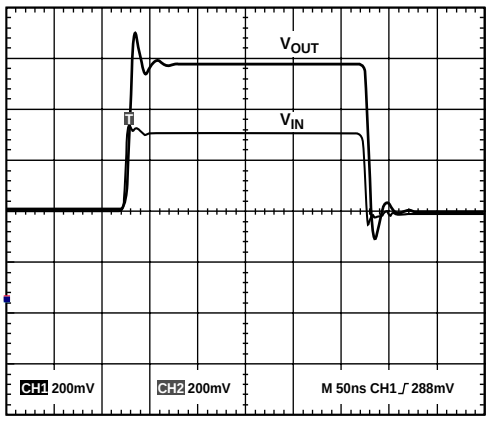

Figure 55. Gain of 3 Pulse Response

SINGLE-SUPPLY OPERATION

The AD8067 is well suited for low voltage single-supply applications, given its N-channel JFET input stage and rail-to-rail output stage. It is fully specified for 5 V supplies. Successful single-supply applications require attention to keep signal voltages within the input and output headroom limits of the amplifier. The input stage headroom extends to 1.7 V (minimum) on a 5 V supply. The center of the input range is 0.85 V. The output saturation limit defines the hard limit of the output headroom. This limit depends on the amount of current the amplifier is sourcing or sinking, as shown in Figure 29.

Traditionally, an offset voltage is introduced in the input network replacing ground as a reference. This allows the output to swing about a dc reference point, typically midsupply. Attention to the required headroom of the amplifier is important, in this case, the required headroom from the positive supply is 3 V; therefore, 1.5 V was selected as a reference, which allows for a 100 mV signal at the input. Figure 56 shows the AD8067 configured for 5 V supply operation with a reference voltage of 1.5 V. Capacitors C1 and C5 ac couple the signal into and out of the amplifier and partially determine the bandwidth of the input and output structures.

$$V_{INPUT}-3\ dB\ Bandwidth = \frac{1}{2\pi R1C1}$$

$$V_{OUTPUT}-3\ dB\ Bandwidth = \frac{1}{2\pi R_L C5}$$

Resistors R2 and R3 set a 1.5 V output bias point for the output signal to swing about. It is critical to have adequate bypassing to provide a good ac ground for the reference voltage. Generally, the bandwidth of the reference network (R2, R3, and C2) is selected to be one tenth that of the input bandwidth. This ensures that any frequencies below the input bandwidth do not pass through the reference network into the amplifier.

Reference network:

$$V_{+REF}-3\ dB\ Bandwidth = \frac{1}{2\pi(R2\,||\,R3)C2}$$

Resistors R4 and R1 set the gain, in this case, an inverting gain of 10 was selected. In this application, the input and output bandwidths were set for approximately 10 Hz. The reference network was set for a tenth of the input and output bandwidth, at approximately 1 Hz.

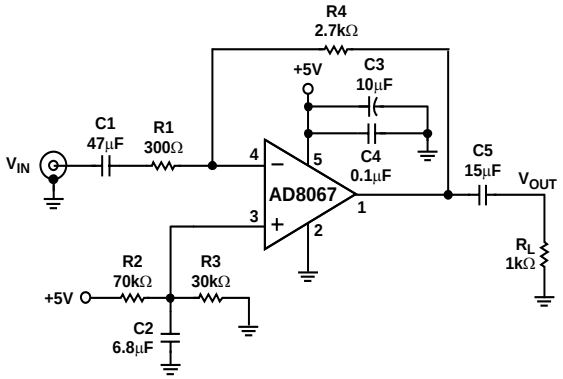

Figure 56. Single-Supply Operation Schematic

HIGH GAIN, HIGH BANDWIDTH COMPOSITE AMPLIFIER

The composite amplifier takes advantage of combining key parameters that can otherwise be mutually exclusive of a conventional single amplifier. For example, most precision amplifiers have good dc characteristics but lack high speed ac characteristics. Composite amplifiers combine the best of both amplifiers to achieve superior performance over their single op amp counterparts. The AD8067 and the AD8009 are well suited for a composite amplifier circuit, combining dc precision with high gain and bandwidth. The circuit runs off a ±5 V power supply at approximately 20 mA of bias current. With a gain of approximately 40 dB, the composite amplifier offers <1 pA input current, a gain bandwidth product of 6.1 GHz, and a slew rate of 630 V/µs.

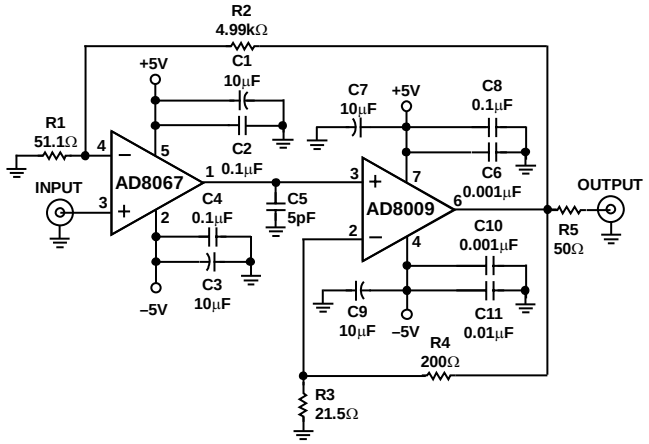

Figure 57. AD8067/AD8009 Composite Amplifier A_V = 100, GBWP = 6.1 GHz

The composite amplifier is set for a gain of 100. The overall gain is set by

$$\frac{V_O}{V_I} = \frac{R2}{R1} + 1$$

The output stage is set for a gain of 10; therefore, the AD8067 has an effective gain of 10, thereby allowing it to maintain a bandwidth in excess of 55 MHz.

The circuit can be tailored for different gain values; keeping the ratios roughly the same ensures that the bandwidth integrity is maintained. Depending on the board layout, Capacitor C5 can be required to reduce ringing on the output. The gain bandwidth and pulse responses are shown in Figure 58, Figure 59, and Figure 60.

Layout of this circuit requires attention to the routing and length of the feedback path. It should be kept as short as possible to minimize stray capacitance.

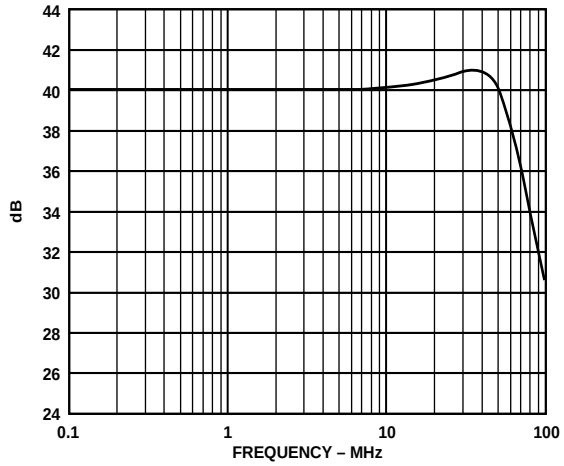

Figure 58. Gain Bandwidth Response

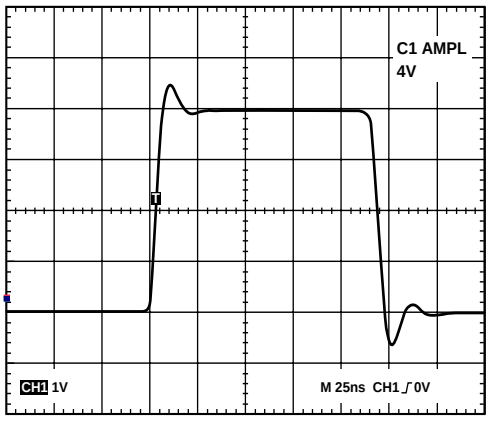

Figure 59. Large Signal Response

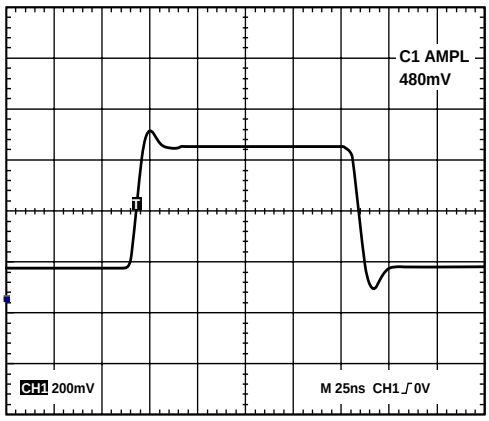

Figure 60. Small Signal Response

OUTLINE DIMENSIONS

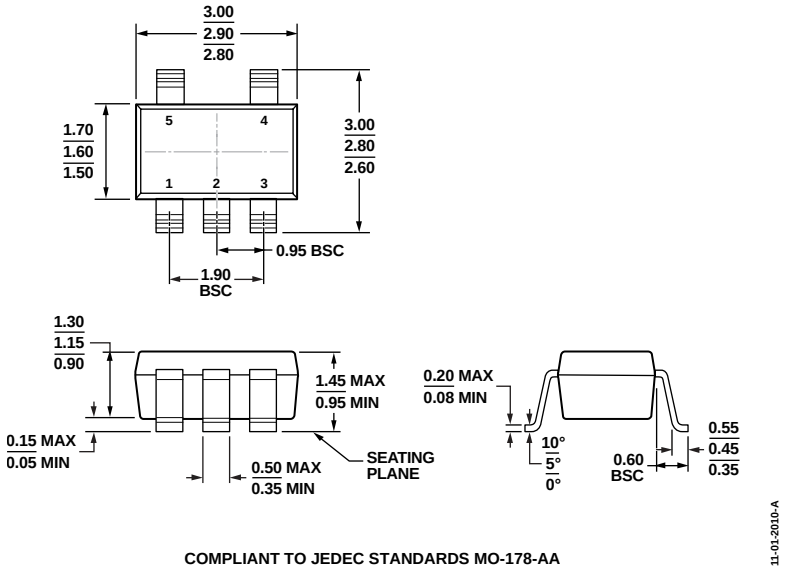

Figure 61. 5-Lead Small Outline Transistor Package [SOT-23}
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding[2]
AD8067ART-REEL	–40°C to +85°C	5-Lead SOT-23	RT-5	HAB
AD8067ART-R2	–40°C to +85°C	5-Lead SOT-23	RT-5	HAB
AD8067ARTZ-REEL	–40°C to +85°C	5-Lead SOT-23	RT-5	HAB#
AD8067ARTZ-REEL7	–40°C to +85°C	5-Lead SOT-23	RT-5	HAB#
AD8067ARTZ-R2	–40°C to +85°C	5-Lead SOT-23	RT-5	HAB#
AD8067ART-EBZ	–40°C to +85°C	Evaluation Board for 5-Lead SOT-23		

[1] Z = RoHS Compliant Part.
[2] # denotes lead-free product may be top or bottom marked.

NOTES

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D03205–0–4/12(B)