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Devices Connected/Referenced

AD9910	1 GSPS Direct Digital Synthesizer (DDS)
AD9520	Clock Generator and Distribution IC
ADCLK846	High Speed LVDS Clock Fanout Buffer

Synchronizing Multiple AD9910 1 GSPS Direct Digital Synthesizers

CIRCUIT FUNCTION AND BENEFITS

Synchronization of multiple DDS devices allows precise digital tuning control of the phase and amplitude across multiple frequency carriers. This type of control is useful in radar applications and quadrature (I/Q) upconversion for side-band suppression.

The circuit in Figure 1 demonstrates how to synchronize four AD9910 1 GSPS, DDS chips using the AD9520 clock generator and the ADCLK846 clock fanout buffer. The result is precise phase alignment between the clock and output signals of four AD9910 devices.
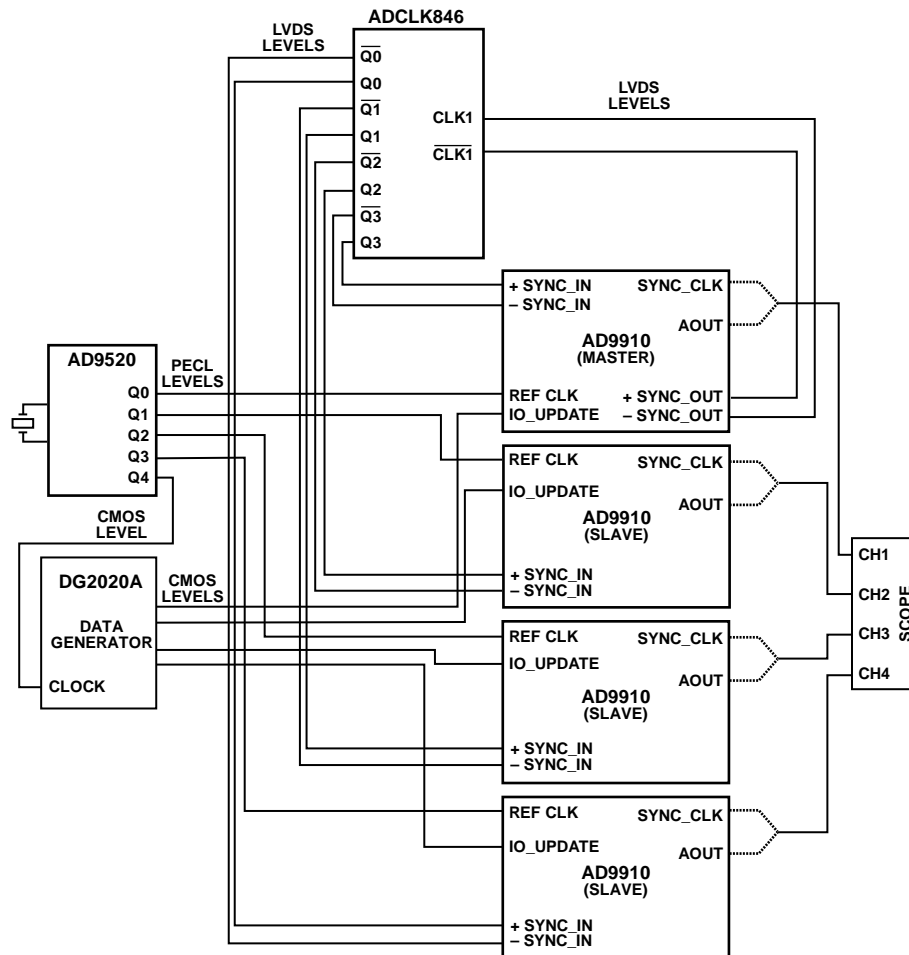

Figure 1. Setup for Synchronization of Multiple AD9910's (Simplified Schematic: Decoupling, Power, and All Connections Not Shown)

Rev. A

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CIRCUIT DESCRIPTION

The circuit in Figure 1 was constructed by connecting the respective evaluation boards for the individual products. Connections were made with matched cable lengths. The first of three basic requirements to synchronize multiple AD9910's is to provide a co-incident reference clock (REF CLK).

The setup uses the AD9520 as the REF CLK source for each AD9910 DDS. The AD9520 runs off an external crystal and the internal PLL. The AD9520 distributes phase aligned 1 GHz REF CLKs (PECL outputs) to all four AD9910 evaluation boards. It also provides a CMOS output clock to the Tektronix DG2020A data pattern generator for the IO_UPDATE.

The next step for synchronization is to align the rising edge of SYNC_CLK for all four AD9910's. The SYNC_CLK provides the reference for a co-incident IO_UPDATE. SYNC_CLK alignment is accomplished using the internal synchronization capability of the AD9910. The ADCLK846 distributes phase aligned SYNC_INs to all four AD9910s. See the AD9910 data sheet for more details on synchronization capability.

Figure 2 shows all four SYNC_CLKs with the AD9910 internal synchronization circuit disabled. Note that the SYNC_CLKs are not inherently aligned even when the REF CLKs are phase aligned.

To phase align the SYNC_CLK rising edges, one AD9910 is programmed as the master device and the others as slave devices. The SYNC_OUT of the master device is an LVDS signal buffered and distributed by the ADCLK846 to all AD9910 evaluation boards. The SYNC_IN signal (LVDS) must meet internal setup and hold time requirements of each device's system clock. To help support this timing requirement, the AD9910 features the ability to delay the SYNC_OUT of the master. For further flexibility, the internal SYNC_IN path of each device can be independently delayed.
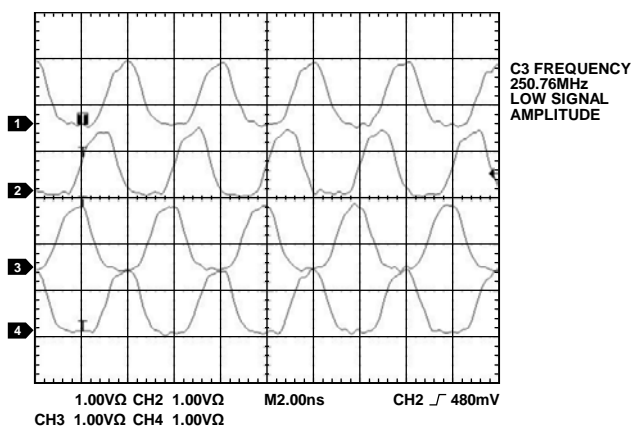
In the setup of Figure 1, connections between boards were made using matched cables, making it possible to use the internal default delay values to phase align the SYNC_CLKs. Figure 3 shows SYNC_CLK phase alignment via the using the synchronization procedure described.

The last requirement to synchronize multiple DDS devices is a co-incident IO_UPDATE. The IO_UPDATE must meet setup and hold times to SYNC_CLK. The IO_UPDATE shown in Figure 1 is sent synchronously to the SYNC_CLK. The last requirement now enables the DDS outputs to be controlled.

Figures 4 and 5 show the DDS outputs in phase alignment. Having the devices synchronized to one another now enables predictable phase and/or amplitude adjustment between DDSs.

Note, in Figure 5 the system clock was reduced to 100 MHz operation, and the outputs were unfiltered to display each DDS raw output. Figure 5 also shows the value of synchronization with each device outputting the same signal.
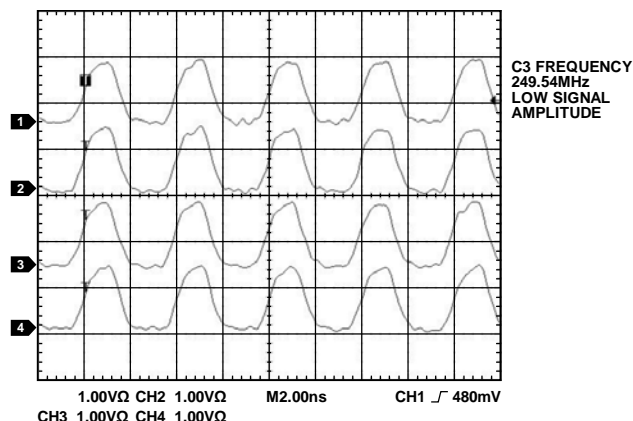
C3 FREQUENCY
249.54MHz
LOW SIGNAL
AMPLITUDE

1.00VΩ CH2 1.00VΩ   M2.00ns   CH1 ⌐ 480mV
CH3 1.00VΩ CH4 1.00VΩ

Figure 3. SYNC_CLK Are Aligned.

C3 FREQUENCY
250.76MHz
LOW SIGNAL
AMPLITUDE

1.00VΩ CH2 1.00VΩ   M2.00ns   CH2 ⌐ 480mV
CH3 1.00VΩ CH4 1.00VΩ

Figure 2. SYNC_CLKs Are Not Aligned.

C3 FREQUENCY
125.321MHz

CH1 200mVΩ ᴮᵂ   200mVΩ ᴮᵂ M5.00ns CH2 ⌐ −80V
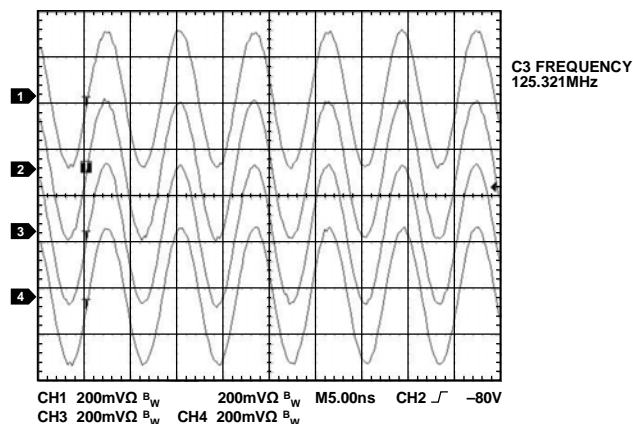CH3 200mVΩ ᴮᵂ CH4 200mVΩ ᴮᵂ

Figure 4. Filtered DDS Outputs Phase Aligned Using the Setup in Figure 1.
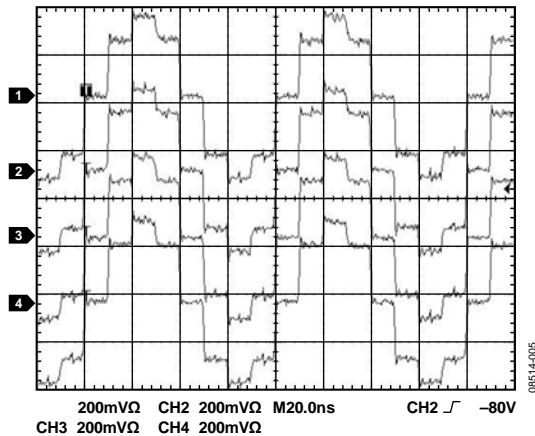
Figure 5. DDS Unfiltered Outputs Phase Aligned Using the Setup in Figure 1.

200mVΩ	**CH2**	**200mVΩ**	**M20.0ns**	**CH2 ⌐ −80V**
CH3 200mVΩ	**CH4**	**200mVΩ**		

COMMON VARIATIONS

Analog Devices offers a variety of direct digital synthesizers, clock distribution chips, and clock buffers to build a DDS-based clock generator. Refer to www.analog.com/dds and www.analog.com/clock for more information.

LEARN MORE

AN-823 Application Note, *Direct Digital Synthesizers in Clocking Applications.* Analog Devices.

AN-837 Application Note, *DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance.* Analog Devices.

Kester, Walt. 2005. *The Data Conversion Handbook.* Analog Devices. Chapters 6 and 7.

Kester, Walt. 2006. *High Speed System Applications.* Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces."

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MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND.* Analog Devices.

MT-085 Tutorial, *Fundamentals of Direct Digital Synthesis (DDS),* Analog Devices.

MT-086 Tutorial, *Fundamentals of Phase Locked Loops (PLL),* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Data Sheets and Evaluation Boards

AD9910 Data Sheet.

AD9910 Evaluation Board.

AD9520 Data Sheet.

AD9520 Evaluation Board.

ADCLK846 Data Sheet.

ADCLK846 Evaluation Board.

REVISION HISTORY

12/09—Rev. 0 to Rev. A

10/09—Revision 0: Initial Version

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