



FEATURES

- Very low power, high performance, low IF transceiver
- Fully integrated io-homecontrol compliant protocol covering
 - Layer 1, Layer 2, and time critical elements of Layer 3
 - Media access
 - Master, slave, and beacon modes supported
 - Automatic io-homecontrol channel scan
 - Automatic CRC, preamble, start byte insertion/check
 - UART data encoding as per io-homecontrol
 - Smart preamble detect/packet sniffing
 - Automatic address filtering
 - Low power modes
- Autonomous packet handling without intervention of host microprocessor thus significantly increasing battery life
- 1-way and 2-way communication supported
- Automatic wake-up timer
- 32-bit hardware timer, 16-bit firmware timer (48 bits total)
- Uses either
 - External 32 kHz crystal
 - Internal 32 kHz RC oscillator
- Patented fast settling automatic frequency control (AFC)
- Fully integrated image rejection calibration (patent pending)
- Digital RSSI
- Operating frequencies
 - Channel 1: 868.25 MHz
 - Channel 2: 868.95 MHz
 - Channel 3: 869.85 MHz

Very low power consumption

- 12.8 mA in receive mode with AGC active
- 11.9 mA in receive mode with manual AGC, ADC off
- 24.1 mA in transmit mode (10 dBm output)
- 0.75 μ A in RCO wake mode
- 1.25 μ A in XTO wake mode (32 kHz oscillator active)
- 38.4 μ A average current in low power mode

Receiver sensitivity (10⁻³ BER)

- 108.5 dBm at 38.4 kbps FSK, 20 kHz deviation

Output power programmable up to 13.5 dBm

- Automatic PA ramping
- Dual PAs offer Tx antenna diversity

Very few external components

- Integrated PLL loop filter
- Integrated Rx/Tx switch
- Integrated battery monitor
- On-chip 8-bit ADC and temperature sensor

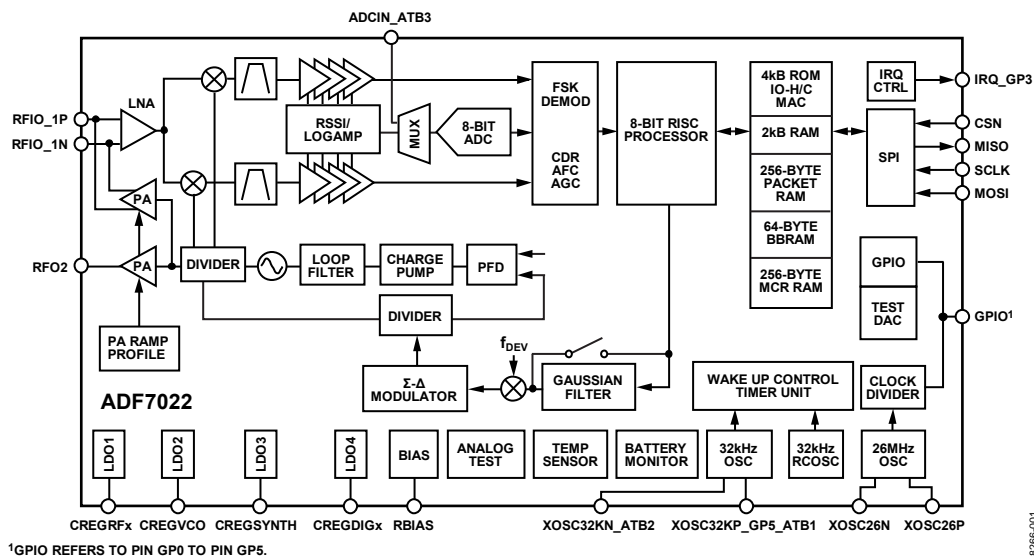
Efficient and flexible SPI control interface

- 4 lines available for low cost microcontroller interface
- Flexible Tx and Rx data buffers
- Efficient burst mode register access
- 1.8 V to 3.6 V power supply
- 5 mm \times 5 mm, 32-lead LFCSP package

APPLICATIONS

- Home automation
- Process and building control

FUNCTIONAL BLOCK DIAGRAM



¹GPIO REFERS TO PIN GP0 TO PIN GP5.

Figure 1.

062846-001

For more information on the ADF7022, contact a local sales office at Analog Devices, Inc.

Rev. SpA

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

ADF7022

NOTES