Tri-Axis Inertial Sensor

Preliminary Technical Data

ADIS16365

FEATURES

Tri-axis gyroscope with digital range scaling
±75°/sec, ±150°/sec, ±300°/sec settings
14-bit resolution
Tri-axis accelerometer
±17 *g* measurement range
14-bit resolution
350 Hz bandwidth
Factory calibrated sensitivity, bias, and alignment
Calibration temperature range: −40°C to +85°C
External clock input for sample synchronization
Digitally controlled bias calibration
Digitally controlled sample rate
Digitally controlled filtering
Programmable condition monitoring
Auxiliary digital input/output
Digitally activated self-test
Programmable power management
Embedded temperature sensor
SPI-compatible serial interface
Auxiliary 12-bit ADC input and DAC output
Single-supply operation: 4.75 V to 5.25 V
2000 *g* shock survivability
Operating temperature range: −40°C to +105°C

APPLICATIONS

Guidance and control
Platform control and stabilization
Motion control and analysis
Inertial measurement units
General navigation
Image stabilization
Robotics

FUNCTIONAL BLOCK DIAGRAM

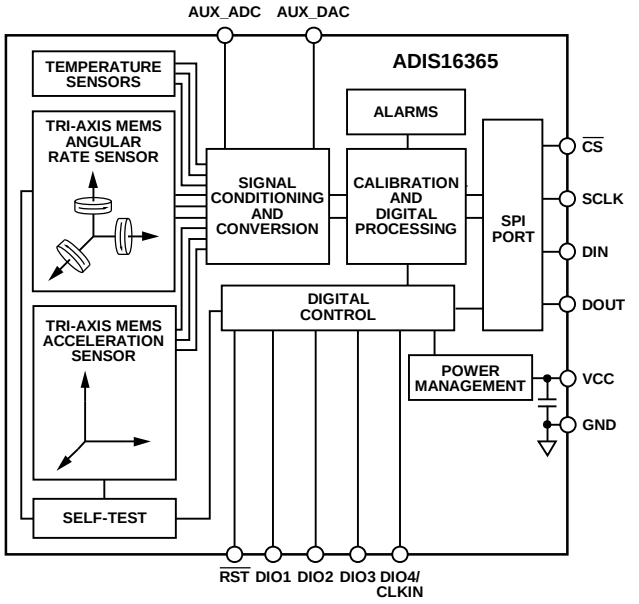

Figure 1.

GENERAL DESCRIPTION

The ADIS16365 *i*Sensor® is a complete triple axis gyroscope and triple axis accelerometer inertial sensing system. This sensor combines the Analog Devices, Inc., *i*MEMS® and mixed signal processing technology to produce a highly integrated solution that provides calibrated, digital inertial sensing. An SPI interface and simple output register structure allow for easy access to data and configuration controls.

The SPI port provides access to the following embedded sensors: X-, Y-, and Z-axis angular rates; X-, Y-, and Z-axis linear acceleration; internal temperature; power supply; and auxiliary analog input. The inertial sensors are precision-aligned across axes and are calibrated for offset and sensitivity over the industrial temperature range of −40 to +85°C. An embedded controller dynamically compensates for all major influences on the sensors, thus maintaining highly accurate sensor outputs without further testing, circuitry, or user intervention.

The following programmable features simplify system integration: in-system autobias calibration, digital filtering and sample rate, self-test, power management, condition monitoring, and auxiliary digital input/output.

This compact module is approximately 23 mm × 23 mm × 23 mm and provides a convenient flex-based connector system.

Rev. PrA

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SPECIFICATIONS

T_A = −40°C to +85°C, V_{CC} = 5.0 V, angular rate = 0°/sec, dynamic range = 300°/sec, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
GYROSCOPE SENSITIVITY	Each axis				
Initial Sensitivity	25°C, dynamic range = ±300°/sec	0.0405	0.05	0.0505	°/sec/LSB
	25°C, dynamic range = ±150°/sec		0.025		°/sec/LSB
	25°C, dynamic range = ±75°/sec		0.0125		°/sec/LSB
Temperature Coefficient			40		ppm/°C
Gyroscope Axis Nonorthogonality	25°C, difference from 90° ideal		TBD		Degree
Gyroscope Axis Misalignment	25°C, relative to base plate and guide pins		±0.5		Degree
Nonlinearity	Best fit straight line		0.1		% of FS
GYROSCOPE BIAS					
In-Run Bias Stability	25°C, 1 σ		0.007		°/sec
Angular Random Walk	25°C		2.4		°/√hr
Temperature Coefficient			0.1		°/sec/°C
Linear Acceleration Effect	Any axis, 1 σ (MSC_CTRL bit [7] = 1)		0.05		°/sec/*g*
Voltage Sensitivity	VCC = 4.75 V to 5.25 V		0.25		°/sec/V
GYROSCOPE NOISE PERFORMANCE					
Output Noise	25°C, ±300°/sec range, 1-tap filter setting		TBD		°/sec rms
	25°C, ±150°/sec range, 4-tap filter setting		TBD		°/sec rms
	25°C, ±75°/sec range, 16-tap filter setting		TBD		°/sec rms
Rate Noise Density	25°C, f = 25 Hz, ±300°/sec, no filtering		TBD		°/sec/√Hz rms
GYROSCOPE FREQUENCY RESPONSE					
3 dB Bandwidth			350		Hz
Sensor Resonant Frequency			14		kHz
GYROSCOPE SELF-TEST STATE					
Change in output bias	±300°/sec range setting	±833	±1500	±2167	LSB
Internal Self-Test Cycle Time			25		ms
ACCELEROMETER SENSITIVITY	Each axis				
Dynamic Range			±17		*g*
Initial Sensitivity	25°C	TBD	0.33	TBD	m*g*/LSB
Temperature Coefficient			40		ppm/°C
Axis Nonorthogonality	25°C, difference from 90° ideal		±0.25		Degree
Axis Misalignment	25°C, relative to base plate and guide pins		±0.5		Degree
Nonlinearity	Best fit straight line		±0.2		% of FS
ACCELEROMETER BIAS					
In-Run Bias Stability	25°C, 1 σ		TBD		m*g*
Velocity Random Walk	25°C, 1 σ		TBD		m/sec/√hr
Temperature Coefficient			TBD		m*g*/°C
ACCELEROMETER NOISE PERFORMANCE					
Output Noise	25°C, no filtering		TBD		m*g* rms
Noise Density	25°C, no filtering		TBD		m*g*/√Hz rms
ACCELEROMETER FREQUENCY RESPONSE					
3 dB Bandwidth			TBD		Hz
Sensor Resonant Frequency			TBD		kHz
ACCELEROMETER SELF-TEST STATE					
Output Change When Active			TBD		LSB
TEMPERATURE SENSOR					
Scale Factor	+25°C output = 0x0000		6.88		LSB/°C

Parameter	Conditions	Min	Typ	Max	Unit
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		+3.3	V
Input Capacitance	During acquisition		20		pF
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		±4		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range				+3.3	V
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS[1]					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
	$\overline{CS}$ signal to wake up from sleep mode			0.55	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All Except $\overline{RST}$			−40	−60	µA
$\overline{RST}$			−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[1]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SLEEP TIMER					
Timeout Period[2]		0.5		128	Sec
FLASH MEMORY					
Endurance[3]		10,000			Cycles
Data Retention[4]	TJ = 85°C	20			Years
START-UP TIME[5]	Time until data is available				
Power-On	Fast mode, SMPL_PRD ≤ 0x07		TBD		ms
	Normal mode, SMPL_PRD ≥ 0x08		TBD		ms
Reset Recovery	Fast mode, SMPL_PRD ≤ 0x07		TBD		ms
	Normal mode, SMPL_PRD ≥ 0x08		TBD		ms
Sleep Mode Recovery			TBD		ms
CONVERSION RATE					
Sample Rate Settings	SMPL_PRD = 0x01 to 0xFF	0.413		819.2	SPS
Clock Accuracy			TBD		
SYNC Input Clock				1.2	kHz

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range, VCC		4.75	5.0	5.25	V
Power Supply Current	Low power mode at 25°C		24		mA
	Fast mode at 25°C		49		mA
	Sleep mode at 25°C		500		µA

[1] The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.
[2] Guaranteed by design.
[3] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature (T_J) 85°C as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature.
[5] The times presented in this section do not include the sensor's transient response time, which is associated with a 50 Hz single-pole system. System accuracy goals should be given consideration when determining the amount of time it takes to start acquiring accurate readings. These times do not include the time it takes to arrive at thermal stability, which can also introduce transient errors.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = +5 V, unless otherwise noted.

Table 2.

Parameter	Description	Fast Mode (SMPL_PRD ≤ 0x09)			Low Power Mode (SMPL_PRD ≥ 0x0A)			Burst Mode			Unit
		Min[1]	Typ	Max	Min[1]	Typ	Max	Min[1]	Typ	Max	
f_{SCLK}		0.01		2.0	0.01		0.3	0.01		1.0	MHz
t_{STALL}	Stall period between data	9			75			$1/f_{SCLK}$			µs
t_{CS}	Chip select to clock edge	48.8			48.8			48.8			ns
t_{DAV}	DOUT valid after SCLK edge			100			100			100	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			24.4			24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			48.8			48.8			ns
t_{SCLKR}, t_{SCLKF}	SCLK Rise/Fall times		5	12.5		5	12.5		5	12.5	ns
t_{DF}, t_{DR}	DOUT rise/fall times		5	12.5		5	12.5		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	5			5			5			ns

[1]Guaranteed by design, not tested.

TIMING DIAGRAMS

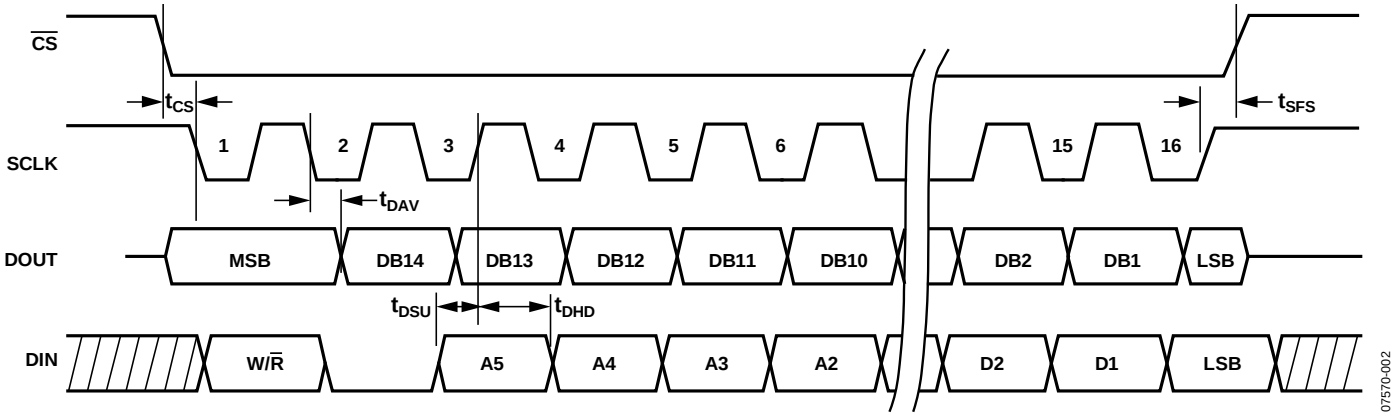

Figure 2. SPI Timing and Sequence

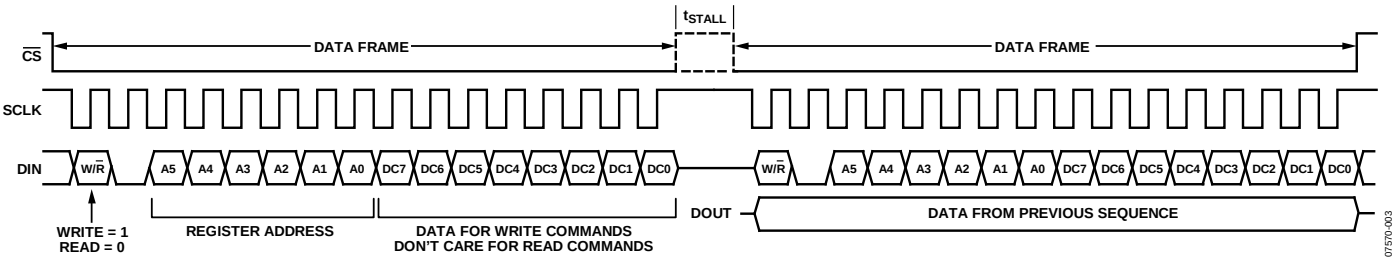

Figure 3. DIN Bit Sequence

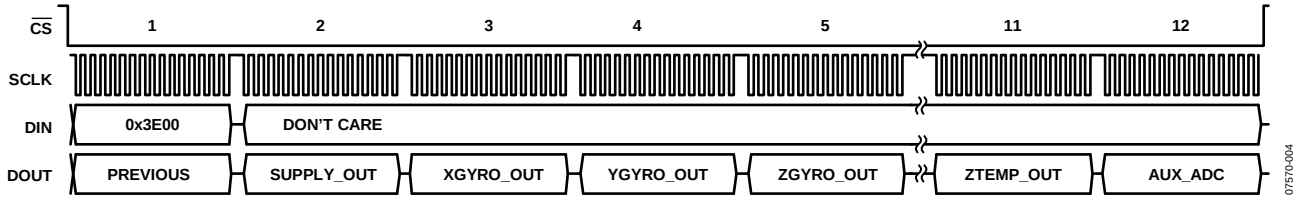

Figure 4. Burst Mode Read Sequence

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VCC to GND	−0.3 V to +6.0 V
Digital Input/Output Voltage to GND	−0.3 V to +5.3 V
Analog Inputs to GND	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C[1,2]

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +85°C.

[2] Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module	39.8°C/W	14.2°C/W	16 grams

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

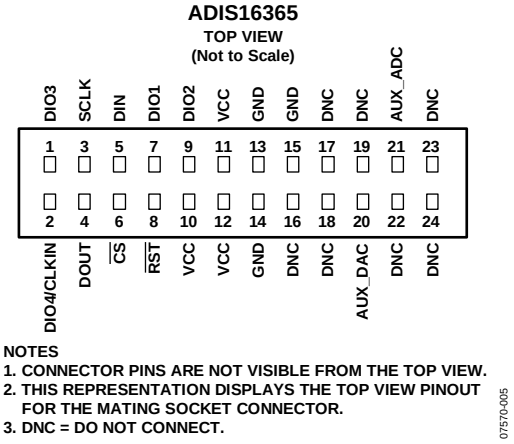

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DIO3	I/O	Configurable Digital Input/Output
2	DIO4/CLKIN	I/O	Configurable Digital Input/Output or Clock Input
16, 17, 18, 19, 22, 23, 24	DNC	N/A	Do Not Connect
3	SCLK	I	SPI Serial Clock
4	DOUT	O	SPI Data Output
5	DIN	I	SPI Data Input
6	$\overline{CS}$	I	SPI Chip Select
7	DIO1	I/O	Configurable Digital Input/Output
8	$\overline{RST}$	I	Reset
9	DIO2	I/O	Configurable Digital Input/Output
10, 11, 12	VCC	S	Power Supply
13, 14, 15	GND	S	Power Ground
20	AUX_DAC	O	Auxiliary, 12-Bit, DAC Output
21	AUX_ADC	I	Auxiliary, 12-Bit, ADC Input

[1] S = supply, O = output, I = input.

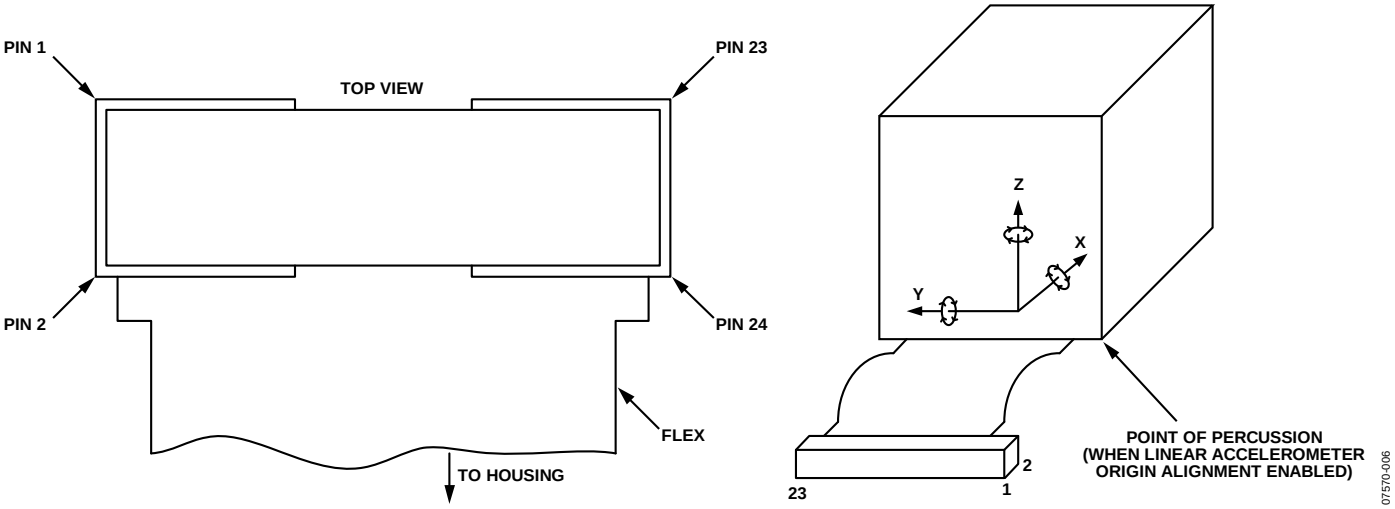

Figure 6. Pin Configuration, Connector Top View

TYPICAL PERFORMANCE CHARACTERISTICS

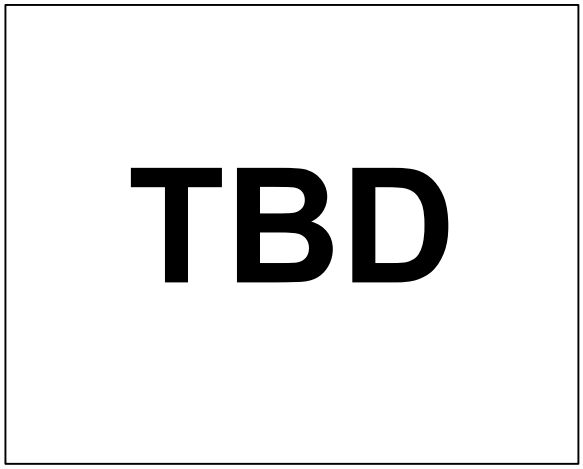

Figure 7.

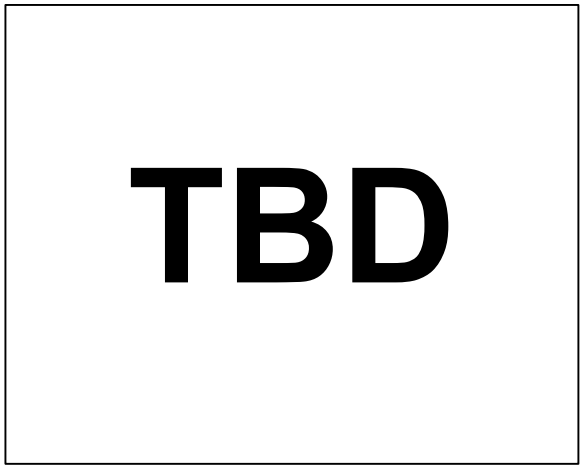

Figure 10.

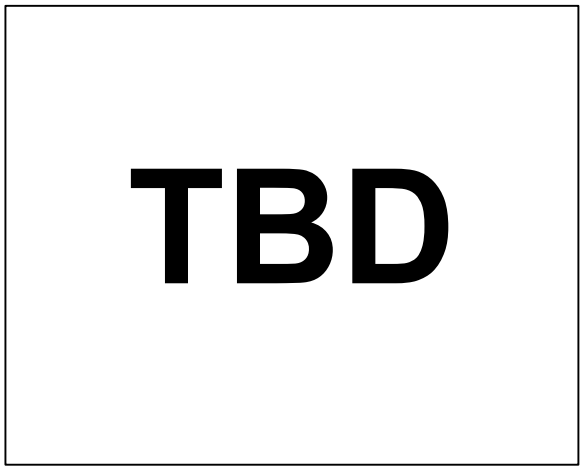

Figure 8.

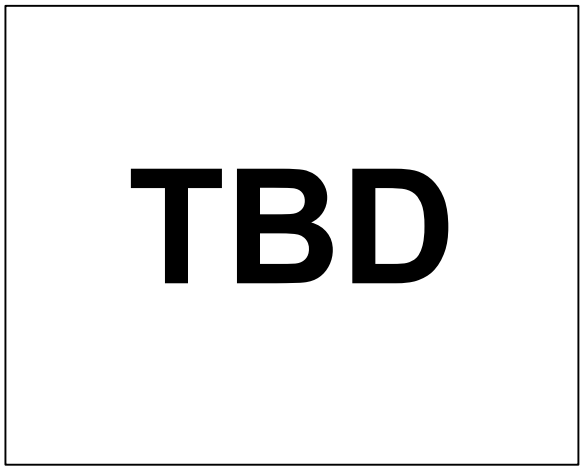

Figure 11.

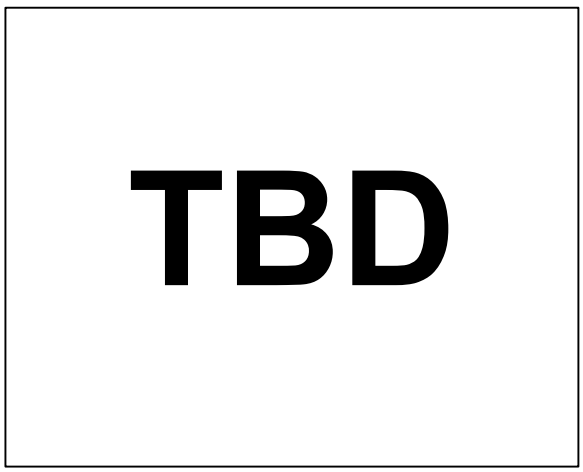

Figure 9.

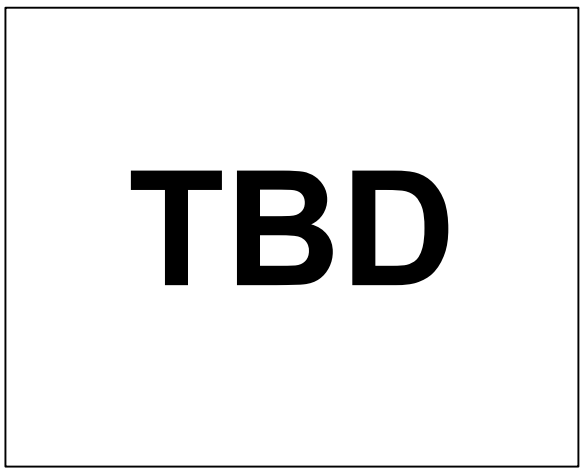

Figure 12.

BASIC OPERATION

The ADIS16365 runs off an internal clock and requires no external initialization. Once the power supply reaches 4.75 V, the ADIS16365 executes an internal initialization sequence and then starts producing data. At this point, the DIO1 will start pulsing as well, repeating each time new data loads into the output registers. This data-ready signal serves as an interrupt service signal, telling the system processor that the device is awake and producing data.

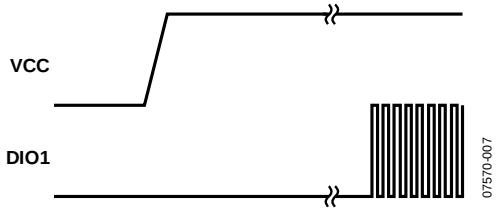

Figure 13. Start-Up Sequence

PHYSICAL INSTALLATION

The ADIS16365 provides slots on each side for attachment. These slots accommodate either 2-56 or 2 mm machine screws. Attach the body of the ADIS16365 to the proper surface prior to inserting the electrical connector, which is located at the end of the flex.

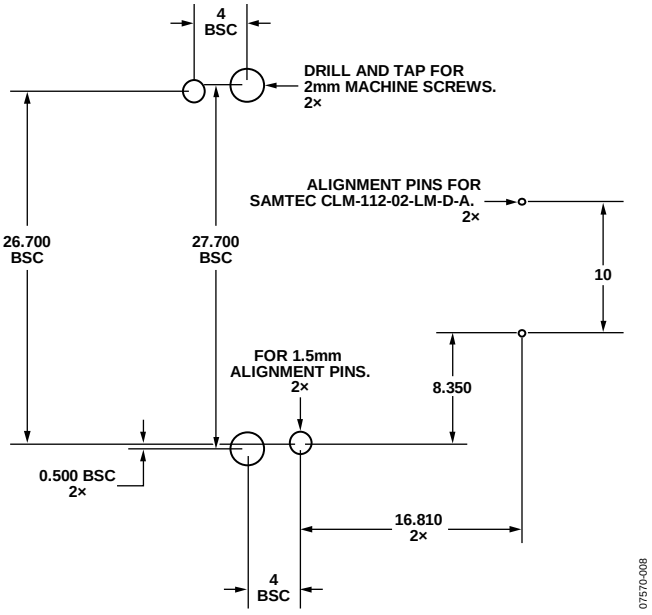

Figure 14. Typical Hole Pattern for the ADIS16365 Attachment

INITIAL HOOK-UP AND CONFIGURATION

The electrical connection uses a 24-pin header that mates to either the CLM or MLE family of connectors from Samtec. The evaluation system for this product uses Samtec part number: CLM-112-02-LM-D-A. Samtec is the appropriate source for suggested pad layout geometries for this mating connector. Although this device runs off a +5 V power supply, the digital lines are compatible with +3.3 V-digital I/O systems.

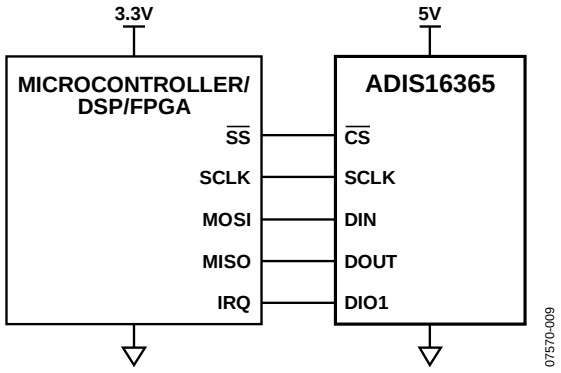

Figure 15. Electrical Hook-Up Diagram

All of the output data and configuration options have 16-bit registers assigned to govern their operation. Each byte has its own unique 6-bit address, which provides user access using the serial peripheral interface (SPI). While SPI is a common digital interface, most digital processor platforms accommodate several configuration options. The parameters listed in Table 6 are configuration options that SPI-compatible digital processor platforms offer in configuration registers. This table is a guide for determining how to configure them for communication with the ADIS16365.

Table 6. Typical Processor SPI Configuration Settings

Processor Setting	Notes
Master	The ADIS16365 operates as a slave.
SCLK Rate ≤ 2MHz (See Table 2)	Derived from a master clock, which is divided down to meet this requirement.
CPOL = 1	Clock polarity.
CPHA = 1	Clock phase.
MSB-first	Bit sequence.
16-bit data cycles	For an 8-bit processor, this requires two back-to-back 8-bit spi_read commands, while keeping the chip-select line low.

DATA COLLECTION

The ADIS16365 produces data outputs in 16-bit segments, based on the previous 16-bit configuration sequence. The bit assignments for the configuration sequence are in Figure 3. For a read command, only the first eight bits require definition. The first two bits are zero, and the next six bits represent the register's lower byte, listed in Table 7. When using 8-bit microcontrollers, use two back-to-back SPI read calls, while keeping the chip select line low. A typical code example for an 8-bit microcontroller may look like the following:

```
Chip_Select = 0;
high_byte = spi_read(0x06);
low_byte = spi_read(0x00);
Chip_Select = 1;
delay 0.01ms (stall time)
```

DEVICE CONFIGURATION

The ADIS16365 SPI provides device configuration control as well, eight bits at a time. Each function has a configurable register, which governs its operation, as listed in Table 7. In Figure 3, the first byte contains the write bit and register address. For example, the first byte of a write to the SMPL_PRD is 0x80 (write bit high) plus 0x36 (low-byte address), which is 0xB6. The second byte of the DIN sequence contains the data, which loads into the specified location. For the lowest sample rate setting, 0xFF is the code. The entire DIN sequence for setting the slowest sample rate is 0xB6FF.

Many of the configuration registers have also been assigned mirror locations in the flash memory, which effectively provides them with a backup storage function. To assure the backup of these registers, the COMMAND register provides an initiation bit for manual flash updates. The ENDURANCE register provides a running count of these events.

BURST MODE DATA COLLECTION

Burst mode data collection offers a more process-efficient method for collecting data from the ADIS16365. In 12 sequential data cycles, separated by only one SCLK time period, all 11-output registers clock out on DOUT. In Figure 4, this sequence starts when the DIN sequence is 0x3E00. After that, the contents of each output register, comes out of DOUT, starting with SUPPLY_OUT and ending with AUX_ADC. The addressing sequence determines the order of the outputs in burst mode.

Table 7. User Register Map

Name	R/W	Flash Backup	Address	Size (Bytes)	Function	Reference
ENDURANCE	R	Yes	0x00	2	Flash memory write count	
SUPPLY_OUT	R	No	0x02	2	Power supply measurement	Table 8
XGYRO_OUT	R	No	0x04	2	X-axis gyroscope output	Table 8
YGYRO_OUT	R	No	0x06	2	Y-axis gyroscope output	Table 8
ZGYRO_OUT	R	No	0x08	2	Z-axis gyroscope output	Table 8
XACCL_OUT	R	No	0x0A	2	X-axis accelerometer output	Table 8
YACCL_OUT	R	No	0x0C	2	Y-axis accelerometer output	Table 8
ZACCL_OUT	R	No	0x0E	2	Z-axis accelerometer output	Table 8
XTEMP_OUT	R	No	0x10	2	X-axis gyroscope temperature measurement	Table 8
YTEMP_OUT	R	No	0x12	2	Y-axis gyroscope temperature measurement	Table 8
ZTEMP_OUT	R	No	0x14	2	Z-axis gyroscope temperature measurement	Table 8
AUX_ADC	R	No	0x16	2	Auxiliary ADC output	Table 8
			0x18	2	Reserved	
XGYRO_OFF	R/W	Yes	0x1A	2	X-axis gyroscope bias offset factor	Table 9
YGYRO_OFF	R/W	Yes	0x1C	2	Y-axis gyroscope bias offset factor	Table 9
ZGYRO_OFF	R/W	Yes	0x1E	2	Z-axis gyroscope bias offset factor	Table 9
XACCL_OFF	R/W	Yes	0x20	2	X-axis acceleration bias offset factor	Table 10
YACCL_OFF	R/W	Yes	0x22	2	Y-axis acceleration bias offset factor	Table 10
ZACCL_OFF	R/W	Yes	0x24	2	Z-axis acceleration bias offset factor	Table 10
ALM_MAG1	R/W	Yes	0x26	2	Alarm 1 amplitude threshold	Table 19
ALM_MAG2	R/W	Yes	0x28	2	Alarm 2 amplitude threshold	Table 19
ALM_SMPL1	R/W	Yes	0x2A	2	Alarm 1 sample size	Table 20
ALM_SMPL2	R/W	Yes	0x2C	2	Alarm 2 sample size	Table 20
ALM_CTRL	R/W	Yes	0x2E	2	Alarm control	Table 21
AUX_DAC	R/W	No	0x30	2	Auxiliary DAC data	Table 16
GPIO_CTRL	R/W	No	0x32	2	Auxiliary digital input/output control	Table 18
MSC_CTRL	R/W	Yes	0x34	2	Miscellaneous control	Table 17
SMPL_PRD	R/W	Yes	0x36	2	Internal sample period (rate) control	Table 13
SENS/AVG	R/W	Yes	0x38	2	Dynamic range/digital filter control	Table 15
SLP_CNT	R/W	No	0x3A	2	Sleep mode control	Table 14
STATUS	R	No	0x3C	2	System status	Table 22
COMMAND	R/W	N/A	0x3E	2	System command	Table 12

OUTPUT DATA REGISTERS

Table 8 provides the data configuration for each output data register in the ADIS16365. Starting with the MSB of the upper byte, each output data register has the following bit sequence: new data (ND) flag, error/alarm (EA) flag, followed by 14 data bits. The data bits are LSB-justified and, in the case of the 12-bit data formats, the remaining two bits are not used. The ND flag indicates that unread data resides in the output data registers. This flag clears and returns to 0 during an output register read sequence. It returns to 1 after the next internal sample update cycle completes. The EA flag indicates an error condition. The STATUS register contains all of the error flags and provides the ability to investigate the root cause.

Table 8. Output Data Register Formats

Register	Bits	Format	Scale
SUPPLY_OUT[1]	12	Binary, +5V = 0x	2.418 mV
XGYRO_OUT[2]	14	Twos complement	0.05°/sec
YGYRO_OUT[2]	14	Twos complement	0.05°/sec
ZGYRO_OUT[2]	14	Twos complement	0.05°/sec
XACCL_OUT	14	Twos complement	3.33 m*g*
YACCL_OUT	14	Twos complement	3.33 m*g*
ZACCL_OUT	14	Twos complement	3.33 m*g*
XTEMP_OUT[3]	12	Binary, 25°C = 0x04FE	0.1453°C
YTEMP_OUT[3]	12	Binary, 25°C = 0x04FE	0.1453°C
ZTEMP_OUT[3]	12	Binary, 25°C = 0x04FE	0.1453°C
AUX_ADC	12	Binary = 0x04FE	0.8059 mV

[1] 5 V = 2730 LSBs (nominal).
[2] Assumes that the scaling is set to 300°/sec. This factor scales with the range.
[3] Typical condition, 25°C = 0 LSB.

CALIBRATION

Manual Bias Calibration

The bias offset registers in Table 9 and Table 10 provide a manual adjustment function for each sensor's output. For example, if an output offset of 0.125°/sec is observed in the Z-axis gyroscope, the ZGYRO_OFF register provides the calibration factor necessary to improve the accuracy. Using the sensitivity of 0.0125°/sec, an adjustment of −10 LSBs is required. The twos complement, hexadecimal code of −10 LSBs is 0x1FF6. See Table 11 for the DIN command.

Table 9. X,Y,ZGYRO_OFF Register Bits

Bits	Description	(Default = 0x0000)
[15:13]	Not used.	
[12:0]	Data bits. Twos complement, 0.0125°/sec per LSB. Typical adjustment range = ±50°/sec.	

Table 10. X,Y,ZACCL_OFF Register Bits

Bits	Description	(Default = 0x0000)
[15:12]	Not used.	
[11:0]	Data bits, Twos complement 3.3 mg/LSB. Typical adjustment range = ±6 *g*.	

Automatic Bias Null Calibration

This single-command calibration function is in the COMMAND register and measures all three-gyroscope output registers, then loads the three bias correction registers with values that return their outputs to zero (null). See Table 11 for the DIN command.

Precision Automatic Bias Null Calibration

This single-command calibration function is in the COMMAND register and incorporates a 30-second average of all three gyroscope output registers, then loads the three bias correction registers with values that return their outputs to zero (null). For optimal calibration accuracy, the device should be stable (no motion) for this entire period. Once it has started, a reset is the only way to stop it prematurely, if required. See Table 11 for the DIN command.

Restoring Factory Calibration

This single command is in the COMMAND register and restores the factory calibration by writing 0x0000 into each bias offset register listed in Table 9 and Table 10. This command also flushes all of the data from the digital filter taps. See Table 11 for the DIN command.

Linear Acceleration Bias Compensation (Gyroscopes)

This function enables compensation for low-frequency acceleration influences on gyroscope bias behavior, using the MSC_CTRL register. See Table 11 for the DIN command.

Linear Acceleration Origin Alignment

This function enables origin alignment for the accelerometers to the point of percussion (see Figure 6), using the MSC_CTRL register. See Table 11 for the DIN command.

Table 11. Calibration Commands

Calibration Function	DIN Word(s)
Adjust Z-Axis Gyroscope Bias by −0.125°/sec: Write 0x1F to 0x1F Write 0xF6 to 0x1E (ZGYRO_OFF)	0x9E1F 0x9FF6
Automatic Bias Null: Write 0x01 to 0x3E (COMMAND)	0xBE01
Precision Automatic Bias Null: Write 0x10 to 0x3E (COMMAND)	0xBE10
Factory Calibration Restore: Write 0x02 to 0x3E (COMMAND)	0xBE02
Enable Linear Acceleration Bias Compensation for the Gyroscopes: Write 0x86 to 0x34 (MSC_CTRL)	0xB486
Enable Origin Alignment for the Accelerometer Sensors: Write 0x46 to 0x34 (MSC_CTRL)	0xB446

The last two entries assume factory default conditions for the MSC_CTRL register. The contents may vary, depending on the other MSC_CTRL settings. See Table 17 for further description of each bit in this register.

OPERATION CONTROL REGISTERS

Global Commands

In addition to the calibration commands, the COMMAND register provides initiation bits for several other common functions. Writing a 1 to the assigned COMMAND bit exercises its function.

Table 12. COMMAND Bit Descriptions

Bits	Description
[15:8]	Not used
[7]	Software reset command
[6:5]	Not used
[4]	Precision autonull command
[3]	Flash update command
[2]	Auxiliary DAC data latch
[1]	Factory calibration restore command
[0]	Autonull command

The software reset command restarts the internal processor, which loads all registers with the contents in their flash memory locations.

The flash update copies the contents of all flash backup registers into their assigned, nonvolatile, flash memory locations. This process takes approximately 50 ms and requires a power supply that is within the specified operating range. After waiting the appropriate time for the flash update to complete, verify successful completion by reading the STATUS register. If the flash update is successful, the flash update error is 0. If the flash update is not successful, reading this error bit accomplishes two things: (1) alerting the system processor to try again, and (2) clearing the error flag, which is required for flash memory access.

The DAC data latch command loads the contents of AUX_DAC into the DAC latches. Because the AUX_DAC contents must be updated one byte at a time, this command ensures a stable DAC output voltage during updates.

Finally, reading the COMMAND register (see

Figure 4) starts the burst mode read sequence.

Internal Sample Rate

The SMPL_PRD register controls the ADIS16365 internal sample rate and has two parts: a selectable time base and a multiplier. The following relationship produces the sample rate:

$$t_S = t_B \times N_S + 1$$

Table 13. SMPL_PRD Bit Descriptions

Bit	Description	(Default = 0x0001)
[15:8]	Not used	
[7]	Time base, 0 = 0.61035 ms, 1 = 18.921 ms	
[6:0]	Increment setting (N_S)	

An example calculation of the default sample period follows:

$SMPL\_PRD$ = 0x03, $B7 - B0$ = 00000011 ->

$B7 = 0 \rightarrow t_B$ = 0.61035 ms, $B6 \ldots B0$ = 000000011 $\rightarrow N_S = 3$

$t_S = t_B \times (N_S + 1)$ = 0.61035 ms × (3+1) = 2.4414 ms

The contents of this register determine whether the device is in fast mode or low power mode." Fast mode occurs when the contents of SMPL_PRD are less than 0x0A. Refer to Table 1 and Table 2 for the performance trade-offs associated with each mode. Setting SMPL_PRD = 0x000 activates the external clock.

Power Management

In addition to offering two different performance modes for power optimization, the ADIS16365 offers a programmable shutdown period that the SLP_CNT register controls.

Table 14. SLP_CNT Bit Descriptions

Bit	Description	(Default = 0x0000)
[15:8]	Not used	
[7:0]	Data bits, 0.5 seconds/LSB (0x08, sleep time = 4 sec)	

Once in sleep mode, a reset or power cycle is required to wake up.

Digital Filtering

The signal conditioning circuit of each sensor has an analog bandwidth of approximately 350 Hz. A programmable-length Bartlett window FIR filter provides opportunity for additional noise reduction on all output data registers. The SENS/AVG register controls the number of taps in power-of-two step sizes, from zero to six.

Filter setup requires one simple step: write the appropriate M factor to the assigned bits in the SENS/AVG register. The bit assignments are listed in Table 15. The frequency response relationship for this filter is

$$H_B(f) = H_A^2(f) \quad H_A(f) = \frac{\sin(\pi \times N \times f \times t_s)}{N \times \sin(\pi \times f \times t_s)}$$

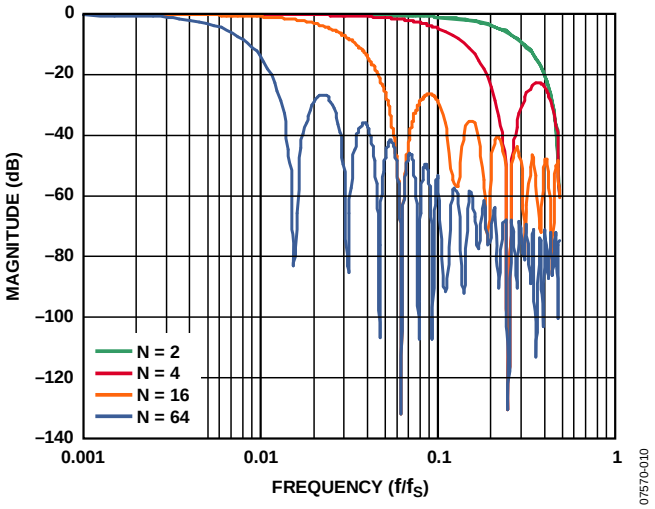

Figure 16. Bartlett Window FIR Frequency Response

Dynamic Range

There are three dynamic range settings: ±75°/sec, ±150°/sec, and ±300°/sec. The lower dynamic range settings (75, 150) limit the minimum filter tap sizes to maintain the resolution as the measurement range decreases. The recommended order for programming the SENS/AVG register is upper byte (sensitivity), followed by lower byte (filtering). The contents of the SENS/AVG register are nonvolatile.

Table 15. SENS/AVG Bit Descriptions

Bits	Value	Description (Default = 0x0000)
[15:11]		Not used
[10:8]		Measurement range (sensitivity) selection
	100	300°/sec (default condition)
	010	150°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02)
	001	75°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04)
[7:3]		Not used
[2:0]		Filter tap setting, number of taps, N = 2^M; for example, 011, N = 2^3 = 8 taps

INPUT/OUTPUT FUNCTIONS

The ADIS16365 provides several input/output functions, including a 12-bit ADC, a 12-bit DAC, and four general purpose, digital input/output lines that have several configuration options.

Auxiliary ADC

The auxiliary ADC is a standard 12-bit ADC that digitizes other system-level analog signals. The output of the ADC can be monitored through the AUX_ADC register, as defined in Table 8. The ADC is a 12-bit successive approximation converter. The output data is presented in straight binary format with the full-scale range extending from 0 V to 3.3 V.

Figure 17 shows the equivalent circuit of the analog input structure of the ADC. The input capacitor (C1) is typically 4 pF and can be attributed to parasitic package capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals are never outside the range of −0.3 V to +3.5 V. Signals outside this range cause the diodes to become forward-biased and to start conducting.

The diodes can handle 10 mA without causing irreversible damage. The resistor is a lumped component that represents the on resistance of the switches. The value of this resistance is typically 100 Ω. Capacitor C2 represents the ADC sampling capacitor and is typically 16 pF.

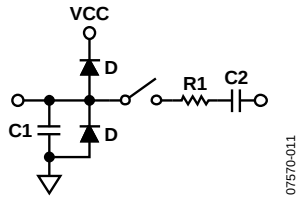

Figure 17. Equivalent Analog Input Circuit
Conversion Phase: Switch Open
Track Phase: Switch Closed

For ac applications, it is recommended that high frequency components from the analog input signal be removed by using a low-pass filter on the analog input pin.

In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input must be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ.

Auxiliary DAC

The auxiliary DAC provides a 12-bit level adjustment function. The AUX_DAC register controls the operation of the auxiliary DAC function, which is useful for systems that require analog level controls. It offers a rail-to-rail buffered output that has a range of 0 V to 3.3 V. The DAC can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches ground, the linearity begins to degrade (100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC output latch function, contained in the COMMAND register, provides continuous operation while writing to each byte of this register. The contents of this register are volatile, which means that the desired output level must be set after every reset and power cycle event.

Table 16. AUX_DAC Bit Descriptions

Bit	Description (Default = 0x0000)
[15:12]	Not used
[11:0]	Data bits, scale factor = 0.8059 mV/code
	Offset binary format, 0 V = 0 codes

Data-Ready I/O Indicator

The MSC_CTRL register provides controls for a data-ready function. For example, writing 0x05 to this register enables this function and establishes DIO2 as an active-low, data-ready line. The duty cycle is 25% (±10% tolerance).

Table 17. MSC_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Not used
[11]	Flash test
[10]	Internal self-test enable (clears on completion) 1 = enabled, 0 = disabled
[9]	Manual self-test, negative stimulus 1 = enabled, 0 = disabled
[8]	Manual self-test, positive stimulus 1 = enabled, 0 = disabled
[7]	Linear acceleration bias compensation for gyroscopes 1 = enabled, 0 = disabled
[6]	Linear accelerometer origin alignment 1 = enabled, 0 = disabled
[5:3]	Not used
[2]	Data-ready enable, 1 = enabled, 0 = disabled
[1]	Data-ready polarity, 1 = active high, 0 = active low
[0]	Data-ready line select, 1 = DIO2, 0 = DIO1

General Purpose I/O

The GPIO_CTRL register controls the direction and data of the general-purpose digital lines, DIO1 through DIO4. For example, writing a 0x02 to the GPIO_CTRL register sets DIO2 as an output line and DIO1, DIO3, and DIO4 as input lines. Reading the data bits in GPIO_CTRL reveals the logic level of each line.

Table 18. GPIO_CTRL Bit Descriptions

Bit	Description (Default = 0x0000)
[15:12]	Not used
[11]	General-Purpose I/O Line 4 data level
[10]	General-Purpose I/O Line 3 data level
[9]	General-Purpose I/O Line 2 data level
[8]	General-Purpose I/O Line 1 data level
[7:4]	Not used
[3]	General-Purpose I/O Line 4, data direction control 1 = output, 0 = input
[2]	General-Purpose I/O Line 3, data direction control 1 = output, 0 = input
[1]	General-Purpose I/O Line 2, data direction control 1 = output, 0 = input
[0]	General-Purpose I/O Line 1, data direction control 1 = output, 0 = input

DIAGNOSTICS

Self-Test

Self-test exercises the mechanical structure of the sensor and provides a simple method for verifying the operation of the entire sensor signal conditioning circuit. There are two different self-test options: startup and manual. If either of these self-tests results in a failure, the self-test error flag, located in the STATUS register, sets to 1. The manual self-test option results in a repeating pattern, until the bit is set back to 0. While in the manual self-test loop, SMPL_PRD and AVG_CNT cannot be changed. See Table 17 for the appropriate MSC_CTRL bit designations.

Alarm Registers

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source, data filtering (prior to comparison), static/dynamic, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations. The ALM_SMPLx registers provide the numbers of samples to use in the dynamic, rate-of-change configuration. The rate-of-change calculation is

$$Y_C = \frac{1}{N_{DS}} \sum_{n=1}^{N_{DS}} y(n+1) - y(n) \Rightarrow Alarm \Rightarrow \text{is } Y_C > \text{or} < M_C ?$$

where:
N_{DS} is the number of samples in ALM_SMPLx.
$y(n)$ is the sampled output data.
M_C is the magnitude for comparison in ALM_MAGx.
> or < is determined by the MSB in ALM_MAGx.

Table 19. ALM_MAG1/ALM_MAG2 Bit Designations

Bit	Description (Default = 0x0000)
[15]	Comparison polarity: 1 = greater than, 0 = less than
[14]	Not used
[13:0]	Data bits, matches format of trigger source selection

Table 20. ALM_SMPL1/ALM_SMPL2 Bit Designations

Bit	Description (Default = 0x0001)
[15:8]	Not used
[7:0]	Data bits: number of samples (both 0x00 and 0x01 = 1)

Table 21. ALM_CTRL Bit Designations

Bits	Value	Description (Default = 0x0000)
[15:12]		Alarm 2 source selection
	0000	Disable
	0001	Power supply output
	0010	X-axis gyroscope output
	0011	Y-axis gyroscope output
	0100	Z-axis gyroscope output
	0101	X-axis accelerometer output
	0110	Y-axis accelerometer output
	0111	Z-axis accelerometer output
	1000	X-axis gyroscope temperature output
	1001	Y-axis gyroscope temperature output
	1010	Z-axis gyroscope temperature output
	1011	Auxiliary ADC input
[11:8]		Alarm 1 source selection (same as Alarm 2)
[7]		Rate of change (ROC) enable for Alarm 2 1 = rate of change, 0 = static level
[6]		Rate of change (ROC) enable for Alarm 1 1 = rate of change, 0 = static level
[5]		Not used
[4]		Comparison data filter setting[1] 1 = filtered data, 0 = unfiltered data
[3]		Not used
[2]		Alarm output enable 1 = enabled, 0 = disabled
[1]		Alarm output polarity 1 = active high, 0 = active low
[0]		Alarm output line select 1 = DIO2, 0 = DIO1

[1] Incline and vertical angles always use filtered data in this comparison.

Status

The STATUS register provides a series of error flags that provide indicator functions for common system-level issues. All of the flags clear (set to 0) after each STATUS register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle.

Table 22. STATUS Bit Descriptions

Bit	Description (Default = 0x0000)
[15:10]	Not used
[9]	Alarm 2 status 1 = active, 0 = inactive
[8]	Alarm 1 status 1 = active, 0 = inactive
[7]	Not used
[6]	Flash failure
[5]	Self-test diagnostic error flag 1 = error condition, 0 = normal operation
[4]	Not used
[3]	SPI communications failure 1 = error condition, 0 = normal operation
[2]	Flash update failed 1 = error condition, 0 = normal operation
[1]	Power supply above 5.25 V 1 ≥ 5.25 V, 0 ≤ 5.25 V (normal)
[0]	Power supply below 4.75 V 1 ≤ 4.75 V, 0 ≥ 4.75 V (normal)

OUTLINE DIMENSIONS

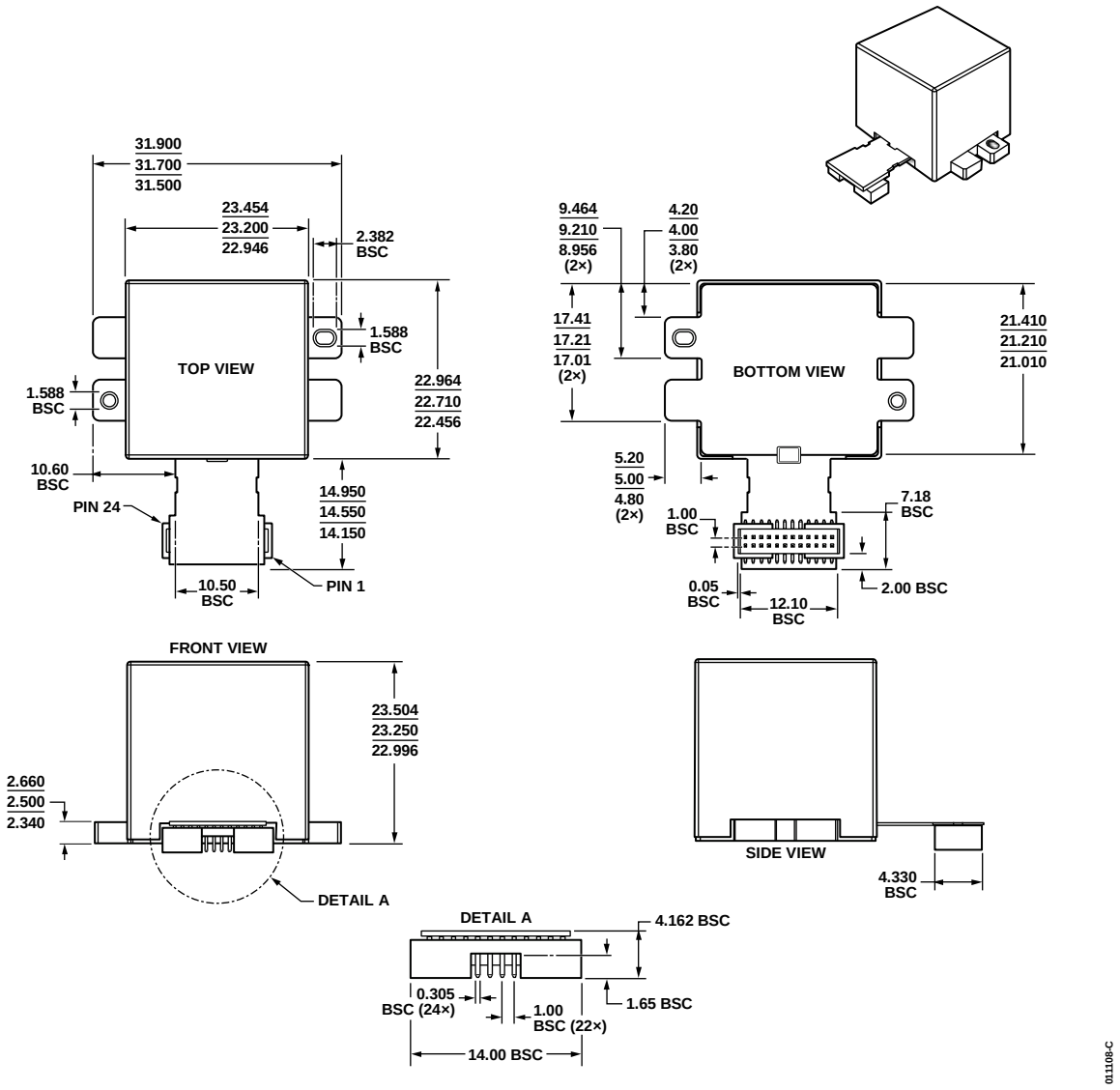

Figure 18. 24-Lead Module with Connector Interface
(ML-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16365BMLZ[1]	–40°C to +105°C	24-Lead Module with Connector Interface	ML-24-2
ADIS16365/PCBZ[1]		Interface Board	

[1] Z = RoHS Compliant Part.

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