ADJD-S311-CR999

Miniature Surface Mount RGB Digital Color Sensor

Data Sheet

Description

The ADJD-S311-CR999 is a cost effective, 4 channels (RGB+CLEAR) digital output sensor in miniature surface-mount package with a mere size of 2.2 x 2.2 x 0.76mm. It is a CMOS IC with integrated RGB filters and analog-to-digital converter front end. This device is designed to cater for wide dynamic range of illumination level and is ideal for applications like portable or mobile devices, which demand higher integration, smaller size and low power consumption. Sensitivity control is performed by the serial interface and can be optimized individually for the different color channel. The sensor can also be used in conjunction with a white LED for reflective color management.

Applications

- General color detection and measurement
- Mobile appliances such as mobile phones, PDAs, MP3 players,etc.
- Consumer appliances
- Portable medical equipments
- Portable color detector/reader

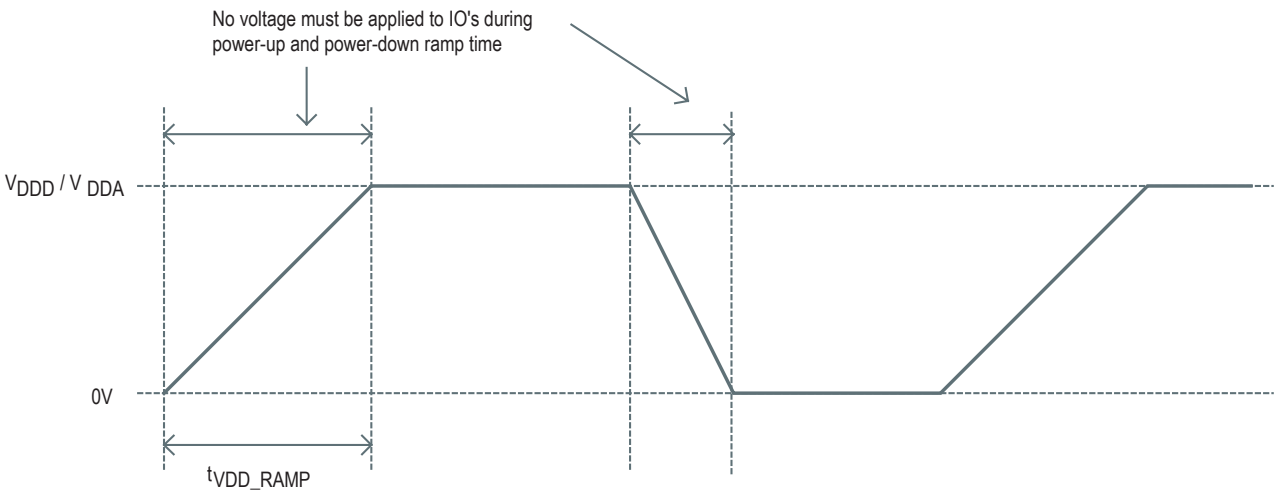
Features

- Fully integrated RGB+clear digital color sensor
- 10 bit resolution per channel output
- Built in oscillator/selectable external clock
- Low supply voltage (VDD) 2.5V
- Digital I/O via 2-wire serial interface
- Adjustable sensitivity for different levels of illumination
- Low power mode (sleep mode)
- Independent gain selection for each channel
- 0°C to 70°C operating temperature
- Industry's smallest form factor
  – CSP 2.2 x 2.2 x 0.76mm
- Lead free package

General Specifications

Feature	Value
Interface	100kHz serial interface
Supply	2.6V digital (nominal), 2.6V analog (nominal)

Powering the Device



ESD Protection Diode Turn-On During Power-Up and Power-Down

A particular power-up and power-down sequence must be used to prevent any ESD diode from turning on inadvertently. The figure above describes the sequence. In general, AVDD and DVDD should power-up and power-down together to prevent ESD diodes from turning on inadvertently. During this period, no voltage should be applied to the IO's for the same reason.

Ground Connection

AGND and DGND must both be set to 0V and preferably star-connected to a central power source as shown in the application diagram. A potential difference between AGND and DGND may cause the ESD diodes to turn on inadvertently.

Electrical Specifications

Absolute Maximum Ratings (Notes 1 & 2)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage temperature	T_{STG_ABS}	-40	85	°C	
Digital supply voltage, DVDD to DVSS	V_{DDD_ABS}	2.5	3.6	V	
Analog supply voltage, AVDD to AVSS	V_{DDA_ABS}	2.5	3.6	V	
Input voltage	V_{IN_ABS}	2.5	3.6	V	All I/O pins
Solder Reflow Peak temperature	T_{L_ABS}		245	°C	
Human Body Model ESD rating	ESD_{HBM_ABS}		2	kV	All pins, human body model per JESD22-A114-B

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Free air operating temperature	T_A	0	25	70	°C
Digital supply voltage, DVDD to DVSS	V_{DDD}	2.5	2.6	3.6	V
Analog supply voltage, AVDD to AVSS	V_{DDA}	2.5	2.6	3.6	V
Output current load high	I_{OH}			3	mA
Output current load low	I_{OL}			3	mA
Input voltage high level (Note 4)	V_{IH}	$0.7V_{DDD}$		V_{DDD}	V
Input voltage low level (Note 4)	V_{IL}	0		$0.3V_{DDD}$	V

DC Electrical Specifications

Over Recommended Operating Conditions (unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Output voltage high level (Note 5)	V_{OH}	I_{OH} = 3mA	V_{DDD}-0.8	V_{DDD}-0.4		V
Output voltage low level (Note 6)	V_{OL}	I_{OH} = 3mA		0.2	0.4	V
Supply current (Note 7)	I_{DD_STATIC}	(Note 8)		3.8	5	mA
Sleep-mode supply current (Note 7)	I_{DD_SLP}	(Note 8)		2		uA
Input leakage current	I_{LEAK}		-10		10	uA

AC Electrical Specifications

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Internal clock frequency	$f_{\_CLK\_int}$			26		MHz
External clock frequency	$f_{\_CLK\_ext}$		16		40	MHz
2-wire interface frequency	$f_{\_2wire}$			100		kHz

Optical Specification

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Dark offset	V_D	Ee = 0		20		LSB

Minimum sensitivity (note 3)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Irradiance Responsivity	Re	λ_P = 460 nm, B Refer Note 9		152		LSB/ ($mWcm^{-2}$)
		λ_P = 542 nm, G Refer Note 10		178		
		λ_P = 645 nm, R Refer Note 11		254		
		λ_P = 645 nm, Clear Refer Note 11		264		

Maximum sensitivity (note 3)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Irradiance Responsivity	Re	λ_P = 460 nm, B Refer Note 9		3796		LSB/ ($mWcm^{-2}$)
		λ_P = 542 nm, G Refer Note 10		4725		
		λ_P = 645 nm, R Refer Note 11		6288		
		λ_P = 645 nm, Clear Refer Note 11		6590		

Saturation Irradiance for minimum sensitivity (note 12)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Saturation Irradiance		λ_P = 460 nm, B Refer Note 9		6.73		mW/cm^2
		λ_P = 542 nm, G Refer Note 10		5.74		
		λ_P = 645 nm, R Refer Note 11		4.03		
		λ_P = 645 nm, Clear Refer Note 11		3.87		

Saturation irradiance for maximum sensitivity (note 12)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Saturation Irradiance		λ_P = 460 nm, B Refer Note 9		0.27		mW/cm^2
		λ_P = 542 nm, G Refer Note 10		0.22		
		λ_P = 645 nm, R Refer Note 11		0.16		
		λ_P = 645 nm, Clear Refer Note 11		0.16		

Notes
1. The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The device should not be operated at these limits. The parametric values defined in the "Electrical Specifications" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Specified at room temperature (25°C) and $V_{DDD} = V_{DDA} = 2.5V$.
4. Applies to all DI pins.
5. Applies to all digital output pins. SDASLV go tri-state when output logic high. Minimum V_{OH} depends on the pull-up resistor value.

Notes: (continued)
6 . Applies to all digital output and digital input-output pins.
7 . Refers to total device current consumption.
8. Output and bidirectional pins are not loaded.
9. Test condition is blue light of peak wavelength (λ_P) 460 nm and spectral half width ($\Delta\lambda_{1/2}$) 25 nm.
10. Test condition is green light of peak wavelength (λ_P) 542 nm and spectral half width ($\Delta\lambda_{1/2}$) 35 nm
11. Test condition is red light of peak wavelength (λ_P) 645 nm and spectral half width ($\Delta\lambda_{1/2}$) 20 nm
12. Saturation irradiance = (MSB)/ (Irradiance responsivity)

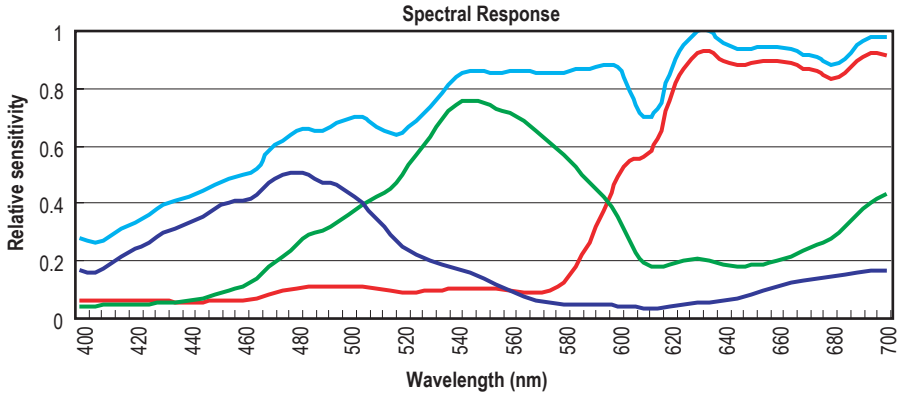


Figure 1. Typical spectral response when the gains for all the color channels are set at equal.

Serial Interface Timing Information

Parameter	Symbol	Minimum	Maximum	Units
SCL clock frequency	f_{scl}	0	100	kHz
(Repeated) START condition hold time	$t_{HD:STA}$	4	-	µs
Data hold time	$t_{HD:DAT}$	0	3.45	µs
SCL clock low period	t_{LOW}	4.7	-	µs
SCL clock high period	t_{HIGH}	4.0	-	µs
Repeated START condition setup time	$t_{SU:STA}$	4.7	-	µs
Data setup time	$t_{SU:DAT}$	250	-	ns
STOP condition setup time	$t_{SU:STO}$	4.0	-	µs
Bus free time between START and STOP conditions	t_{BUF}	4.7	-	µs

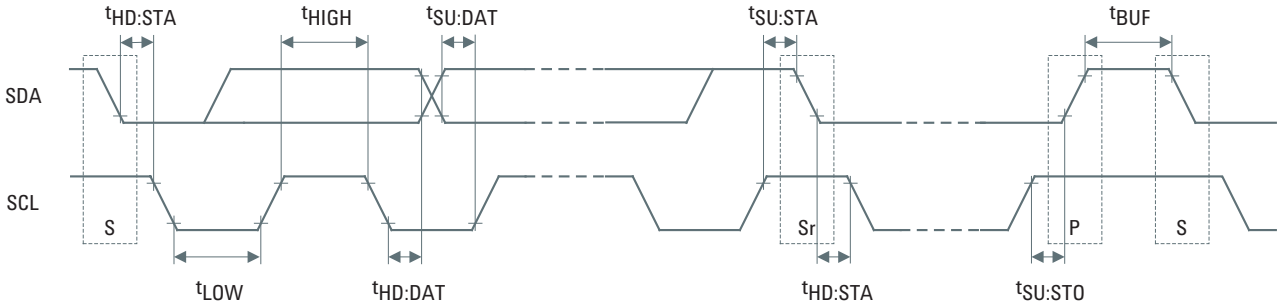


Figure 2. Serial Interface Bus Timing Waveforms

Serial Interface Reference

Description

The programming interface to the ADJD-S311 is a 2-wire serial bus. The bus consists of a serial clock (SCL) and a serial data (SDA) line. The SDA line is bi-directional on ADJD-S311 and must be connected through a pull-up resistor to the positive power supply. When the bus is free, both lines are HIGH.

The 2-wire serial bus on ADJD-S311 requires one device to act as a master while all other devices must be slaves. A master is a device that initiates a data transfer on the bus, generates the clock signal and terminates the data transfer while a device addressed by the master is called a slave. Slaves are identified by unique device addresses.

Both master and slave can act as a transmitter or a receiver but the master controls the direction for data transfer. A transmitter is a device that sends data to the bus and a receiver is a device that receives data from the bus.

The ADJD-S311 serial bus interface always operates as a slave transceiver with a data transfer rate of up to 100kbit/s.

START/STOP Condition

The master initiates and terminates all serial data transfers. To begin a serial data transfer, the master must send a unique signal to the bus called a START condition. This is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH.

The master terminates the serial data transfer by sending another unique signal to the bus called a STOP condition. This is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

The bus is considered to be busy after a START (S) condition. It will be considered free a certain time after the STOP (P) condition. The bus stays busy if a repeated START (Sr) is sent instead of a STOP condition.

The START and repeated START conditions are functionally identical. See figure 3.

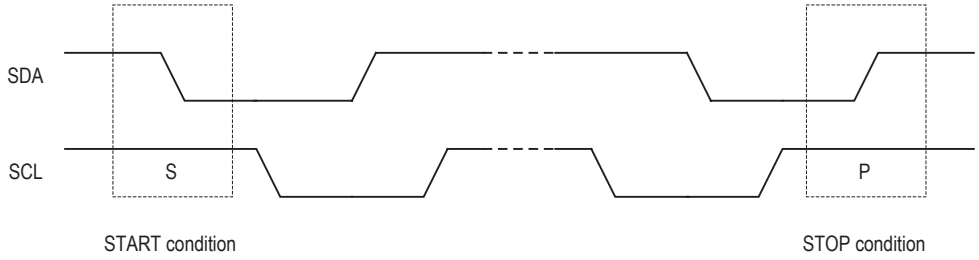


Figure 3. START/STOP Condition

Data Transfer

The master initiates data transfer after a START condition. Data is transferred in bits with the master generating one clock pulse for each bit sent. For a data bit to be valid, the SDA data line must be stable during the HIGH period of the SCL clock line. Only during the LOW period of the SCL clock line can the SDA data line change state to either HIGH or LOW.

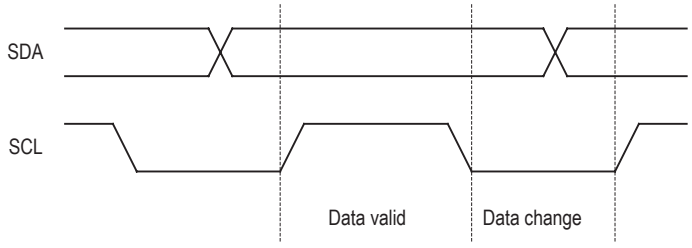


Figure 4. Data Bit Transfer

The SCL clock line synchronizes the serial data transmission on the SDA data line. It is always generated by the master. The frequency of the SCL clock line may vary throughout the transmission as long as it still meets the minimum timing requirements.

The master by default drives the SDA data line. The slave drives the SDA data line only when sending an acknowledge bit after the master writes data to the slave or when the master requests the slave to send data.

The SDA data line driven by the master may be implemented on the negative edge of the SCL clock line. The master may sample data driven by the slave on the positive edge of the SCL clock line. Figure shows an example of a master implementation and how the SCL clock line and SDA data line can be synchronized.

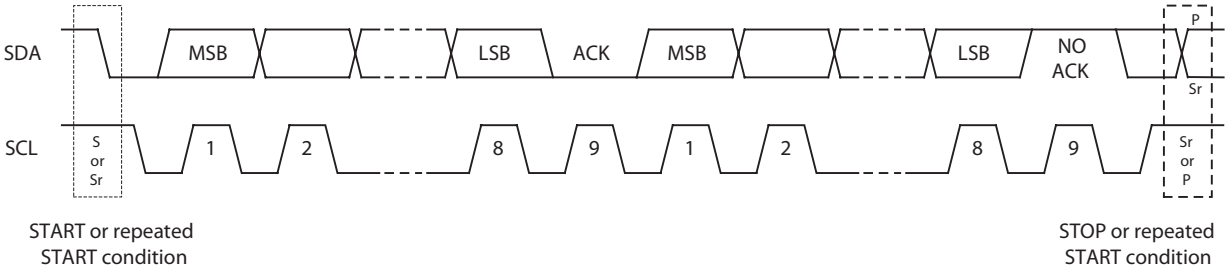


Figure 5. Data Byte Transfer

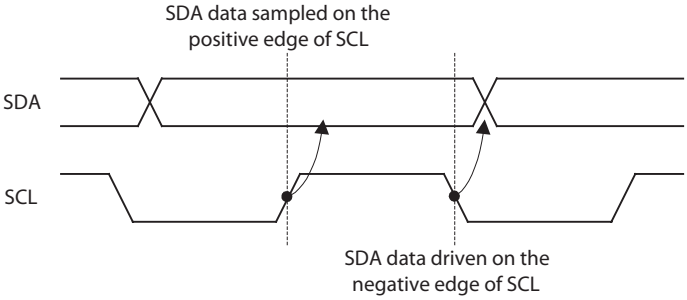


Figure 6. Data Bit Synchronization

A complete data transfer is 8-bits long or 1-byte. Each byte is sent most significant bit (MSB) first followed by an acknowledge or not acknowledge bit. Each data transfer can send an unlimited number of bytes (depending on the data format).

Acknowledge/Not acknowledge

The receiver must always acknowledge each byte sent in a data transfer. In the case of the slave-receiver and master-transmitter, if the slave-receiver does not send an acknowledge bit, the master-transmitter can either STOP the transfer or generate a repeated START to start a new transfer.

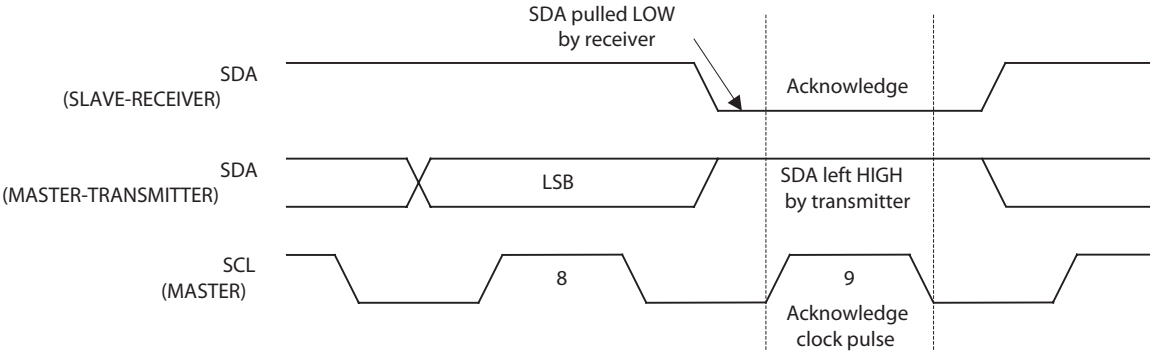


Figure 7. Slave-Receiver Acknowledge

In the case of the master-receiver and slave-transmitter, the master generates a not acknowledge to signal the end of the data transfer to the slave-transmitter. The master can then send a STOP or repeated START condition to begin a new data transfer.

In all cases, the master generates the acknowledge or not acknowledge SCL clock pulse.

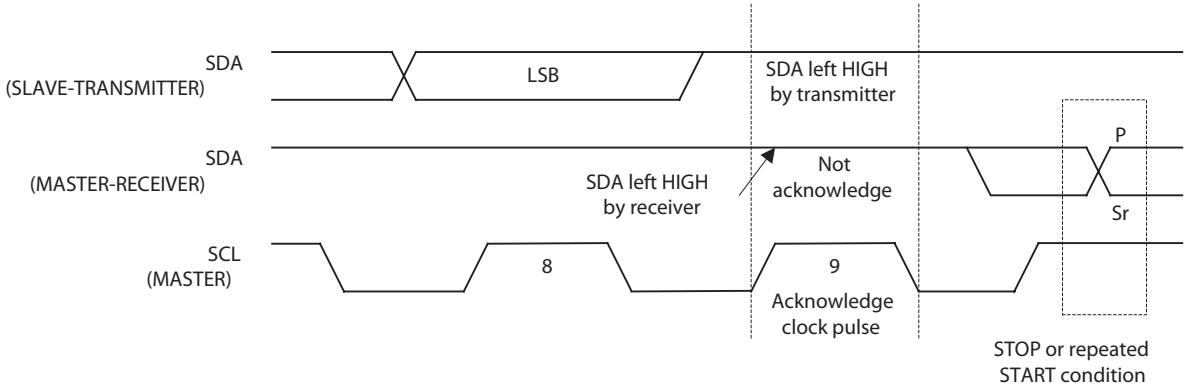


Figure 8. Master-Receiver Acknowledge

Addressing

Each slave device on the serial bus needs to have a unique address. This is the first byte that is sent by the master-transmitter after the START condition. The address is defined as the first seven bits of the first byte.

The eighth bit or least significant bit (LSB) determines the direction of data transfer. A 'one' in the LSB of the first byte indicates that the master will read data from the addressed slave (master-receiver and slave-transmitter). A 'zero' in this position indicates that the master will write data to the addressed slave (master-transmitter and slave-receiver).

A device whose address matches the address sent by the master will respond with an acknowledge for the first byte and set itself up as a slave-transmitter or slave-receiver depending on the LSB of the first byte.

The slave address on ADJD-S311 is 0x74 (7-bits).

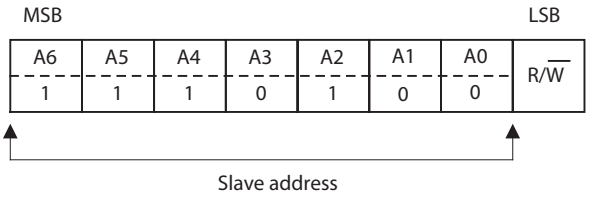


Figure 9. Slave Addressing

Data format

ADJD-S311 uses a register-based programming architecture. Each register has a unique address and controls a specific function inside the chip.

To write to a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then writes the new register data. Once the slave acknowledges, the master generates a STOP condition to end the data transfer.

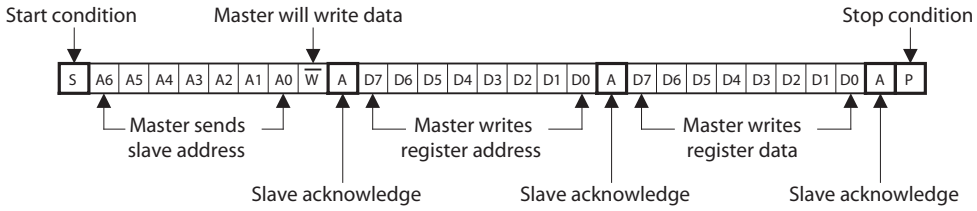


Figure 10. Register Byte Write Protocol

To read from a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then generates a repeated START condition and resends the slave address sent previously. The least significant bit (LSB) of the slave address must indicate that the master wants to read from the slave. The addressed device will then acknowledge the master.

The master reads the register data sent by the slave and sends a no acknowledge signal to stop reading. The master then generates a STOP condition to end the data transfer.

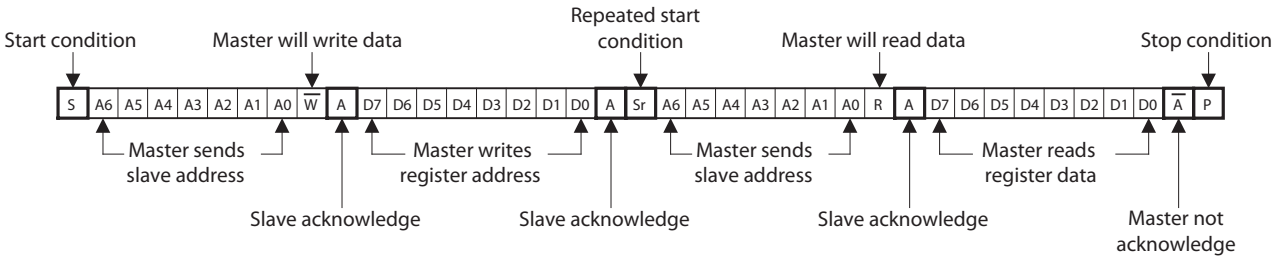


Figure 11. Register Byte Read Protocol

Application Diagram

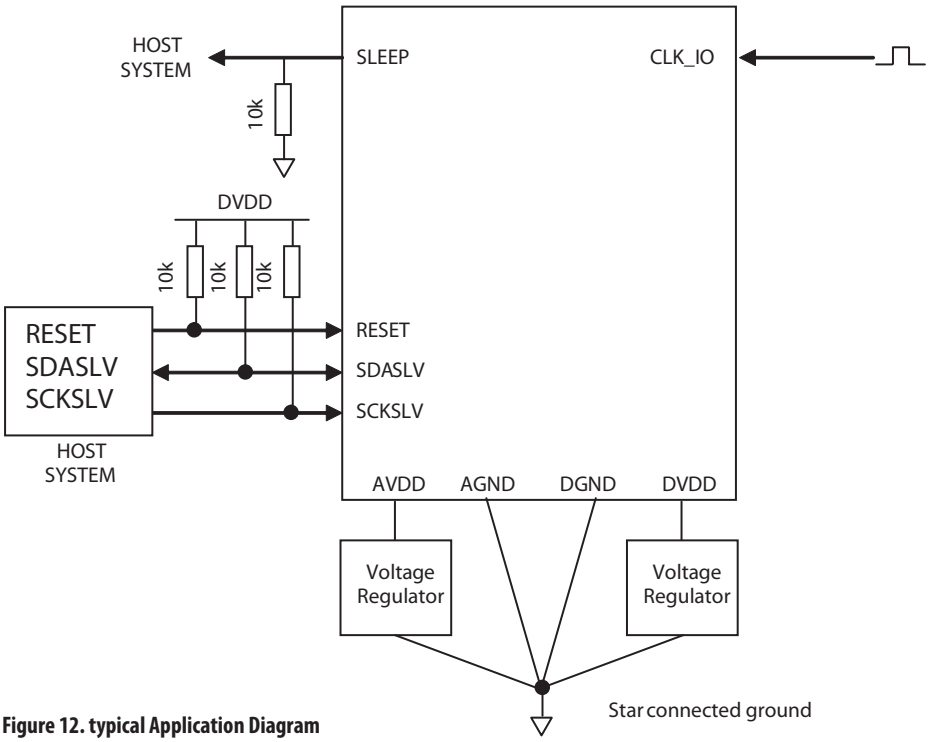
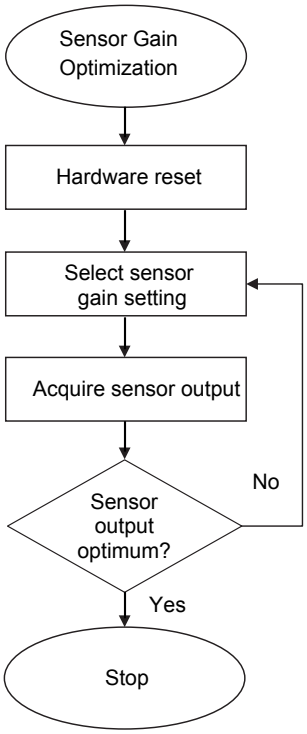


Figure 12. typical Application Diagram

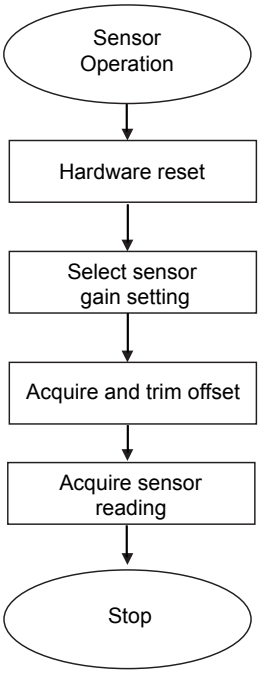
High Level Description

The sensor needs to be configured before it can be used. The gain selection needs to be set for optimum performance depending on light levels. The flowcharts below describe the different procedures required.

Sensor gain optimization flowchart



Sensor operation flowchart



* Please refer to application note for more detailed information.

Detail Description

A hardware reset (by asserting XRST) should be performed before starting any operation.

Sensor Gain Settings

The sensor gain can be adjusted by varying the number of capacitors and integration time slot of the sensor manually through the following registers.

Address (Hex)	Register	Description
6	CAP_RED	Number of red channel capacitors
7	CAP_GREEN	Number of green channel capacitors
8	CAP_BLUE	Number of blue channel capacitors
9	CAP_CLEAR	Number of clear channel capacitors
A	INT_RED	Number of red channel integration time slots
C	INT_GREEN	Number of green channel integration time slots
E	INT_BLUE	Number of blue channel integration time slots
10	INT_CLEAR	Number of clear channel integration time slots

Sensor ADC Output Registers

To obtain sensor ADC value, '01' Hex must be written to CTRL register. Then, read the value from CTRL register. If value is 00H, can read sensor output from data register.

Address (Hex)	Register	Description
00	CTRL	Control register
40	DATA_RED_LO	Red channel ADC data – low byte
41	DATA_RED_HI	Red channel ADC data – high byte
42	DATA_GREEN_LO	Green channel ADC data – low byte
43	DATA_GREEN_HI	Green channel ADC data – high byte
44	DATA_BLUE_LO	Blue channel ADC data – low byte
45	DATA_BLUE_HI	Blue channel ADC data – high byte
46	DATA_CLEAR_LO	Clear channel ADC data – low byte
47	DATA_CLEAR_HI	Clear channel ADC data – high byte

* Please refer to application note for more detailed information.

Setup Value for Number of Integration Time Slot

The following value can be written to each of the integration time registers to adjust the gain of the sensor. The default value after reset for these registers is 00H. These registers control the number of integration time selected for each channel. The integration time slot can be varied from 00H to FFFH. More integration time slot will give higher sensitivity.

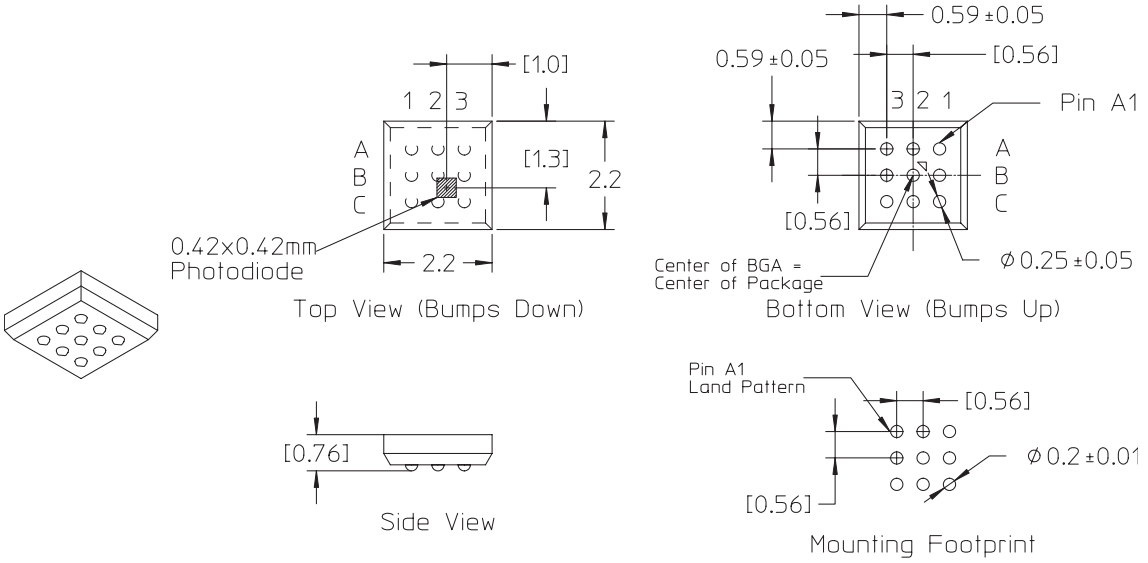
Setup Value for Number of Capacitor

The following value can be written to each of the capacitor registers to adjust the gain of the sensor. The default value after reset for these registers is 0FH. These registers control the number of capacitors selected for each channel. The maximum selectable capacitor is 16 with the registers starting from 0 (i.e. 0 to 15). Less capacitor will give higher sensitivity.

Value (Hex)	Number of Capacitor
00	1
01	2
02	3
03	4
04	5
05	6
06	7
07	8
08	9
09	10
0A	11
0B	12
0C	13
0D	14
0E	15
0F	16

* Please refer to application note for more detailed information.

Mechanical Drawing



Note:
1. Dimensions are in milimeters (mm)
2. Standard tolerances (unless otherwise specified)
   a. Linear tolerance = +/-0.1mm
   b. Angular tolerance = +/-1°

Pin Configuration

	1	2	3
A	DVDD	SCKSLV	AVDD
B	CLKIO	SDASLV	SLEEP
C	DGND	RESET	AGND

Dimensions

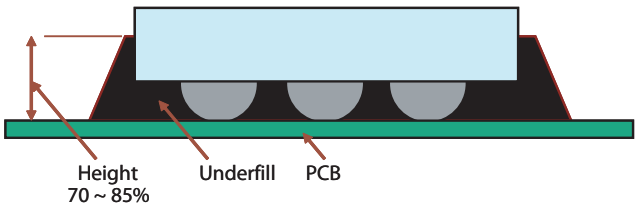
Description	Nominal (um)
Package Body Dimension X	2200
Package Body Dimension Y	2200
Package Height	760
Ball Diameter	250
Total Pin Count	9

Pin Information

Pin	Name	Type	Description
A1	DVDD	Power	Digital power pin
A2	SCKSLV	Input	Serial interface clock pin
A3	AVDD	Power	Analog power pin
B1	CLKIO	Input	External clock input
B2	SDASLV	Input/Output	Bidirectional data pin. A pull-up resistor should be tied to SDASLV because it goes tri-state to output logic 1
B3	SLEEP	Input	When SLEEP = 1, the device goes into sleep mode. In sleep mode, all analog circuits are powered down and the clock signal is gated away from the core logic resulting in very low current consumption.
C1	DGND	Ground	Tie to digital ground
C2	RESET	Input	Global, asynchronous, active-low system reset. When asserted low, XRST resets all registers. Minimum reset pulse low is 1us and must be provided by external circuitry.
C3	AGND	Power	Tie to analog ground

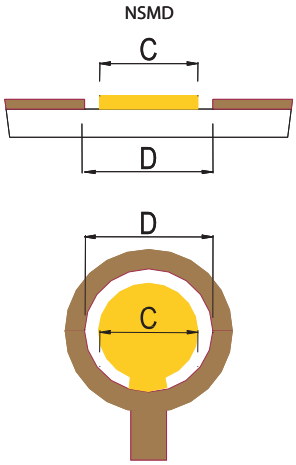
Recommended Underfill Type and Characteristic

- Henkel FP4548
- Low moisture absorption
- Low CTE
- Underfill up to 70-85% of height



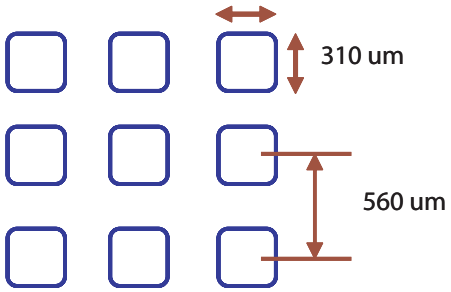
Recommended PCB land pad design

- NiAu flash over copper pad
- Pad Diameter (C)= 0.20 mm
- NSMD Diameter (D)= 0.25 ~ 0.30 mm



Recommended stencil design

- Stencil thickness 5 mils
- Stencil type Ni Electroforming
- Stencil Aperture Type Square
- Stencil Aperture 310 um
- Additional Feature Rounded square edge

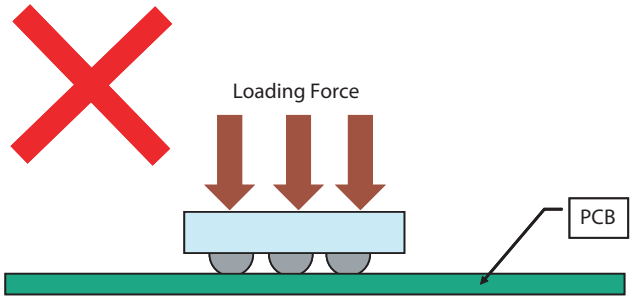


After soldering or mounting precaution

Please ensure that all soldered or reflowed CSP package that is mounted on the PCB is not exposed to compression or loading force directly perpendicular to the flat top surface.

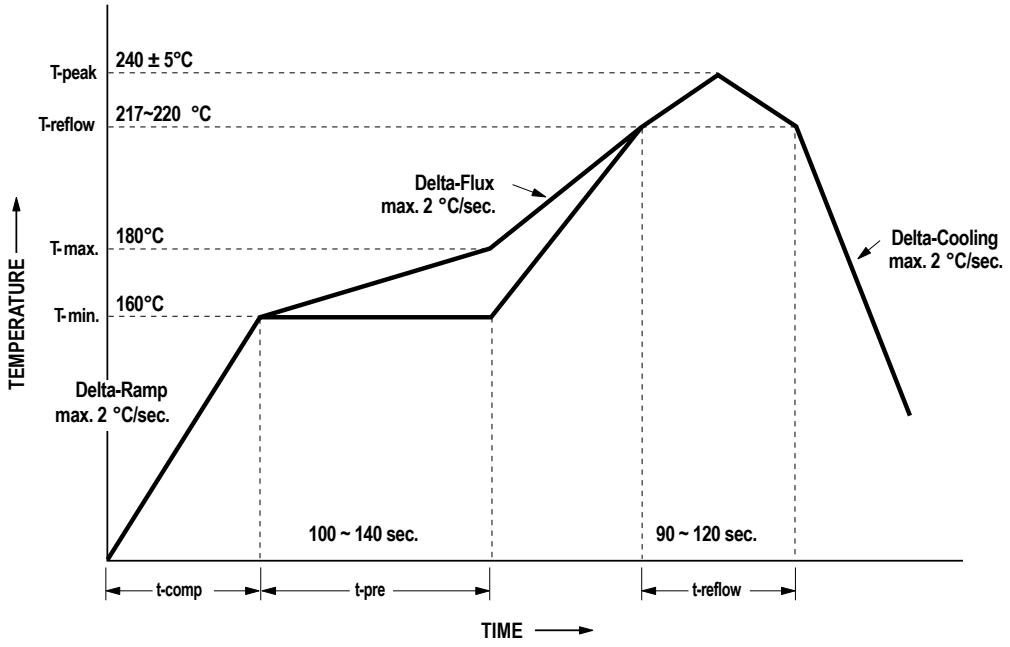
Precaution:

Excessive loading force directly perpendicular to the flat top surface may cause pre-mature failure.



Recommended Reflow Profile

It is recommended that Henkel Pb-free solder paste LF310 be used for soldering ADJD-S311-CR999. Below is the recommended reflow profile.



Recommendations for Handling and Storage of ADJD-S311-CR999

This product is qualified as Moisture Sensitive Level 3 per Jedec J-STD-020. Precautions when handling this moisture sensitive product is important to ensure the reliability of the product. Do refer to Avago Application Note AN5305 Handling Of Moisture Sensitive Surface Mount Devices for details.

A. Storage before use

- Unopened moisture barrier bag (MBB) can be stored at 30°C and 90%RH or less for maximum 1 year
- It is not recommended to open the MBB prior to assembly (e.g. for IQC)
- It should also be sealed with a moisture absorbent material (Silica Gel) and an indicator card (cobalt chloride) to indicate the moisture within the bag

B. Control after opening the MBB

- The humidity indicator card (HIC) shall be read immediately upon opening of MBB
- The components must be kept at <30°C/60%RH at all time and all high temperature related process including soldering, curing or rework need to be completed within 168hrs

C. Control for unfinished reel

- For any unused components, they need to be stored in sealed MBB with desiccant or desiccator at <5%RH

D. Control of assembled boards

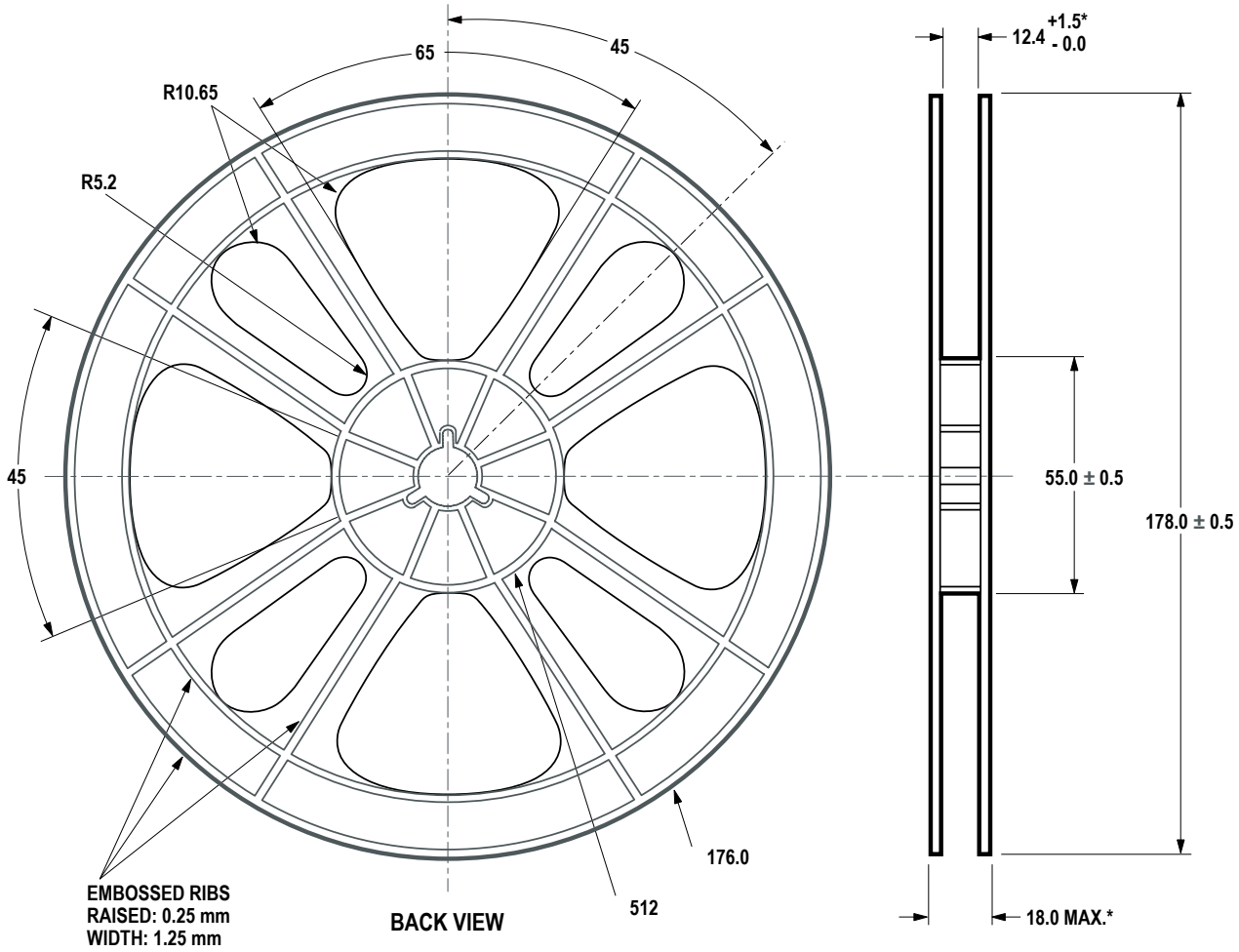
- If the PCB soldered with the components is to be subjected to other high temperature processes, the PCB need to be stored in sealed MBB with desiccant or desiccator at <5%RH to ensure no components have exceeded their floor life of 168hrs

E. Baking is required if:

- "10%" or "15%" HIC indicator turns pink
- The components are exposed to condition of >30°C/60%RH at any time.
- The components floor life exceeded 168hrs
- Recommended baking condition (in component form): 125°C for 24hrs

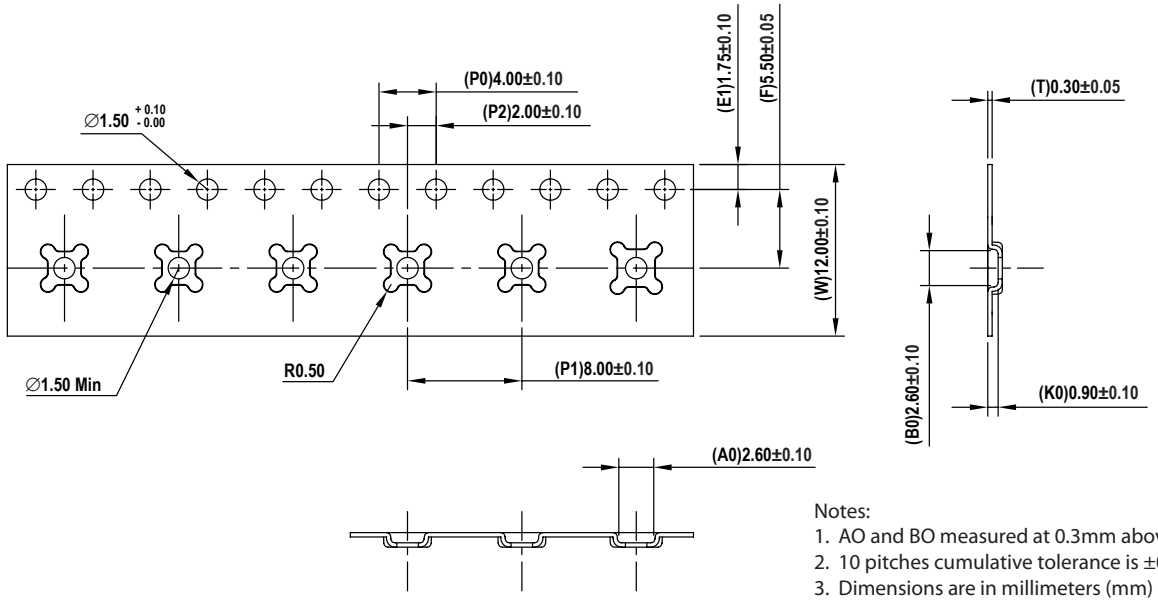
Package Tape and Reel Dimensions

Reel Dimensions



Notes:
1. *Measure at hub area.
2. All flange edges to be rounded.

Carrier Tape Dimensions



Notes:
1. AO and BO measured at 0.3mm above base of pocket
2. 10 pitches cumulative tolerance is ±0.2mm
3. Dimensions are in millimeters (mm)

Appendix A: Sensor Register List

	ADD (DEC)	ADD (HEX)	MNEMONIC	WIDTH	RESET (DEC)	TYPE	ACCESS	B7	B6	B5	B4	B3	B2	B1	B0	NOTES
FN	0	0	CTRL	2	0	BITS	R/W	N/A						GOFS	GSSR	
	1	1	CONFIG	3	0	BITS	R/W	N/A					EXTCLK	SLEEP	TOFS	
SENSOR	6	6	CAP_RED	4	15	NUMBER	R/W	N/A				CAP_RED[3:0]				
	7	7	CAP_GREEN	4	15	NUMBER	R/W	N/A				CAP_GREEN[3:0]				
	8	8	CAP_BLUE	4	15	NUMBER	R/W	N/A				CAP_BLUE[3:0]				
	9	9	CAP_CLEAR	4	15	NUMBER	R/W	N/A				CAP_CLEAR[3:0]				
	10	A	INT_RED_LO	8	0	NUMBER	R/W	INT_RED[7:0]								
	11	B	INT_RED_HI	8	0	NUMBER	R/W	INT_RED[11:8]								
	12	C	INT_GREEN_LO	8	0	NUMBER	R/W	INT_GREEN[7:0]								
	13	D	INT_GREEN_HI	8	0	NUMBER	R/W	INT_GREEN[11:8]								
	14	E	INT_BLUE_LO	8	0	NUMBER	R/W	INT_BLUE[7:0]								
	15	F	INT_BLUE_HI	8	0	NUMBER	R/W	INT_BLUE[11:8]								
	16	10	INT_CLEAR_LO	8	0	NUMBER	R/W	INT_CLEAR[7:0]								
	17	11	INT_CLEAR_HI	8	0	NUMBER	R/W	INT_CLEAR[11:8]								
SAMPLE DATA	64	40	DATA_RED_LO	8	0	NUMBER	R	DATA_RED[7:0]								
	65	41	DATA_RED_HI	3	0	NUMBER	R	N/A						DATA_RED[9:8]		
	66	42	DATA_GREEN_LO	8	0	NUMBER	R	DATA_GREEN[7:0]								
	67	43	DATA_GREEN_HI	3	0	NUMBER	R	N/A						DATA_GREEN[9:8]		
	68	44	DATA_BLUE_LO	8	0	NUMBER	R	DATA_BLUE[7:0]								11/10-bit data
	69	45	DATA_BLUE_HI	3	0	NUMBER	R	N/A						DATA_BLUE[9:8]		
	70	46	DATA_CLEAR_LO	8	0	NUMBER	R	DATA_CLEAR[7:0]								
	71	47	DATA_CLEAR_HI	3	0	NUMBER	R	N/A						DATA_CLEAR[9:8]		
OFFSET DATA	72	48	OFFSET_RED	8	0	NUMBER	R	SIGN_RED	OFFSET_RED[6:0]							
	73	49	OFFSET_GREEN	8	0	NUMBER	R	SIGN_GREEN	OFFSET_GREEN[6:0]							sign = 1 is -ve
	74	4A	OFFSET_BLUE	8	0	NUMBER	R	SIGN_BLUE	OFFSET_BLUE[6:0]							
	75	4B	OFFSET_CLEAR	8	0	NUMBER	R	SIGN_CLEAR	OFFSET_CLEAR[6:0]							

Appendix A: Sensor Register List

1) CTRL: Control Register

B7	B6	B5	B4	B3	B2	B1	B0
N/A						GOFS	GSSR

N/A	Not available.
GSSR	Get sensor reading. Active high and automatically cleared. Result is stored in registers 64-71 (DEC)
GOFS	Get offset reading. Active high and automatically cleared. Result is stored in registers 72-75 (DEC)

2) CONFIG: Configuration Register

B7	B6	B5	B4	B3	B2	B1	B0
N/A					EXTCLK	SLEEP	TOFS

N/A	Not available.
EXTCLK	External clock mode. Active high.
SLEEP	Sleep mode. Active high and external clock mode only. Automatically cleared if otherwise.
TOFS	Trim offset mode. Active high.

3) CAP_RED: Capacitor Settings Register for Red Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_RED[3:0]			

N/A	Not available.
CAP_RED	Number of red channel capacitors.

4) CAP_GREEN: Capacitor Settings Register for Green Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_GREEN[3:0]			

N/A	Not available.
CAP_GREEN	Number of green channel capacitors.

5) CAP_BLUE: Capacitor Settings Register for Blue Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_BLUE[3:0]			

N/A	Not available.
CAP_BLUE	Number of blue channel capacitors.

6) CAP_CLEAR: Capacitor Settings Register for Clear Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_CLEAR[3:0]			

N/A	Not available.
CAP_CLEAR	Number of clear channel capacitors.

7) INT_RED: Integration Time Slot Setting Register for Red Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_RED[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_RED[11:8]			

INT_RED	Number of red channel integration time slots.

8) INT_GREEN: Integration Time Slot Setting Register for Green Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_GREEN[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_GREEN[11:8]			

INT_GREEN	Number of green channel integration time slots.

9) INT_BLUE: Integration Time Slot Setting Register for Blue Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_BLUE[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_BLUE[11:8]			

INT_BLUE	Number of blue channel integration time slots.

10) INT_CLEAR: Integration Time Slot Setting Register for Clear Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_CLEAR[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_CLEAR[11:8]			

INT_CLEAR	Number of clear channel integration time slots.

11) DATA_RED_LO: Low Byte Register of Red Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_RED[7:0]							

DATA_RED	Red channel ADC data.

12) DATA_RED_HI: High Byte Register of Red Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_RED[9:8]	

N/A	Not available.
DATA_RED	Red channel ADC data.

13) DATA_GREEN_LO: Low Byte Register of Green Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_GREEN[7:0]							

DATA_GREEN	Green channel ADC data.

14) DATA_GREEN_HI: High Byte Register of Green Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_GREEN[9:8]	

N/A	Not available.
DATA_GREEN	Green channel ADC data.

15) DATA_BLUE_LO: Low Byte Register of Blue Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_BLUE[7:0]							

DATA_BLUE	Blue channel ADC data.

16) DATA_BLUE_HI: High Byte Register of Blue Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_BLUE[9:8]	

N/A	Not available.
DATA_BLUE	Blue channel ADC data.

17) DATA_CLEAR_LO: Low Byte Register of Clear Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_CLEAR[7:0]							

DATA_CLEAR	Clear channel ADC data.

18) DATA_CLEAR_HI: High Byte Register of Clear Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_CLEAR[9:8]	

N/A	Not available.
DATA_CLEAR	Clear channel ADC data.

19) OFFSET_RED: Offset Data Register for Red Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_RED	OFFSET_RED[6:0]						

SIGN_RED	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_RED	Red channel ADC offset data.

20) OFFSET_GREEN: Offset Data Register for Green Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_GREEN	OFFSET_GREEN[6:0]						

SIGN_GREEN	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_GREEN	Green channel ADC offset data.

21) OFFSET_BLUE: Offset Data Register for Blue Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_BLUE	OFFSET_BLUE[6:0]						

SIGN_BLUE	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_BLUE	Blue channel ADC offset data.

22) OFFSET_CLEAR: Offset Data Register for Clear Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_CLEAR	OFFSET_CLEAR[6:0]						

SIGN_CLEAR	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_CLEAR	Clear channel ADC offset data.

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