20 MHz to 500 MHz Dual IF Amplifier

Data Sheet **ADL5534**

FEATURES

Fixed gain of 20 dB
Operation up to 500 MHz
Input/output internally matched to 50 Ω
Integrated bias control circuit
OIP3 of 40 dBm at 70 MHz
P1dB of 20.4 dBm at 70 MHz
Noise figure of 2.5 dB at 70 MHz
Temperature and power supply stable
Single 5 V power supply

FUNCTIONAL BLOCK DIAGRAM

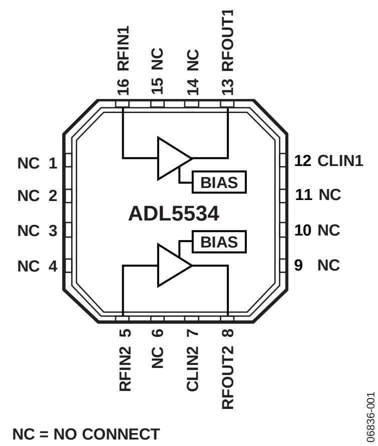

Figure 1.

GENERAL DESCRIPTION

The ADL5534 contains two broadband, fixed-gain, linear amplifiers and operates at frequencies up to 500 MHz. The device can be used in a wide variety of equipment, including cellular, satellite, broadband, and instrumentation equipment.

The ADL5534 has a fixed gain of 20 dB, which is stable over frequency, temperature, power supply, and from device-to-device. The amplifiers are single-ended and internally matched to 50 Ω. Only input/output ac-coupling capacitors, power supply decoupling capacitors, and an external bias inductor are required for operation of each amplifier.

The ADL5534 is fabricated on a GaAs HBT process. The device is packaged in a 16-lead 5 mm × 5 mm LFCSP that uses an exposed paddle for excellent thermal impedance. The ADL5534 consumes 98 mA of current per amplifier on a single 5 V supply, and is fully specified for operation from −40°C to +85°C.

A similar amplifier, ADL5531 (available from Analog Devices, Inc.) is the 20 dB gain single-channel version. Fully populated evaluation boards for both the ADL5531 and ADL5534 are available.

Rev. B **Document Feedback**

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Updated Outline Dimensions ... 16
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11/13—Rev. 0 to Rev. A

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Added Figure 15, Renumbered Sequentially ... 9
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

6/08—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		20		500	MHz
Gain (S21)	190 MHz		20.4		dB
Input Return Loss (S11)	190 MHz		−18.0		dB
Output Return Loss (S22)	190 MHz		−29.0		dB
Reverse Isolation (S12)	190 MHz		−23.0		dB
FREQUENCY = 70 MHz					
Gain			21.0		dB
vs. Frequency	±5 MHz		±0.04		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.20		dB
vs. Supply	4.75 V to 5.25 V		±0.20		dB
Output 1 dB Compression Point			20.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		40.0		dBm
Noise Figure			2.5		dB
Device-to-Device Isolation	Measured at output with input applied to alternate device		−46.0		dB
FREQUENCY = 190 MHz					
Gain		19.5	20.4	21	dB
vs. Frequency	±50 MHz		±0.15		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.20		dB
vs. Supply	4.75 V to 5.25 V		±0.17		dB
Output 1 dB Compression Point			20.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		39.0		dBm
Noise Figure			2.7		dB
Device-to-Device Isolation	Measured at output with input applied to an alternate device		−38.0		dB
FREQUENCY = 380 MHz					
Gain		19.0	19.8	20.5	dB
vs. Frequency	±50 MHz		±0.18		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.22		dB
vs. Supply	4.75 V to 5.25 V		±0.16		dB
Output 1 dB Compression Point			20.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		36.0		dBm
Noise Figure			3.0		dB
Device-to-Device Isolation	Measured at output with input applied to an alternate device		−34.0		dB
POWER INTERFACE	RFOUT1, RFOUT2 pins				
Supply Voltage		4.75	5	5.25	V
Supply Current	Per amplifier		98	110	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±15		mA
Power Dissipation			0.5		W

TYPICAL SCATTERING PARAMETERS

VPOS = 5 V and T_A = 25°C; the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

	S11		S21		S12		S22	
Freq. (MHz)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
20	−22.72	−102.04	21.79	174.78	−24.08	5.82	−18.56	−42.21
50	−20.40	−138.34	21.07	171.81	−23.40	6.92	−21.33	−71.17
100	−19.83	−160.87	20.66	169.90	−23.11	7.81	−25.56	−90.45
150	−19.95	−170.03	20.51	167.16	−23.01	9.36	−27.64	−95.94
200	−20.29	−174.24	20.39	164.06	−22.93	11.42	−27.78	−94.45
250	−20.72	−176.35	20.27	160.68	−22.85	13.45	−26.69	−91.22
300	−20.93	−175.04	20.16	157.31	−22.77	15.66	−24.58	−89.94
350	−21.06	−174.10	20.01	153.74	−22.69	17.74	−22.78	−90.89
400	−21.43	−171.87	19.85	150.30	−22.61	20.07	−20.76	−91.14
450	−21.58	−168.25	19.68	146.82	−22.51	22.24	−18.97	−92.39
500	−21.75	−163.79	19.45	142.72	−22.36	24.88	−17.10	−92.91

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage on RFOUT1, RFOUT2	5.5 V
Input Power on RFIN1, RFIN2	10 dBm
Internal Power Dissipation (Paddle Soldered)	900 mW
θ_{JA} (Junction-to-Air)	54°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

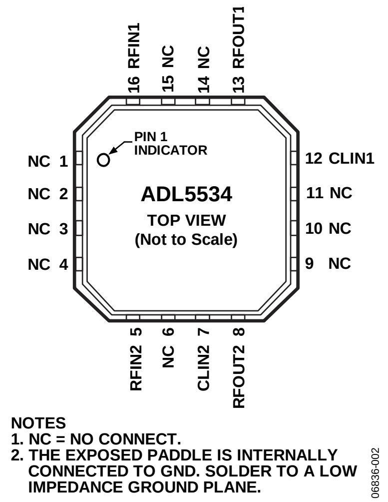

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 4, 6, 9, 10, 11, 14, 15	NC	No Connect.
5, 16	RFIN2, RFIN1	RF Input. Requires a dc blocking capacitor. Use a 10 nF capacitor for normal operation.
7, 12	CLIN2, CLIN1	A 1 nF capacitor connected from Pin 7 to ground and Pin12 to ground provides decoupling for the on-board linearizer.
8, 13	RFOUT2, RFOUT1	RF Output and Bias. DC bias is provided to this pin through an inductor. A 470 nH inductor is recommended for normal operation. The RF path requires a dc blocking capacitor. Use a 10 nF capacitor for normal operation.
	Exposed Paddle	GND. Solder this paddle to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

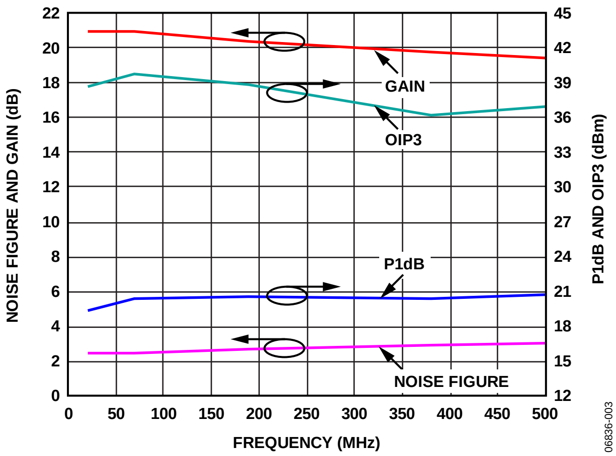

Figure 3. Noise Figure, Gain, P1dB, and OIP3 vs. Frequency

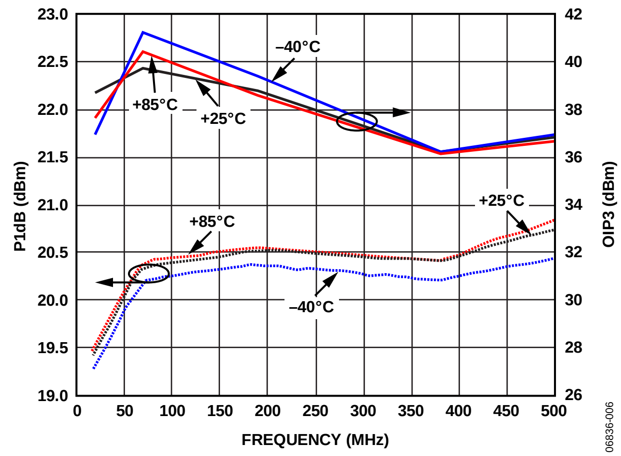

Figure 6. P1dB and OIP3 vs. Frequency and Temperature

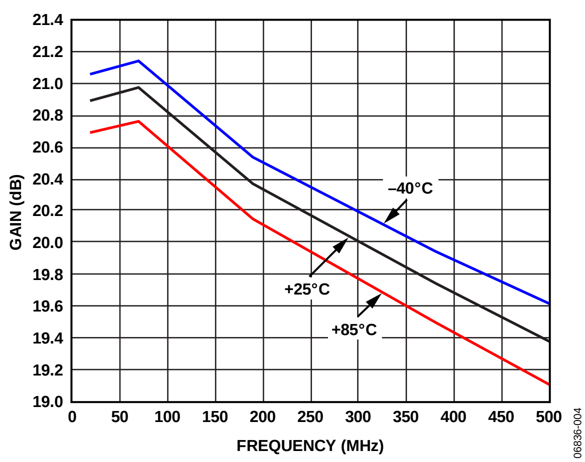

Figure 4. Gain vs. Frequency and Temperature

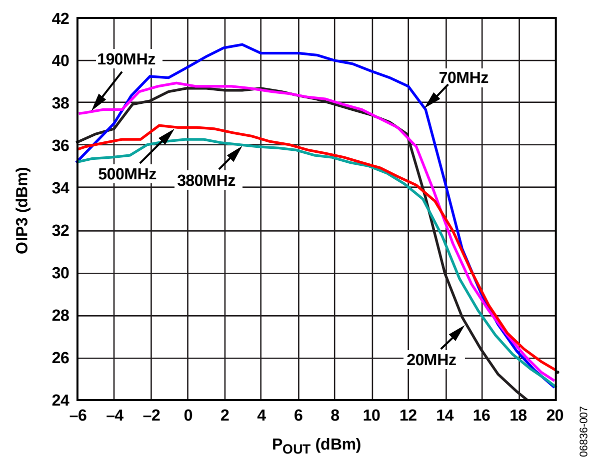

Figure 7. OIP3 vs. Output Power and Frequency

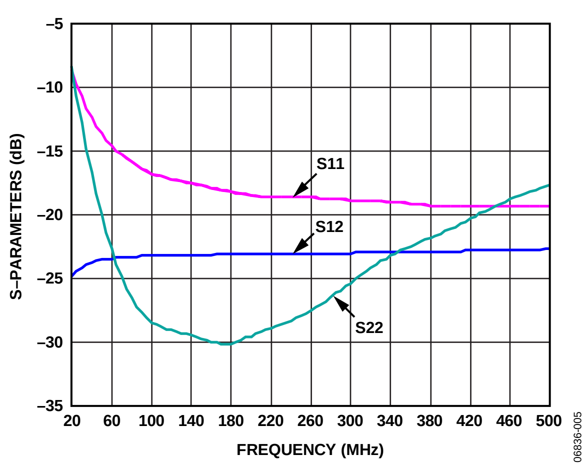

Figure 5. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

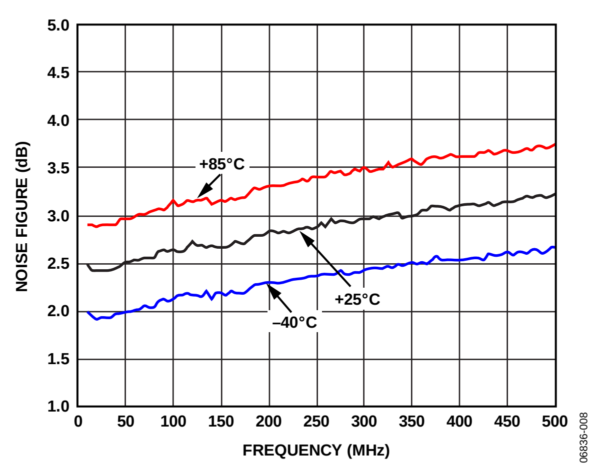

Figure 8. Noise Figure vs. Frequency and Temperature

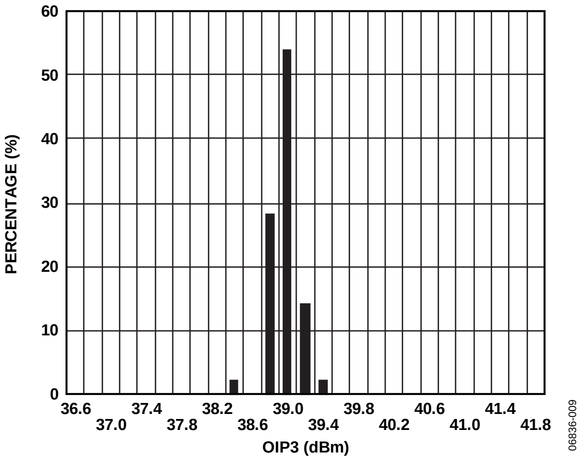

Figure 9. OIP3 Distribution at 190 MHz

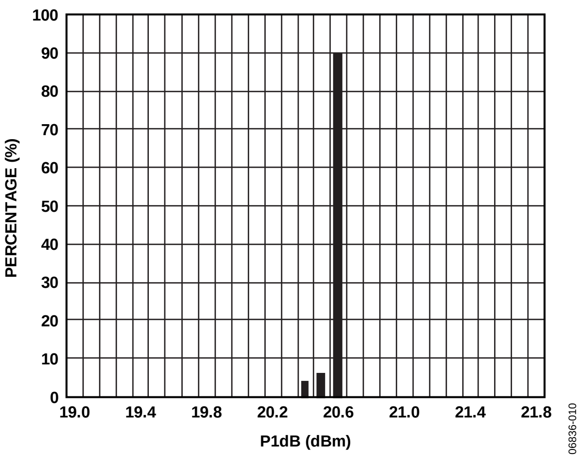

Figure 10. P1dB Distribution at 190 MHz

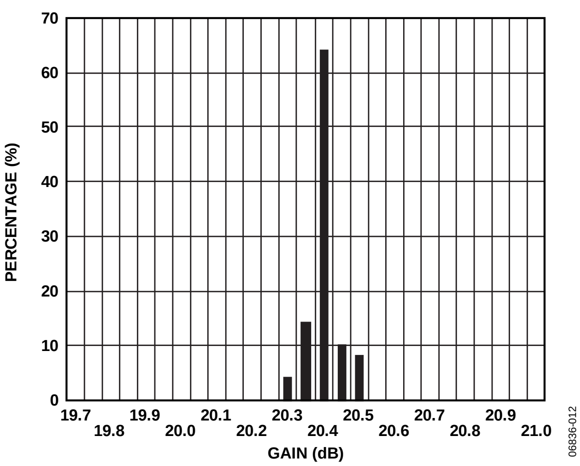

Figure 11. Gain Distribution at 190 MHz

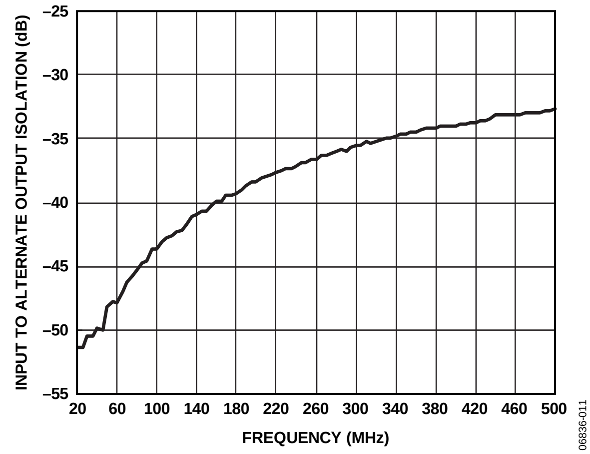

Figure 12. Device-to-Device Isolation vs. Frequency

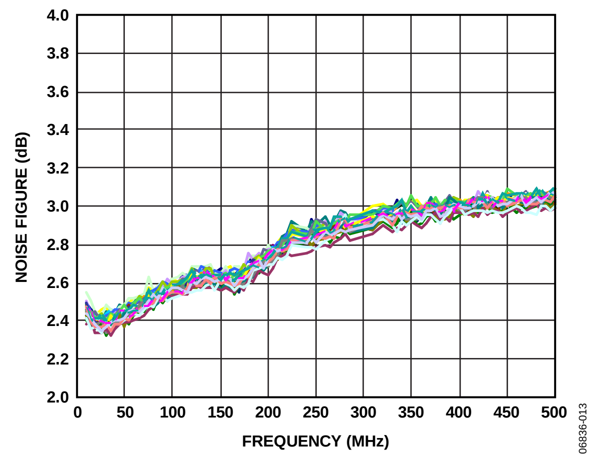

Figure 13. Noise Figure vs. Frequency at 25°C, Multiple Devices Shown

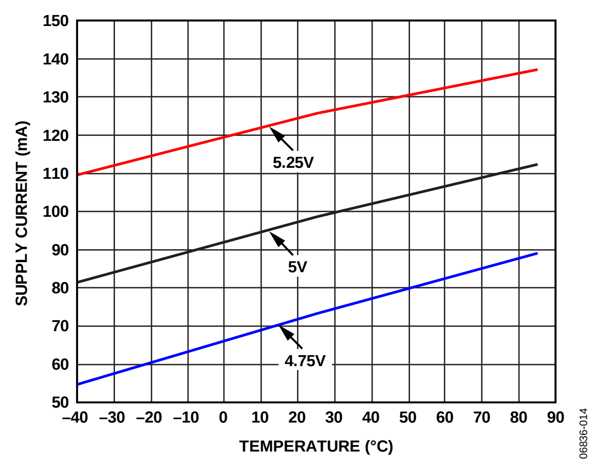

Figure 14. Supply Current vs. Temperature and Supply Voltage

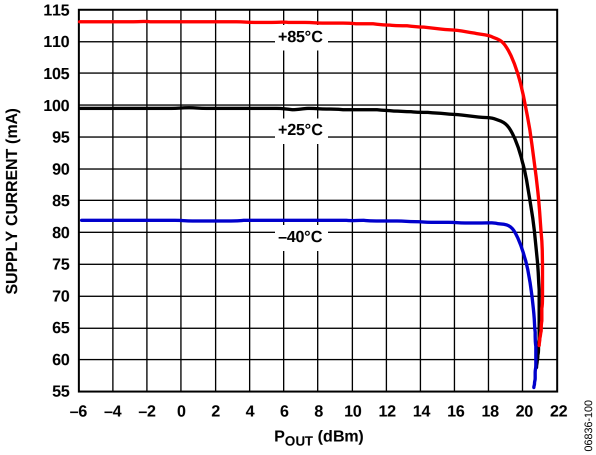

Figure 15. Supply Current vs. P_{OUT} and Temperature V Supply = 5 V

BASIC CONNECTIONS

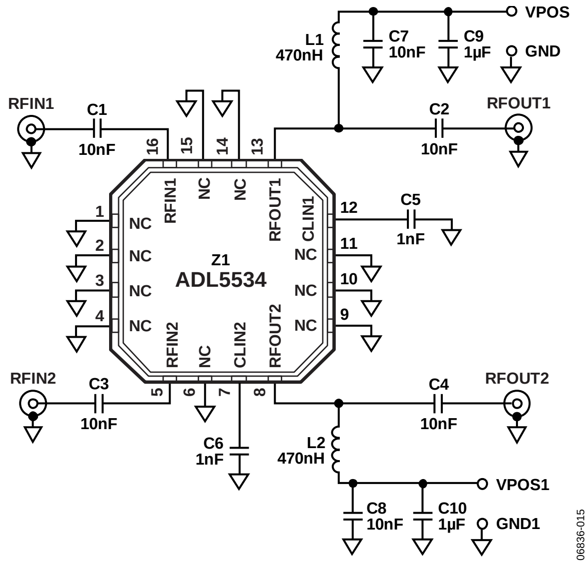

Figure 16. Basic Connections

Table 5. Recommended Components for Basic Connections

Frequency	C1, C2, C3, C4, C7, C8	L1, L2	C5, C6	C9, C10
20 MHz to 500 MHz	10 nF	470 nH	1 nF	1 µF

The basic connections for operating the ADL5534 are shown in Figure 16. Recommended components are listed in Table 5. The inputs and outputs should be ac-coupled with appropriately sized capacitors (device characterization was performed with 10 nF capacitors). DC bias is provided to the amplifier via the L1 and L2 inductors connected to the RFOUT1 and RFOUT2 pins. The recommended inductors for L1 and L2 are Coilcraft, 1008CS-471XJLC or equivalent. The bias voltage should be decoupled using 10 nF and 1 µF capacitors. A bias voltage of 5 V is required.

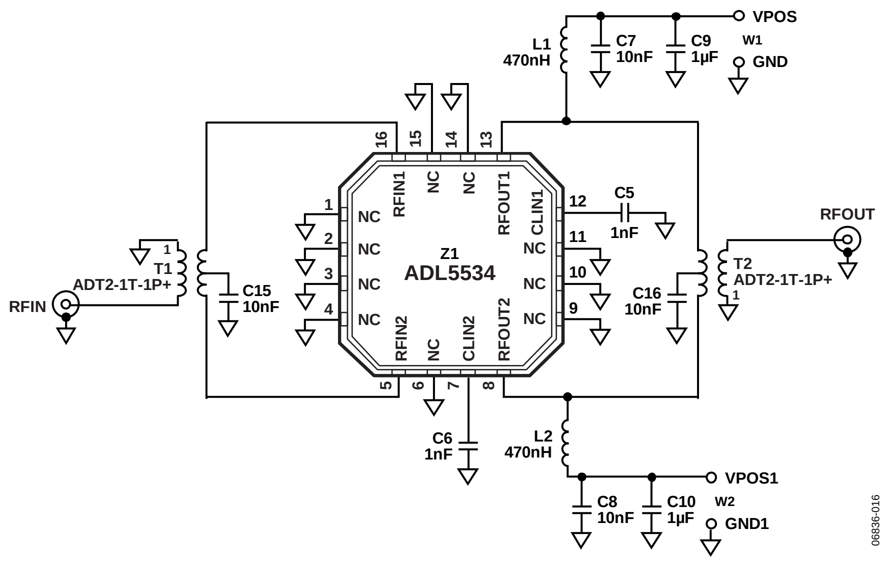

Figure 17. Connections for Operating as a Balanced Amplifier

USING BALUNS TO COMBINE BOTH AMPLIFIERS INTO A SINGLE AMPLIFIER

The ADL5534 is ideal for use in a balanced amplifier configuration. To accomplish this, flux-coupled RF transformers with a 2:1 impedance ratio can be used for wide band operation. Alternatively, a balun can be constructed using lumped element components for operation over a narrow frequency range. Figure 17 shows the necessary connections for configuring the ADL5534 for operation as a balanced amplifier. Figure 18 shows the performance of the ADL5534 operating in a balanced configuration.

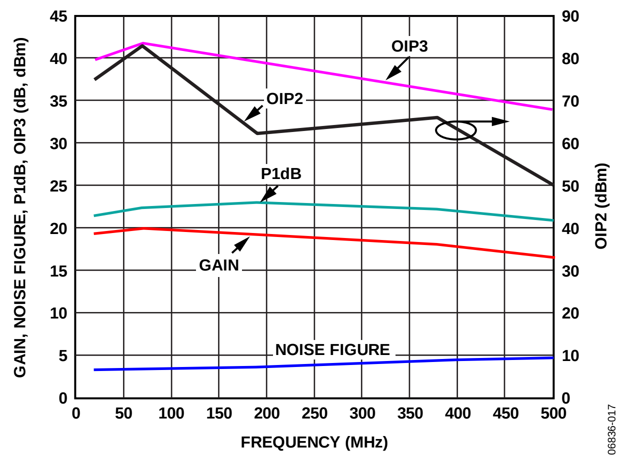

Figure 18. Performance of the ADL5534 Operating in Balanced Configuration

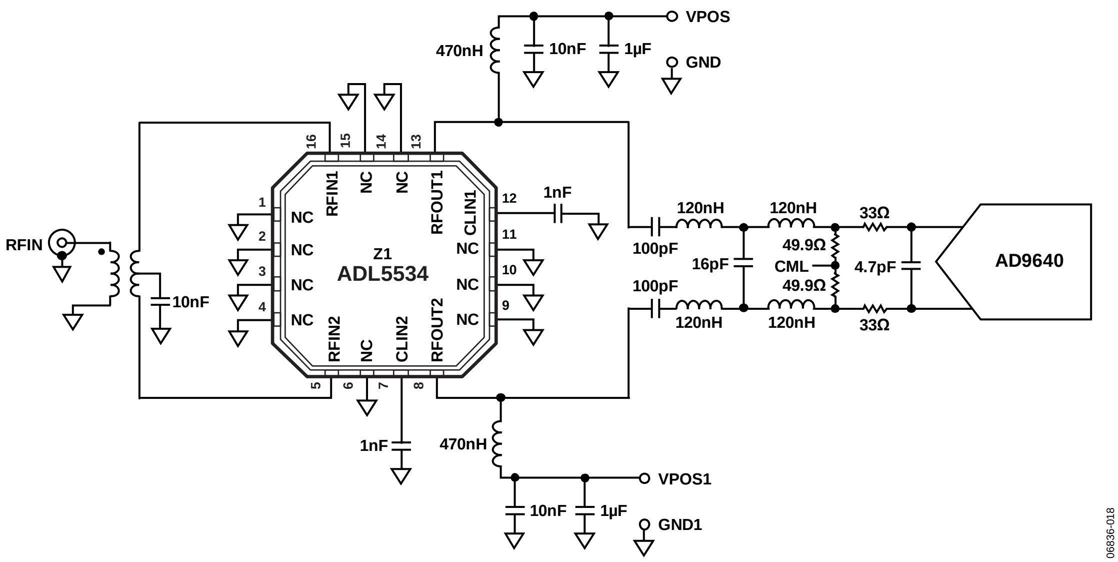

Figure 19. Narrow-Band IF Sampling Solution for Unbuffered ADC

ADC DRIVING APPLICATION

The ADL5534 is a high linearity, fixed gain IF amplifier suitable for use as an ADC driver. The ADL5534 has a differential input and output impedance of 100 Ω. A flux-coupled RF transformer with a 2:1 impedance ratio was used to perform the single-ended-to-differential conversion at the input of the ADL5534. The interface between the ADL5534 and the AD9640 is a third-order low pass filter presenting a 100 Ω differential impedance to the source and load. The ADL5534 must be ac-coupled to prevent dc bias from entering the inputs of the ADC. Capacitors of 100 pF were chosen to reduce any low frequency noise coming from the ADL5534 and provide dc blocking. The measured results for this interface shows 0.5 dB insertion loss for a 20 MHz bandwidth centered around 92 MHz. The wideband response for the interface is shown in Figure 20. The single-tone results in Figure 21 show an SNR of 69.3 dB and an SFDR of 82 dBc. The two-tone results in Figure 22 show an IMD3 of –80.5 dBc and an SFDR of 78 dBc.

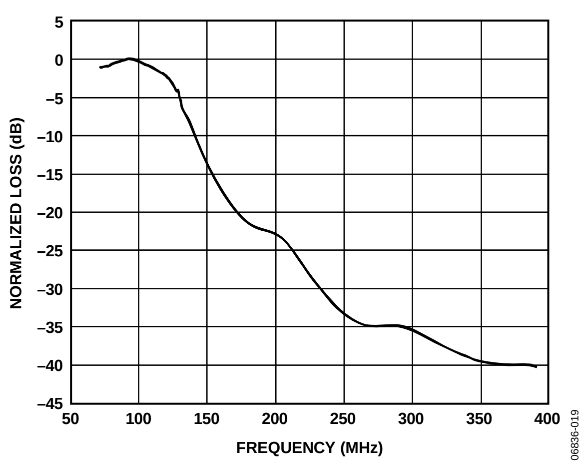

Figure 20. Measured Frequency Response of ADC interface in Figure 19

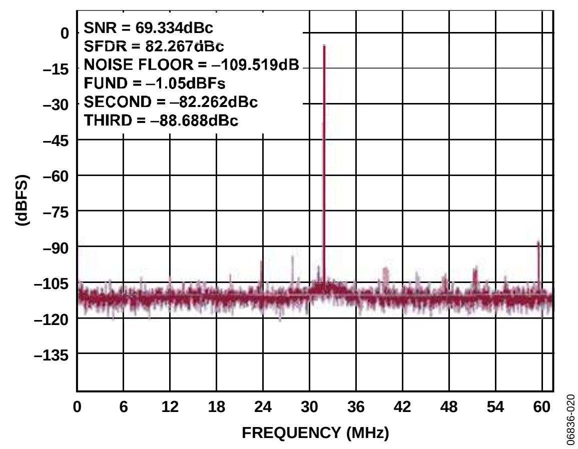

Figure 21. Measured Single-Tone Performance of the Circuit in Figure 19

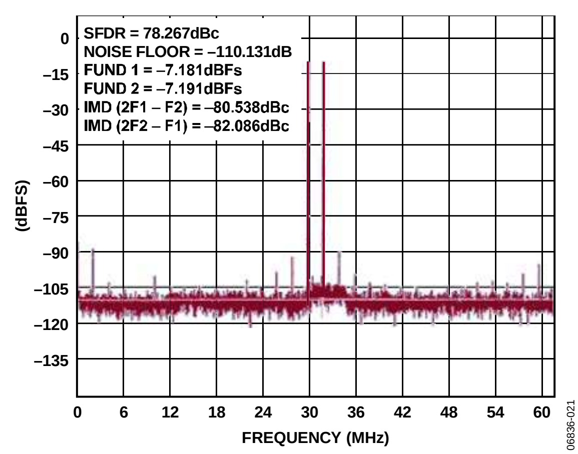

Figure 22. Measured Two-Tone Performance of the Circuit in Figure 19

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 23 shows the recommended land pattern for ADL5534. To minimize thermal impedance, the exposed paddle on the package underside should be soldered down to a ground plane. If multiple ground layers exist, they should be stitched together using vias. Pin 1 to Pin 4, Pin 6, Pin 9 to Pin 11, and Pin 14 to Pin 15 can be left unconnected, or can be connected to ground. Connecting these pins to ground improves device-to-device isolation and slightly enhances thermal impedance. For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

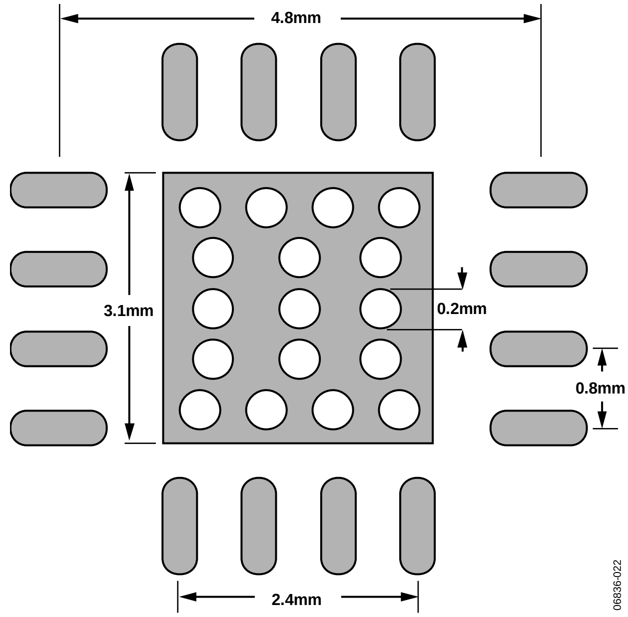

Figure 23. Recommended Land Pattern

EVALUATION BOARD

Figure 24 shows the schematic for the ADL5534 evaluation board. The board is powered by a single 5 V supply. The components used on the board are listed in Table 6. Transformers (T1 and T2) are provided so the ADL5534 can be configured as a balanced amplifier. Applying 5 V to VPOS biases the amplifier corresponding to RFIN1 and RFOUT1. Applying 5 V to VPOS1 biases the amplifier corresponding to RFIN2 and RFOUT2. To bias both amplifiers from a single supply, connect 5 V to VPOS or VPOS1 and attach a jumper across W3.

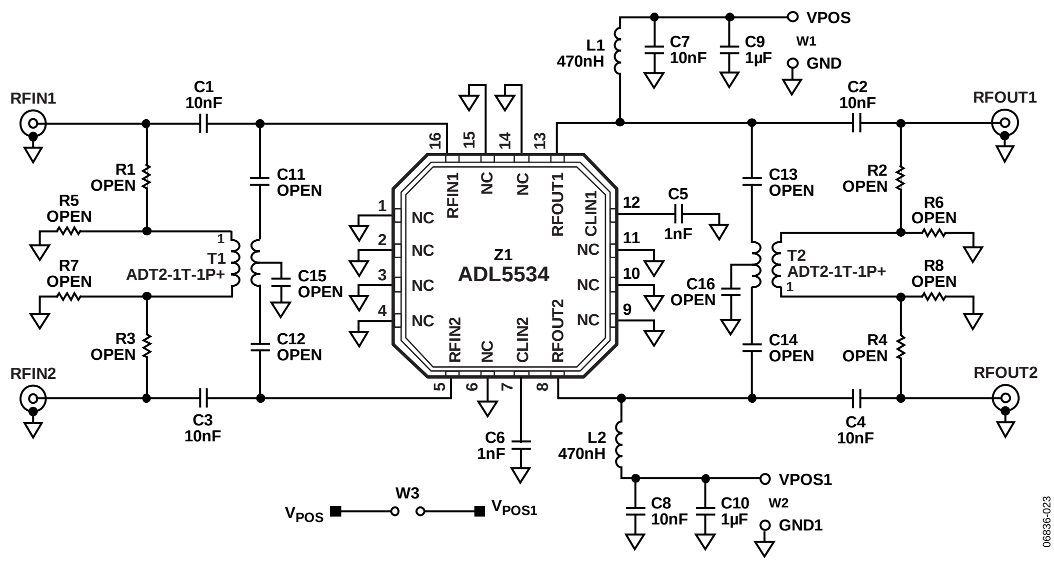

Figure 24. Evaluation Board Schematic

Table 6. Evaluation Board Configuration Options

Component	Description	Default Condition
C1, C2, C3, C4	AC coupling capacitors	10 nF, Size 0402
C5, C6	Provides decoupling for the on-board linearizer	1 nF, Size 0603
C11, C12, C13, C14, C15, C16	Optional components used for configuring ADL5534 as a balanced amplifier	Open, Size 0402
C9, C10	Power-supply decoupling capacitors	1 µF, Size 0603
C7, C8	Power-supply decoupling capacitors	10 nF, Size 0603
R1, R2, R3, R4, R5, R6, R7, R8	Optional components used for configuring ADL5534 as a balanced amplifier	Open, Size 0603
T1, T2	T1 and T2 are 50 Ω to100 Ω impedance transformers used to configure the ADL5534 as a balanced amplifier; T1 and T2 are used to present a 100 Ω differential impedance to the ADL5534	Installed (Mini-Circuits® ADT2-1T-1P+)
L1, L2	DC bias inductor	470 nH, Size 1008
VPOS, GND, VPOS1, GND1	Clip-on terminals for power supply	VPOS, VPOS1; red GND, GND1; black
W1, W2	2-pin jumper for connection of ground and supply via cable	W1, W2
W3	2-pin jumper used to connect VPOS to VPOS1	W3

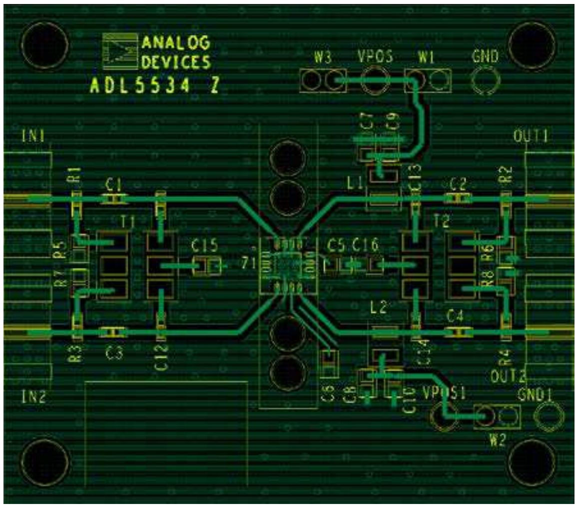

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Figure 25. Evaluation Board Layout (Top)

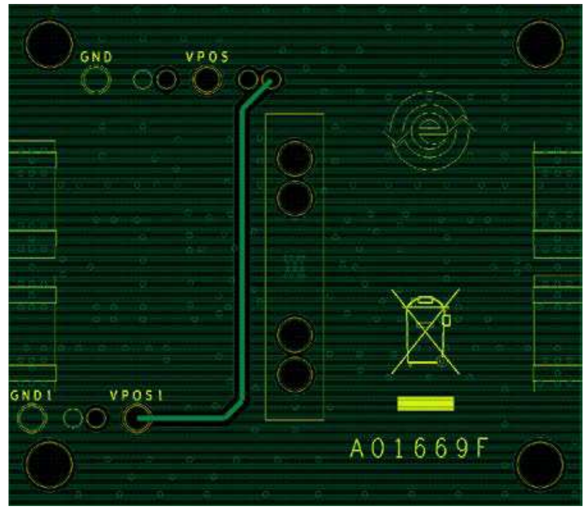

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Figure 26. Evaluation Board Layout (Bottom)

OUTLINE DIMENSIONS

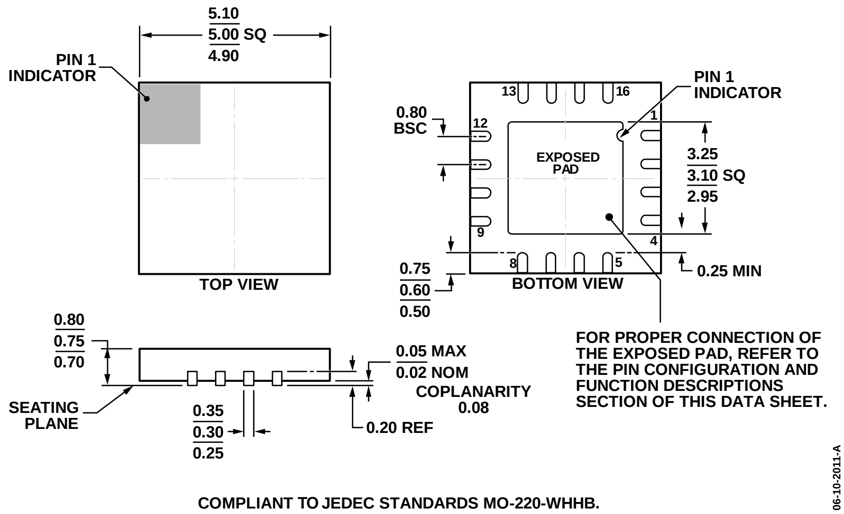

Figure 27. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
CP-16-31
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5534ACPZ-R7	−40°C to +85°C	16-Lead LFCSP_WQ, 7" Tape and Reel	CP-16-31	1500
ADL5534-EVALZ		Evaluation Board		1

[1] Z = RoHS Compliant Part.