

Accutek Microcircuit Corporation

AK63232Z
32,768 x 32 Bit CMOS / BiCMOS
Static Random Access Memory

DESCRIPTION

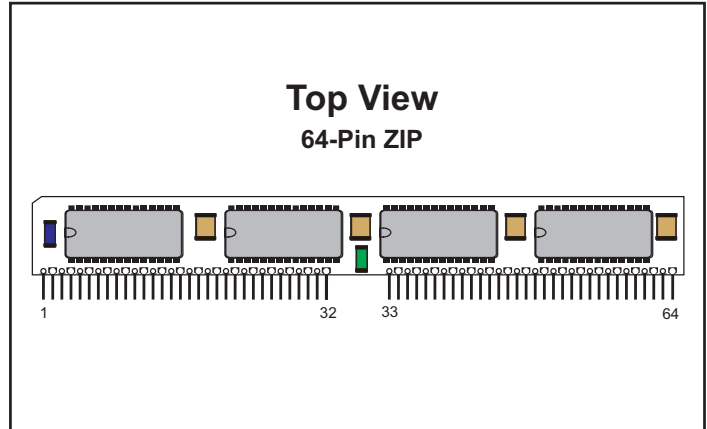
The Accutek AK63232Z SRAM Module consists of fast high performance SRAMs mounted on a low profile, 64 pin ZIP Board. The module utilizes four 28 pin 32K x 8 SRAMs in 300 mil SOJ packages and four decoupling capacitors mounted on the front side of a printed circuit board.

The SRAMs used have common I/O functions and single output enable functions. Also, four separate chip select (CE) connections are used to independently enable the four bytes. The modules can be supplied in a variety of access time values from 8 nSEC to 45 nSEC in CMOS or BiCMOS technology.

The Accutek module is designed to have a maximum seated height of 0.500 inch. The module conforms to JEDEC-standard sizes and pin-out configurations. This, along with use of two pins for module memory density identification, PD₀ and PD₁, minimizes interchangeability and design considerations when changing from one module size to the other in customer applications.

FEATURES

- 32,768 x 32 bit organization
- JEDEC standard 64 pin ZIP format
- Common I/O, single \overline{OE} functions with four separate chip selects (CE)
- Low height, 0.500 inch maximum seated height



- Upward compatible with 64K x 32 (AK63264), 256K x 32 (AK632256), 512K x 32 (AK632512) and 1 Meg x 32 (AK6321024)
- Presence Detect, PD₀ and PD₁ for identifying module density
- Fast Access Times range from 8 nSEC BiCMOS to 45 nSEC CMOS
- TTL compatible inputs and outputs
- Single 5 volt power supply - AK63232Z
- Single 3.3 volt power supply - AK63232Z/3.3
- Operating temperature range in free air, 0°C to 70°C

PIN NOMENCLATURE

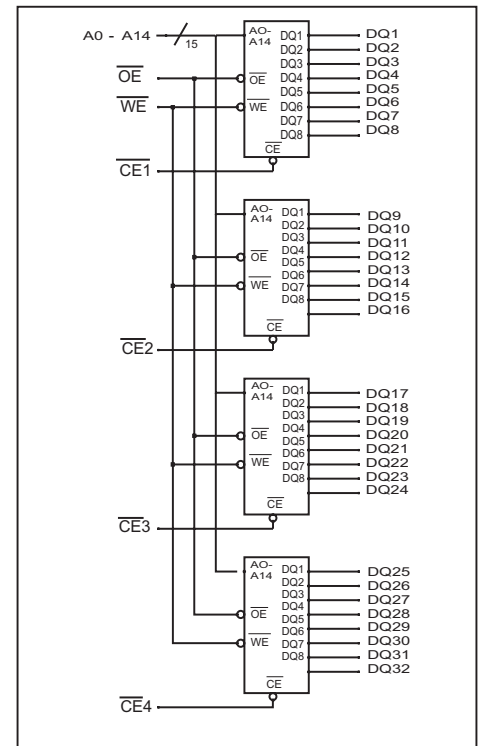
A ₀ - A ₁₄	Address Inputs
\overline{CE}_1 - \overline{CE}_4	Chip Enable
DQ ₁ - DQ ₃₂	Data In/Data Out
\overline{OE}	Output Enable
PD ₀ - PD ₁	Presence Detect
V _{cc}	Power Supply
V _{ss}	Ground
\overline{WE}	Write Enable

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V _{ss}	17	A ₂	33	CE ₄	49	A ₄
2	PD ₀	18	A ₉	34	CE ₃	50	A ₁₁
3	PD ₁	19	DQ ₁₃	35	NC	51	A ₅
4	DQ ₁	20	DQ ₅	36	NC	52	A ₁₂
5	DQ ₉	21	DQ ₁₄	37	OE	53	V _{cc}
6	DQ ₂	22	DQ ₆	38	V _{ss}	54	A ₁₃
7	DQ ₁₀	23	DQ ₁₅	39	DQ ₂₅	55	A ₆
8	DQ ₃	24	DQ ₇	40	DQ ₁₇	56	DQ ₂₁
9	DQ ₁₁	25	DQ ₁₆	41	DQ ₂₆	57	DQ ₂₉
10	DQ ₄	26	DQ ₈	42	DQ ₁₈	58	DQ ₂₂
11	DQ ₁₂	27	V _{ss}	43	DQ ₂₇	59	DQ ₃₀
12	V _{cc}	28	WE	44	DQ ₁₉	60	DQ ₂₃
13	A ₀	29	NC	45	DQ ₂₈	61	DQ ₃₁
14	A ₇	30	A ₁₄	46	DQ ₂₀	62	DQ ₂₄
15	A ₁	31	CE ₂	47	A ₃	63	DQ ₃₂
16	A ₈	32	CE ₁	48	A ₁₀	64	V _{ss}

PD₀ = Open
PD₁ = Open

FUNCTIONAL DIAGRAM



MODULE OPTIONS

Leaded ZIP: AK63232Z

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position 1 2 3 4 5 6 7 8

1 Product

AK = Accuthek Memory

2 Type

4 = Dynamic RAM
5 = CMOS Dynamic RAM
6 = Static RAM

3 Organization/Word Width

1 = by 1 16 = by 16
4 = by 4 32 = by 32
8 = by 8 36 = by 36
9 = by 9

4 Size/Bits Depth

64 = 64K 4096 = 4 MEG
256 = 256K 8192 = 8 MEG
1024 = 1 MEG 16384 = 16 MEG

5 Package Type

G = Single In-Line Package (SIP)
S = Single In-Line Module (SIM)
D = Dual In-Line Package (DIP)
W = .050 inch Pitch Edge Connect
Z = Zig-Zag In-Line Package (ZIP)

6 Special Designation

P = Page Mode
N = Nibble Mode
K = Static Column Mode
W = Write Per Bit Mode
V = Video Ram

7 Separator

- = Commercial 0°C to +70°C
M = Military Equivalent Screened (-55°C to +125°C)
I = Industrial Temperature Tested (-45°C to +85°C)
X = Burned In

8 Speed (first two significant digits)

DRAMS	SRAMS
50 = 50 nS	8 = 8 nS
60 = 60 nS	12 = 12 nS
70 = 70 nS	15 = 15 nS
80 = 80 nS	20 = 20 nS

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

EXAMPLES:

AK63232Z-12

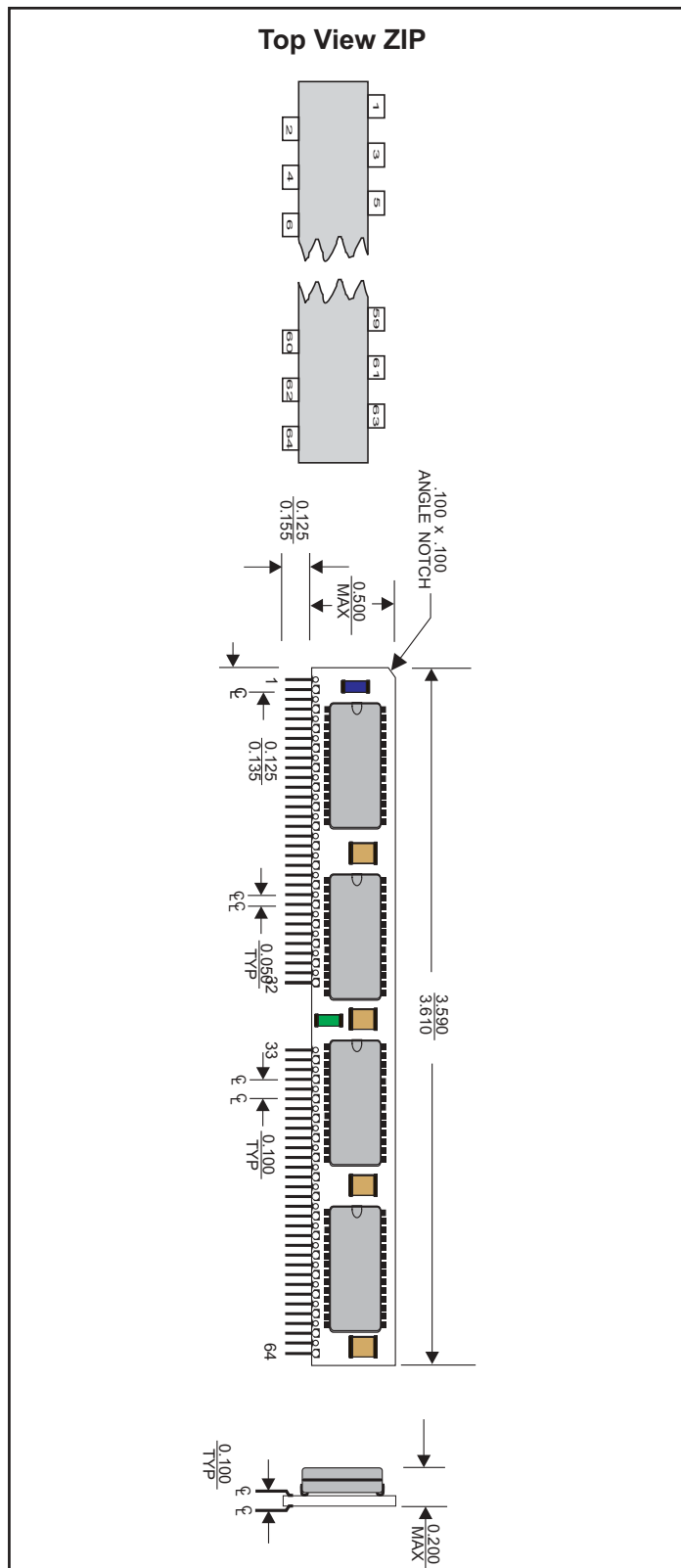
32K x 32, 12 nSEC SRAM ZIP Module



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MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.