AK481024S / AK481024G
1,048,576 x 8 Bit CMOS
Dynamic Random Access Memory

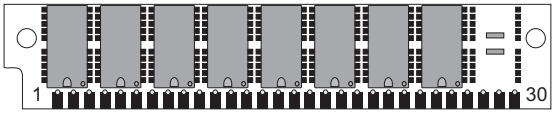
DESCRIPTION

The Accutek AK481024 high density memory module is a random access memory organized in 1 Meg x 8 bit words. The assembly consists of eight standard 1 Meg x 1 DRAMs in plastic leaded chip carriers (SOJ) mounted on the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

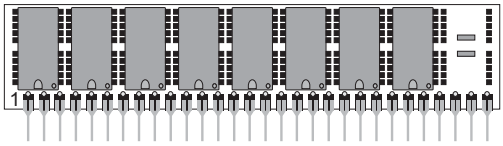
The operation of the AK481024 is identical to eight 1 Meg x 1 DRAMs. The data input is tied to the data output and brought out separately for each device, with common $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable ($\overline{WE}$) signal must always go low before $\overline{CAS}$ in a write cycle, Read-Write and Read-Modify-Write operation is not possible.

Front View

30-Pin SIM



30-Pin SIP



FEATURES

- 1,048,576 x 8 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC standard pinout
- Each device has common D and Q lines with common $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ control
- $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Power
  3.08 Watt Max Active (80 nSEC)
  2.64 Watt Max Active (100 nSEC)
  2.20 Watt Max Active (120 nSEC)
  44 mW Max Standby
- Operating free air temperature 0^0C to 70^0C
- Upward compatible with AK584096 and AK5816384
- Downward compatible with AK48256

PIN NOMENCLATURE

DQ_1 - DQ_8	Data In / Data Out
A_0 - A_9	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
Vcc	5v Supply
Vss	Ground
NC	No Connect

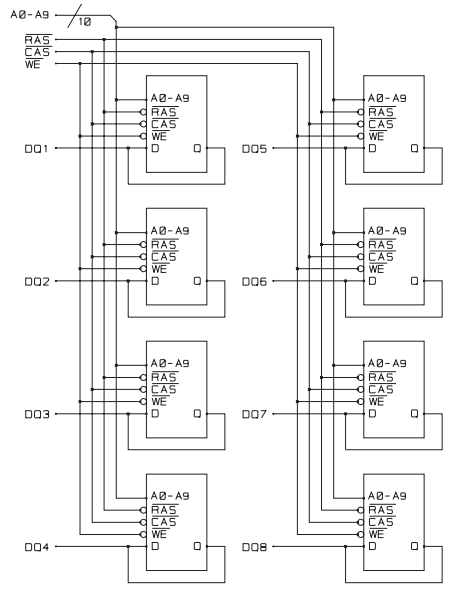
MODULE OPTIONS

Leadless SIM: AK481024S
Leaded SIP: AK481024G

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL
1	Vcc	16	DQ5
2	CAS	17	A8
3	DQ1	18	A9
4	A0	19	NC
5	A1	20	DQ6
6	DQ2	21	WE
7	A2	22	Vss
8	A3	23	DQ7
9	Vss	24	NC
10	DQ3	25	DQ8
11	A4	26	NC
12	A5	27	RAS
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	Vcc

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8

1 Product

AK = Accutek Memory

2 Type

4 = Dynamic RAM
5 = CMOS Dynamic RAM
6 = Static RAM

3 Organization/Word Width

1 = by 1 16 = by 16
4 = by 4 32 = by 32
8 = by 8 36 = by 36
9 = by 9

4 Size/Bits Depth

64 = 64K 4096 = 4 MEG
256 = 256K 8192 = 8 MEG
1024 = 1 MEG 16384 = 16 MEG

5 Package Type

G = Single In-Line Package (SIP)
S = Single In-Line Module (SIM)
D = Dual In-Line Package (DIP)
W = .050 inch Pitch Edge Connect
Z = Zig-Zag In-Line Package (ZIP)

6 Special Designation

P = Page Mode
N = Nibble Mode
K = Static Column Mode
W = Write Per Bit Mode
V = Video Ram

7 Separator

- = Commercial 0^0C to +70^0C
M = Military Equivalent Screened (-55^0C to +125^0C)
I = Industrial Temperature Tested (-45^0C to +85^0C)
X = Burned In

8 Speed (first two significant digits)

DRAMS			SRAMS		
50	=	50 nS	8	=	8 nS
60	=	60 nS	10	=	10 nS
70	=	70 nS	12	=	12 nS
80	=	80 nS	15	=	15 nS

The numbers and coding on this page do not include all variations available but are show as examples of the most widely used variations. Contact Accutek if other information is required.

EXAMPLES:

AK481024SP-80

1 Meg x 8, 80 nSEC DRAM 30 pin SIM Configuration, Page Mode

AK481024GN-70

1 Meg x 8, 70 nSEC Dram 30 pin SIP Configuration, Nibble Mode

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MECHANICAL DIMENSIONS

Inches