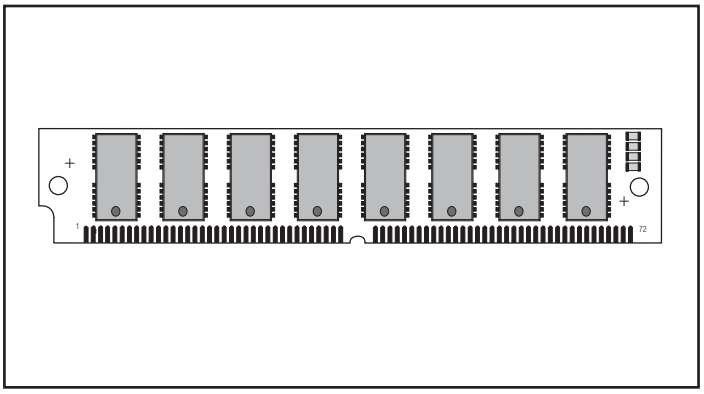
ACCUTEK
MICROCIRCUIT CORPORATION

AK5321024W
1,048,576 Word by 32 Bit CMOS Dynamic Random Access Memory



DESCRIPTION

The Accutek AK5321024W high density memory module is a CMOS Dynamic RAM organized in 1024K x 32 bit words. The module consists of eight standard 1 Meg x 4 DRAMs in plastic SOJ packages. The assembly has eight drams mounted on the front surface of a printed circuit board with a low profile height of only 0.875" in a 72 pin leadless SIM configuration. This configuration allows socket-mounting of large quantities of memory in applications where high density and ease of inserting additional memory are important.

The operation of the AK5321024W is identical to eight 1 Meg x 4 DRAMs. There are four $\overline{CAS}$ lines and two $\overline{RAS}$ lines. Independent byte control is accomplished by four $\overline{CAS}$ lines. Each separate $\overline{CAS}$ line controls two of the 1 Meg x 4 DRAMs to form an 8 bit byte. The bank of 32 bits is controlled by the two $\overline{RAS}$ lines. A sixteen bit data path can be produced by connecting DQ_0 to DQ_{16}, DQ_1 to DQ_{17}, etc. and alternately strobing $\overline{RAS_0}$ with $\overline{RAS_2}$.

FEATURES

- 1,048,576 x 32 bit organization
- Low profile board height of 0.875 inch
- 72 pad Single In-Line Module
- Multiple $\overline{CAS}$ and $\overline{RAS}$ lines allow x16 or x32 bit widths
- Power
  5.28 Watt Max Active (60nS)
  4.40 Watt Max Active (70 nS)
  44 mW Max Standby
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only or hidden refresh
- Single 5 Volt Power Supply
- 1024 Refresh Cycles, 16 mSEC
- Available in Fast Page Mode and EDO
- Available in leadless SIM or leaded ZIP versions
- Downward compatible with AK532512 and AK532256
- Upward compatible with AK5322048, AK5324096 and AK5328192
- Operating free air temperature 0^0C to 70^0C

ADDITIONAL OPTIONS AVAILABLE

- 256K x 32 version, AK532256
- 512K x 32 version, AK532512
- 2 Meg x 32 version, AK5322048
- 4 Meg x 32 version, AK5324096
- 8 Meg x 32 version, AK5328192

PIN NOMENCLATURE

A_0 - A_9	Address Inputs
DQ_0 - DQ_{31}	Data In/Data Out
$\overline{CAS_0}$ - $\overline{CAS_3}$	Column Address Strobe
$\overline{RAS_0}$ & $\overline{RAS_2}$	Row Address Strobe
$\overline{WE}$	Write Enable
PD_1 - PD_4	Presence Detect
Vcc	5v Supply
Vss	Ground
NC	No Connect

MODULE OPTIONS

Leadless SIM: AK5321024W
Leaded ZIP: AK5321024Z

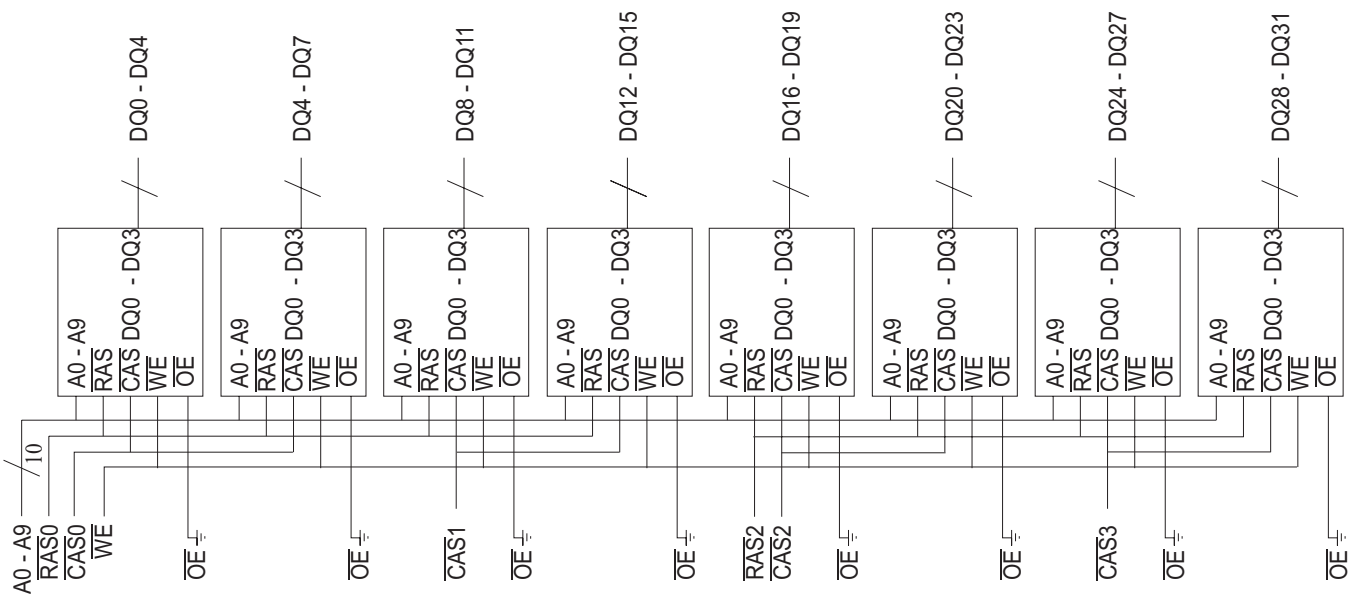
PIN ASSIGNMENT

Pin #	Symbol	Pin #	Symbol	Pin #	Symbol	Pin #	Symbol
1	Vss	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	Vss	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	Vcc	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	46	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	Vss

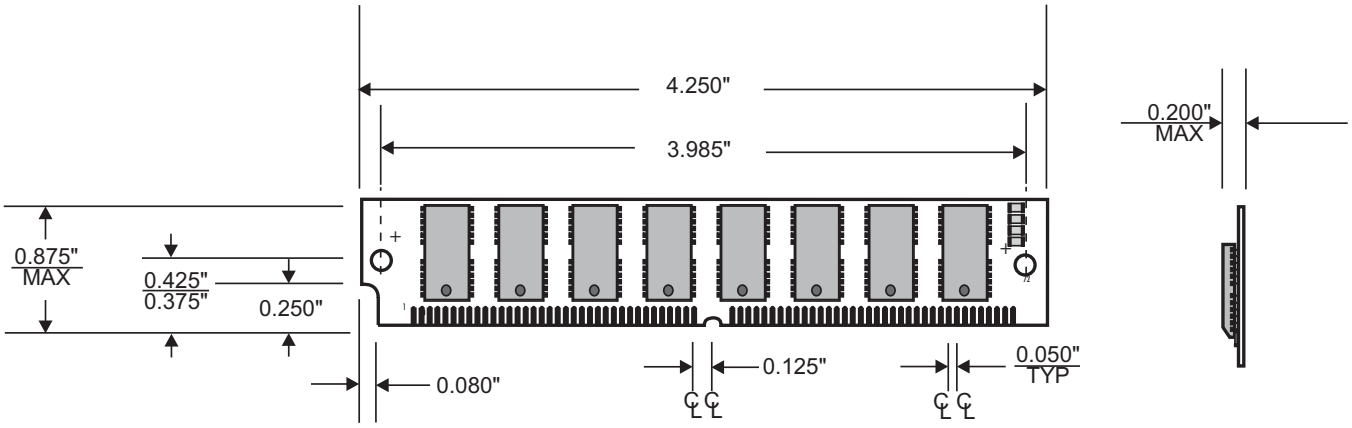
Presence Detect

	-60	-70
PD1	Vss	Vss
PD2	Vss	Vss
PD3	NC	Vss
PD4	NC	NC

FUNCTIONAL DIAGRAM



MECHANICAL DIMENSIONS



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