AK9844A

4Kbit EEPROM with 4ch 8bit D/A Converter

General Description

The AK9844A includes 4 channel, 8-bit D/A converters with on-chip output buffer amps and it is capable to store the input digital data of each D/A converter by on-chip non-volatile CMOS EEPROM. The AK9844A is optimally designed for various circuit adjustments for consumer and industrial equipments and it is ideally suited for replacing mechanical trimmers.

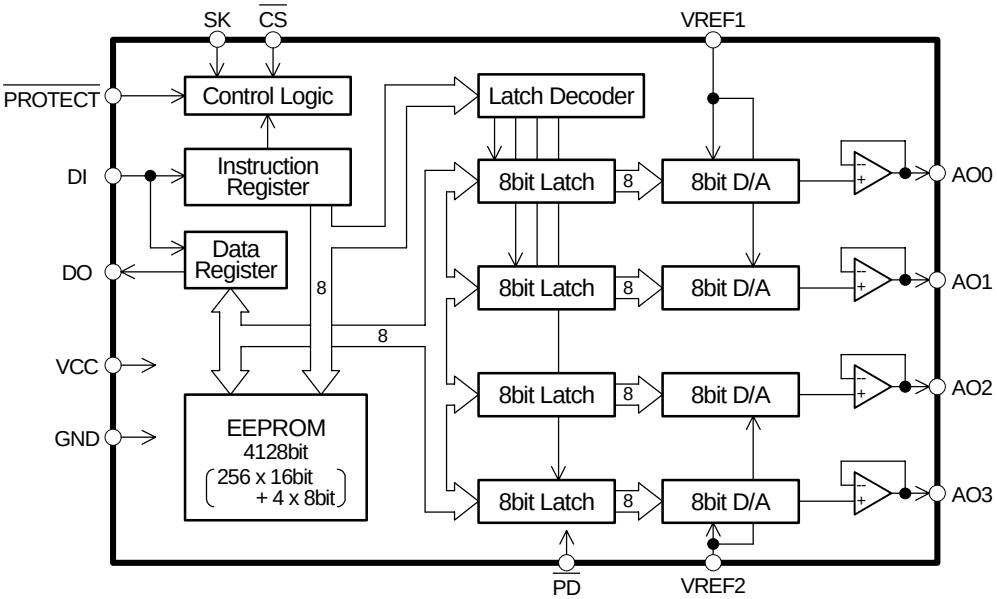
Features

☐ EEPROM section
- ・4 word x 8-bit organization (Dedicated for DAC data)
- ・256 word x 16-bit organization (General purpose memory)
- ・Serial data interface
- ・Sequential register read
- ・Automatic write cycle
- ・100K write cycles
- ・10 year data retention

☐ D/A section
- ・4 channels
- ・Resolution : 8-bits
- ・Differential Non-Linearity : ±1.0 LSB
- ・Linearity Error : ±1.5 LSB
- ・Output Voltage Range : GND to VCC

☐ AUTO READ Function

☐ Power down mode



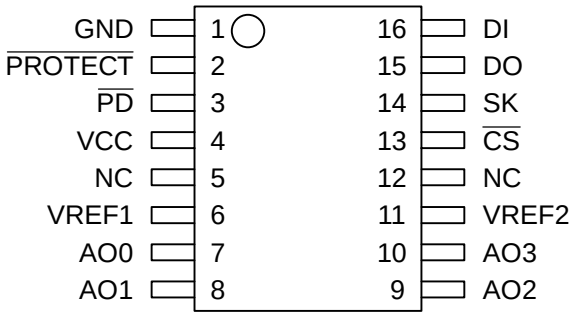
Block Diagram

■ Ordering Guide

AK9844AV -40°C to +85°C 16-pin TSSOP

■ Pin Layout

AK9844AV



16pin TSSOP

■ Pin Description

No.	Pin Name	I/O	Function
1	GND	-	Ground Pin, 0V
2	PROTECT	I	Protect Pin "L" : Programming to the D/A Section of EEPROM is disabled. "H" : Normal operation
3	PD	I	Power-down Pin "L" : Power down mode "H" : Normal mode
4	VCC	-	Power Supply
6	VREF1	I	Voltage Reference Input1 The analog output ranges of the AO0 and the AO1 are set by the VREF1 pin.
7 8 9 10	AO0 AO1 AO2 AO3	O	Analog Output Pins (8-bit D/A outputs)
11	VREF2	I	Voltage Reference Input1 The analog output ranges of the AO2 and the AO3 are set by the VREF2 pin.
13	CS	I	Chip Select Pin (Schmitt-trigger input)
14	SK	I	Serial Clock Pin (Schmitt-trigger input)
15	DO	O	Serial Data Output Pin
16	DI	I	Serial Data Input Pin
5, 12	NC	-	Not Connected

Functional Description

The AK9844A includes the EEPROM section and the D/A converter section which consists of 4 channel, 8bit D/A converters with output buffer amps. The EEPROM section is divided into memory block and DAC register block. The capacity of the memory block is 4096bits which are organized into 256 registers of 16bits each. The DAC digital input data for D/A converters are stored in the DAC register block which is organized into 4 registers of 8bits each. The address for the memory block is "000000000" to "011111111". The address for the DAC register is "100000000" to "100000011".
The configuration of the EEPROM section is showed on figure.1.
The AK9844A can connect to the serial communication port of popular one chip microcontrollers directly (3 line negative clock synchronous interface). At write operation, the AK9844A takes in the write data from the DI pin to a register synchronously with rising edge of the SK pin. At read operation, the AK9844A takes out the read data from a register to the DO pin synchronously with falling edge of the SK pin.
The AK9844A has 6 instructions such as READ, WRITE, WREN, WRDS, PDEN and PDDS. The each instruction is organized by op-code block(8bits), address block(8bits), and data(8bits x 2). The output of DAC is set by storing the DAC digital input data in the DAC register block.
The DO pin is high impedance except that the DO pin outputs the read data and the status signal.

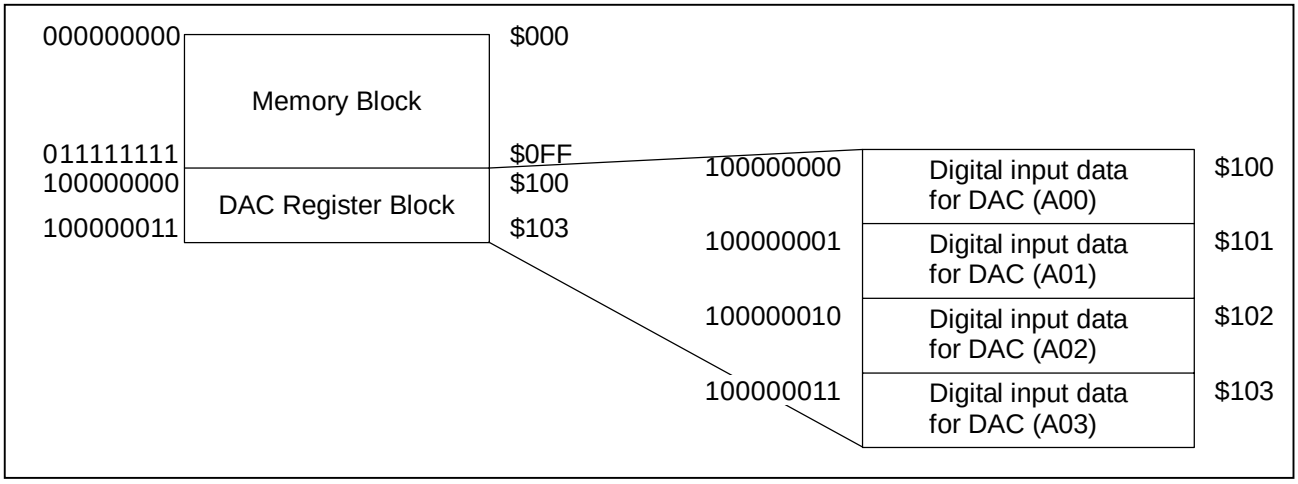


Figure 1. Configuration of the EEPROM section

■ Data Protection

To protect against accidental data disturb, the AK9844A has programming enable state and programming disable state. In programming disable state, the programming operation is not executed.

When VCC is applied to the AK9844A, the AK9844A is powered up in the programming disable mode. The programming instruction should be preceded by the WREN instruction. Once the WREN instruction is executed, the programming state remains enabled until the WRDS instruction is executed or VCC is removed from the device. Execution of the READ instruction is independent of both WREN and WRDS instructions.

The AK9844A also can prohibit to program into the DAC register block by the control of the $\overline{\text{PROTECT}}$ pin. When the $\overline{\text{PROTECT}}$ pin is "L", the programming into the DAC register block is not executed.

$\overline{\text{PROTECT}}$ pin	$\overline{\text{PROTECT}}$="H"		$\overline{\text{PROTECT}}$="L"	
Programming State	Enable	Disable	Enable	Disable
Memory Block	○	×	○	×
DAC Register Block	○	×	×	×

○: Programming into the block is executed.
×: Programming into the block is not executed.

Table 1. Relation between the programming operation and the $\overline{\text{PROTECT}}$ pin

■ Output of D/A converter

The AK9844A includes 4 channel, 8bit D/A converter. The output voltage ranges for AO0 and AO1 are set by the VREF1 pin and the output voltage ranges for AO2 and AO3 are set by the VREF2 pin. The output voltage can be set by the READ or WRITE instruction.

When the DAC register block is specified in the WRITE instruction, the output voltage for the specified D/A converter is set. When the WRITE instruction is executed in case that the PROTECT pin is "H" and the programming state is enabled, the output voltage for the specified D/A converter is set and the specified address in the DAC register block in EEPROM is written with the data specified in the instruction.

When the WRITE instruction is executed in case that the $\overline{\text{PROTECT}}$ pin is "H" and the programming state is disabled, the output voltage for the specified D/A converter is set and the specified address in the DAC register block in EEPROM is not written with the data specified in the instruction. When the WRITE instruction is executed in case that the $\overline{\text{PROTECT}}$ pin is "L", the output voltage for the specified D/A converter is not set and the specified address in the DAC register block in EEPROM is not written with the data specified in the instruction. The relation between the WRITE instruction and the DAC register block is showed on the Table 2.

When the DAC register block is specified in the READ instruction, the output voltage for the specified D/A converter is set by the data which is stored in the DAC register block in EEPROM, and the DO pin outputs the data in the specified address.

Execution of the READ instruction is independent of the $\overline{\text{PROTECT}}$ pin and the programming state.

$\overline{\text{PROTECT}}$ pin	Programming State	DAC register block (EEPROM section)	Output of DAC (D/A Converter section)
"H"	Enable	The specified address in the DAC register block is written with the data specified in the instruction.	The output voltage for the specified D/A converter is set by the data specified in the instruction.
	Disable	The data in the DAC register section does not change.	
"L"	Enable		The output of the DAC does not change.
	Disable		

Table 2. Relation between the WRITE instruction and the DAC register block

○ AUTO READ Function

When VCC is applied to the AK9844A, the data on EEPROM are read out and loaded at a time to each corresponding D/A (4 channels total) automatically, starting from AO0 to AO3 in ascending order. Then each D/A analog output is settled to pre-determined value.

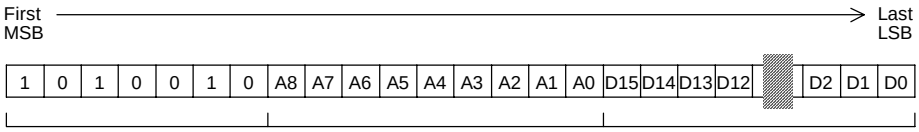
If the $\overline{\text{CS}}$ pin goes to "H" and then goes to "L" after "power-up" with the $\overline{\text{PROTECT}}$ pin and the $\overline{\text{CS}}$ pin left "L", AUTO READ cycle is initiated. After the $\overline{\text{CS}}$ pin goes to "L", 4 channel D/A outputs are settled to pre-determined value within 2ms.

In AUTO READ cycle, the SK pin and the DI pin become "don't care" and the serial data do not output.

If the WREN instruction is executed after AUTO READ cycle is completed, programming into the memory block on the internal EEPROM is enabled.

■ Instruction and Data Format

The instructions consist of op-code(8bits), address(8bits) and data(8bits x 2). The followings are the instruction and data set at WRITE execution.



Op-code

Address

A8	A7	A6	A5	A4	A3	A2	A1	A0	Function	
0	0	0	0	0	0	0	0	0	Memory Block	
0	0	0	0	0	0	0	0	1		
0	1	1	1	1	1	1	1	1		
1	0	0	0	0	0	0	0	0	DAC Register Block	Data for A00
1	0	0	0	0	0	0	0	1		Data for A01
1	0	0	0	0	0	0	1	0		Data for A02
1	0	0	0	0	0	0	1	1		Data for A03

Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D/A Output Voltage
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	≒ (VREF / 256) x1
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	≒ (VREF / 256) x2
1	1	1	1	1	1	1	0	X	X	X	X	X	X	X	X	≒ (VREF / 256) x255
1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	≒ VREF

■ Power Down Function

There are the power down mode and the normal mode in AK9844A. When the AK9844A is in power down mode, the outputs of D/A are "High impedance" and the DAC section is in the standby mode and the power consumption of the AK9844A is decreased.
The power down mode of AK9844A can be determined by the control of the $\overline{PD}$ pin or the PDEN/PDDS instructions.

When the $\overline{PD}$ pin is low level, the AK9844A is in power down mode. When the $\overline{PD}$ pin is high level, the state of the AK9844A can be determined by PDEN/PDDS instructions. When the $\overline{PD}$ pin is High level and the PDEN instruction is executed, the AK9844A becomes the power down mode. Once the AK9844A becomes the power down mode, the AK9844A is in the power down mode until the PDDS instruction is executed. When the PDDS instruction is executed, the AK9844A becomes the normal mode.

If the $\overline{CS}$ pin is High level in the power down mode, the EEPROM section also becomes the standby mode and the AK9844A becomes the lower power-down mode.

The relation between the $\overline{PD}$ pin and the PDEN/PDDS instructions is showed on Table 3. The relation between the power down mode and the DAC/EEPROM section is showed on Table 4. The state at the time AK9844A is powered up is showed on Table 5.

$\overline{PD}$ pin	instruction	mode
Low level	PDEN	power down mode
	PDDS	
High level	PDEN	power down mode
	PDDS	normal mode

Table 3. Relation between the $\overline{PD}$ pin and the PDEN/PDDS instructions

State	DAC section	EEPROM section
normal mode	normal mode	normal mode
power down mode1 $\overline{CS}$ pin="L"	standby mode	normal mode
power down mode2 $\overline{CS}$ pin="H"	standby mode	standby mode

Table 4. Relation between the power down mode and the DAC/EEPROM section

Condition at the time AK9844A is powered on		State
$\overline{PD}$ pin="L"	$\overline{CS}$ pin="L"	power down mode1
	$\overline{CS}$ pin="H"	power down mode2
$\overline{PD}$ pin="H"		normal mode

Table 5. State at the time AK9844A is powered up

■ Precautions for use

1) Output voltage of D/A converter at the time the AK9844A is powered up
At the time the AK9844A is powered up, the D/A converters output "VREF/2" until the instruction or AUTO READ is executed.
2) Power Supply Decoupling
On the boards, decoupling capacitors(0.1μF) between power supply pins(VCC,VREF1,VREF2) and GND should be located as near as possible to the part.

Instruction Set

The AK9844A has 6 instructions such as READ, WRITE, WREN, WRDS, PDEN, PDDS. Each instruction consists of Op-code, address and data. The instruction set is showed on Table 6.
When the instructions are executed consecutively, the CS pin should be brought to high level for a minimum of 250ns(tCS) between consecutive instruction cycle.

Instruction	Op-code		Address	Data	Comments
READ	1010100	A8	A7 A6 A5 A4 A3 A2 A1 A0	D15-D0	Read register
WRITE	1010010	A8	A7 A6 A5 A4 A3 A2 A1 A0	D15-D0	Write register
WREN	1010001	1	X X X X X X X X	X	Write enable
WRDS	1010000	0	X X X X X X X X	X	Write disable
PDEN	1010110	0	X X X X X X X X	X	Power down enable
PDDS	1010011	0	X X X X X X X X	X	Power down disable

X: Don't care

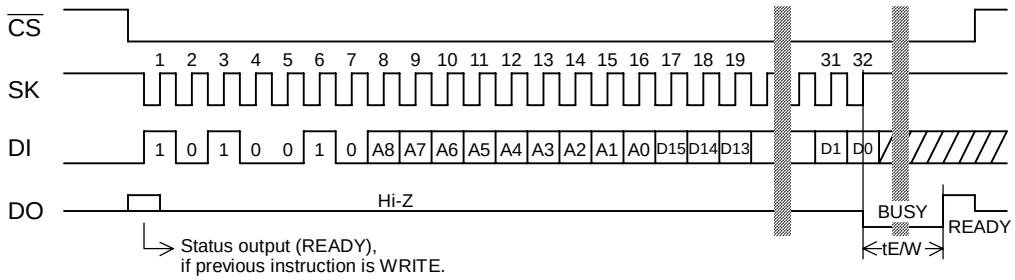
Table 6. Instruction set

■ WRITE

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the 32nd rising edge of SK to read DO in, the AK9844A will be put into the automatic write time-out period. During the automatic write time-out period (Busy status), the CS pin need not be high level.

The DO pin indicates the Ready/Busy status of the EEPROM in AK9844A. After the 32nd rising edge of SK to read DO in, the AK9844A will be put into the automatic write time-out period. When the automatic write time-out period start, the DO pin outputs the Ready/Busy status. When the DO pin outputs low level, the AK9844A is in the automatic write time-out and the next instruction can not be accepted. When the DO pin outputs high level, the automatic write time-out period has ended and the AK9844A is ready for a next instruction.

When the CS pin is changed to high level after confirmation of Ready/Busy signal on the DO pin, the DO pin becomes "Hi-Z". The Ready/Busy signal can be confirmed until the initial 1 bit of the next instruction inputs from the execution of the WRITE instruction.



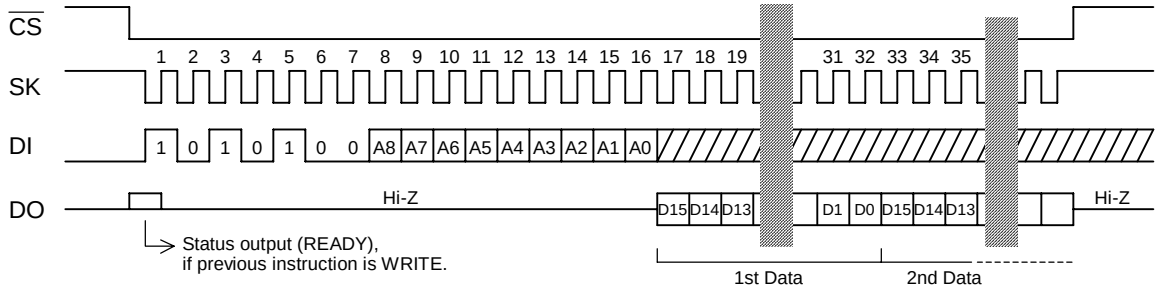
WRITE instruction

■ READ

The read instruction is the only instruction which outputs serial data on the DO pin.
After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial-out shift register. When the 17th falling edge of SK is received, the DO pin will come out of high impedance state and shift out the data from D15 first in descending order which is located at the address specified in the instruction.

○ Sequential register read

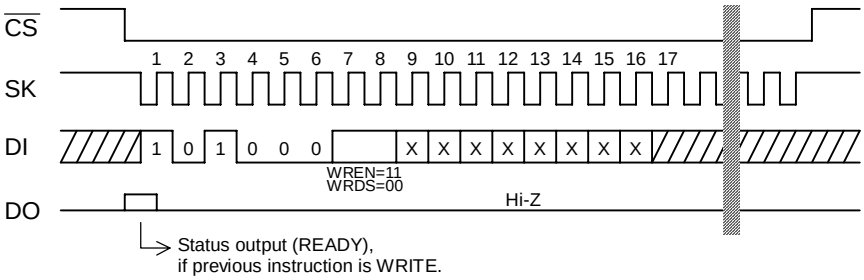
The data in the next address can be read sequentially to provide clock. The memory automatically cycles to the next register after each 16 data bits are clocked out.
The sequential register read function is effective for address: A7~A0. When the highest address is reached ($0FF/$103), the address counter rolls over to address $000/$100 allowing the read cycle to be continued indefinitely.



READ instruction

■ WREN / WRDS

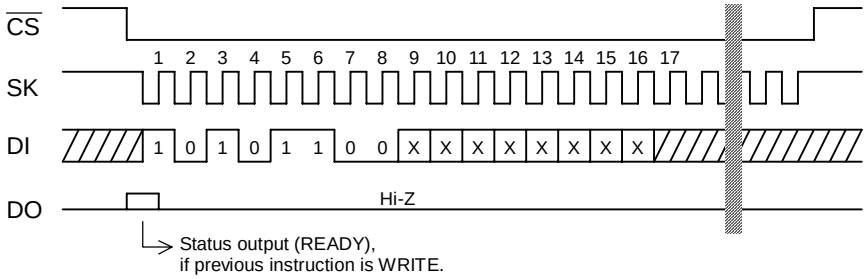
When VCC is applied to the part, it powers up in the programming disable(WRDS) state.
Programming must be preceded by a programming enable(WREN) instruction. Programming remains enabled until a programming disable(WRDS) instruction is executed or VCC is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is not affected by both WREN and WRDS instruction.



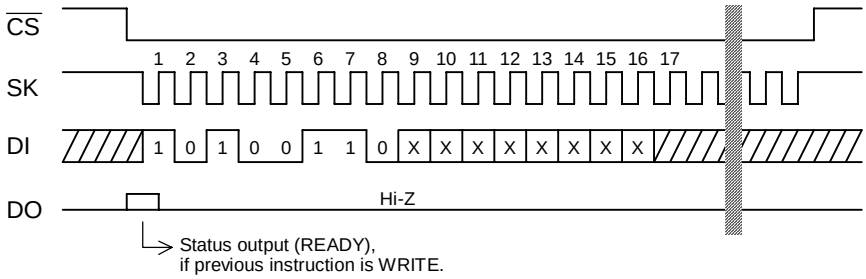
WREN / WRDS instruction

■ PDEN / PDDS

The AK9844A has the power-down mode and the normal mode. When the PDEN instruction is executed while the $\overline{PD}$ pin is high level, the AK9844A becomes the power-down mode. The AK9844A is in the power-down mode until PDDS instruction is executed. After the PDDS instruction is executed, the AK9844A changed to normal mode from power-down mode.
In case that the $\overline{PD}$ pin is low level, the PDEN/PDDS instructions are invalid and are not executed.



PDEN instruction



PDDS instruction

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Power Supply	VCC	Relative to GND	-0.6	+7.0	V
Input Voltage	VIO	Relative to GND	-0.6	VCC+0.6	V
Ambient Temperature	Ta		-40	+85	°C
Storage Temperature	Tst		-65	+150	°C

Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	VCC1	DAC operation	2.7		5.5	V
	VCC2	EEPROM operation	1.8		5.5	V
Analog Output Load Capacitance	AOC				100	pF

Electrical Characteristics

■ D.C. ELECTRICAL CHARACTERISTICS

(1.8V ≤ VCC ≤ 5.5V, GND=0V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Consumption (Note1, Note2)	IDD1	Normal mode WRITE, 1/tSKP=2MHz			6.5	mA
	IDD2	Normal mode READ, 1/tSKP=2MHz			3.3	mA
	IDD3	Power down mode1 READ, 1/tSKP=2MHz			0.75	mA
	IDD4	Power down mode2			0.8	μA
Input High Voltage1 $\overline{CS}$, SK, $\overline{PROTECT}$ pin	VIH1		0.8xVCC			V
Input High Voltage2 $\overline{PD}$, DI pin	VIH2	2.2V ≤ VCC ≤ 5.5V	0.7xVCC			V
	VIH3	1.8V ≤ VCC < 2.2V	0.8xVCC			V
Input Low Voltage1 $\overline{CS}$, SK, $\overline{PROTECT}$ pin	VIL1				0.2xVCC	V
Input Low Voltage2 $\overline{PD}$, DI pin	VIL2	2.2V ≤ VCC ≤ 5.5V			0.3xVCC	V
	VIL3	1.8V ≤ VCC < 2.2V			0.2xVCC	V
Output High Voltage	VOH	IOH=-50μA	VCC-0.3			V
Output Low Voltage	VOL1	2.2V ≤ VCC ≤ 5.5V IOL=1.0mA			0.4	V
	VOL2	1.8V ≤ VCC < 2.2V IOL=0.1mA			0.4	V
Input Leakage	ILI	VIN=VCC			±1.0	μA
3 State Leakage Current	IOZ	$\overline{CS}$="H"			±1.0	μA

Note1: VCC=5.5V, VIN=VCC/GND, DO=OPEN

Note2: Please refer to "Power Down Function" regarding power down mode.

■ A.C. ELECTRICAL CHARACTERISTICS

1) EEPROM section

(1.8V ≤ VCC ≤ 5.5V, GND=0V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SK Cycle Time	tSKP1	2.5V ≤ VCC ≤ 5.5V	500			ns
	tSKP2	1.8V ≤ VCC < 2.5V	1.5			μs
SK Pulse Width	tSKW1	2.5V ≤ VCC ≤ 5.5V	250			ns
	tSKW2	1.8V ≤ VCC < 2.5V	750			ns
SK High Pulse Width	tSKH1	4.0V ≤ VCC ≤ 5.5V	250			ns
	tSKH2	2.5V ≤ VCC < 4.0V	500			ns
(Note3)	tSKH3	1.8V ≤ VCC < 2.5V	750			ns
$\overline{CS}$ Setup Time	tCSS		100			ns
$\overline{CS}$ Hold Time	tCSH1	READ, WREN, WRDS, PDEN, PDDS	100			ns
	tCSH2	WRITE (Note4)	1000			ns
SK Setup Time	tSKS		100			ns
Data Setup Time	tDIS1	4.0V ≤ VCC ≤ 5.5V	100			ns
	tDIS2	2.5V ≤ VCC < 4.0V	150			ns
	tDIS3	1.8V ≤ VCC < 2.5V	200			ns
Data Hold Time	tDIH1	4.0V ≤ VCC ≤ 5.5V	100			ns
	tDIH2	2.5V ≤ VCC < 4.0V	150			ns
	tDIH3	1.8V ≤ VCC < 2.5V	200			ns
Data Output Delay (READ)	tPD1	4.0V ≤ VCC ≤ 5.5V			150	ns
	tPD2	2.5V ≤ VCC < 4.0V			250	ns
	tPD3	2.2V ≤ VCC < 2.5V			300	ns
(Note5)	tPD4	1.8V ≤ VCC < 2.2V			500	ns
Data Output Delay (RDY/$\overline{BUSY}$) (Note5)	tPD				1000	ns
Selftimed Programming Time	tE/W1	2.5V ≤ VCC ≤ 5.5V			7	ms
	tE/W2	1.8V ≤ VCC < 2.5V			10	ms
Write Recovery Time	tRC		100			ns
Min $\overline{CS}$ High Time	tCS		250			ns
DO High-Z Time	tOZ				500	ns

Note3: tSKH is the high pulse width of 16th SK pulse in READ operation. When the data in the next address are read sequentially by continuing to provide clock, tSKH are applied to the high pulse width of 32nd and 48th (multiple of 16) SK pulse in READ operation.

Note4: In case that the data of the DAC section is not changed and the output of the DAC is changed, tCSH is min. 1μs. In case of the other WRITE instruction, tCSH is min. 100ns.

Note5: CL=100pF

2) DAC section

(2.7V ≤ VCC ≤ 5.5V, GND=0V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Reference Voltage A0, A1 A2, A3	 VREF1 VREF2		 2.7 2.7		 VCC VCC	 V V
D/A Reference Current	IREF	VREF=5.0V		200	400	μA
Resolution		Monotonicity			8	bit
Differential Non-Linearity	DNL	VCC=VREF=5.0V	-1	0	+1	LSB
Integral Non-Linearity (Note7)	NL	1LSB=VREF/256 IAO=0.0μA	-1.5	0	+1.5	LSB
Error for Input data "00" (Note6)	EZERO	CL=100pF			+0.1	V
Error for Input data "FF" (Note6)	EFULL				+0.1	V
Buffer-AMP Output Voltage Range(1) 3.6V ≤ VCC ≤ 5.5V (Note8)	VAO1	|IAO| = 0μA	0.1		VCC-0.1	V
	VAO2	|IAO| ≤ 200μA	0.2		VCC-0.2	V
	VAO3	|IAO| ≤ 1mA	0.3		VCC-0.3	V
Buffer-AMP Output Voltage Range(2) 2.7V ≤ VCC < 3.6V	VAO4	|IAO| = 0μA	0.1		VCC-0.1	V
	VAO5	|IAO| ≤ 500μA	0.3		VCC-0.3	V
Setup Time in AUTO READ	tARS		500			μs
D/A Settling Time (CL=100pF)	tLDD1	3.6V ≤ VCC ≤ 5.5V		100	200	μs
	tLDD2	2.7V ≤ VCC < 3.6V			400	μs

Note6: Please refer to the Figure 2.

Note7: Integral Non-Linearity is the error between the actual line and the ideal line. The ideal line exhibits a perfect linear DAC output characteristics between the input digital data "00" and the input digital data "FF".

Note8: VCC=VREF

* Please refer to "Instruction and Data Format" regarding the relation between input digital data and DAC output voltage.

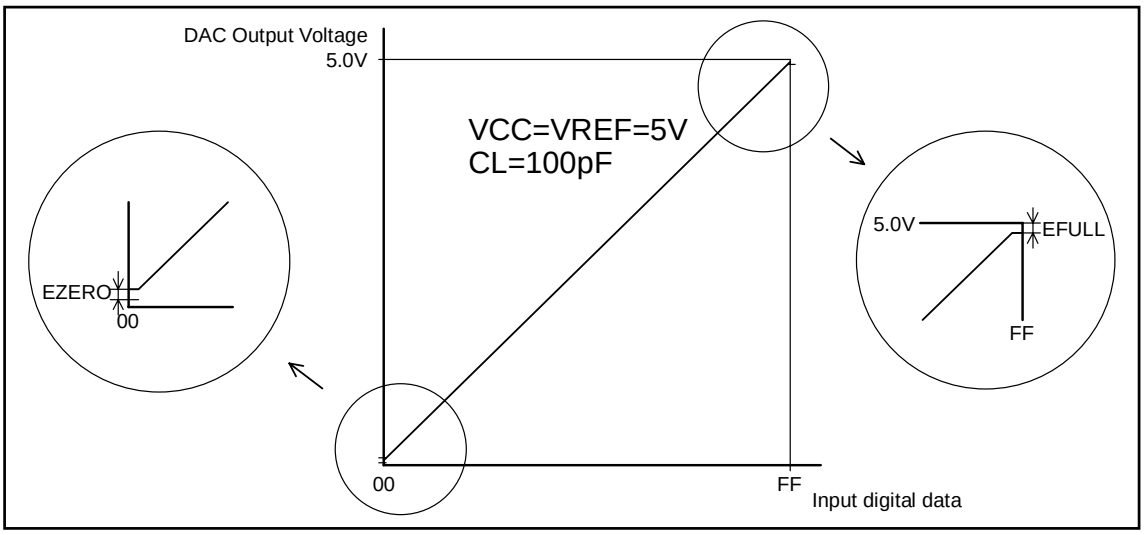
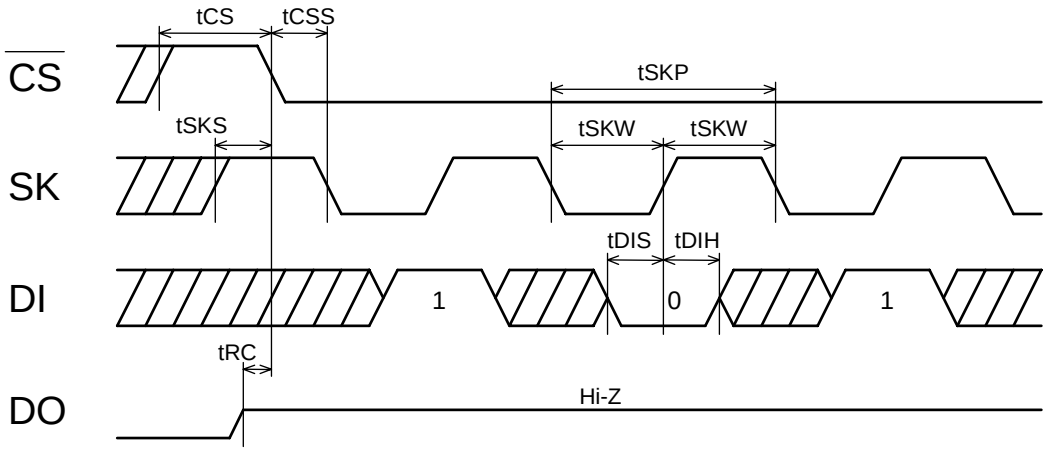
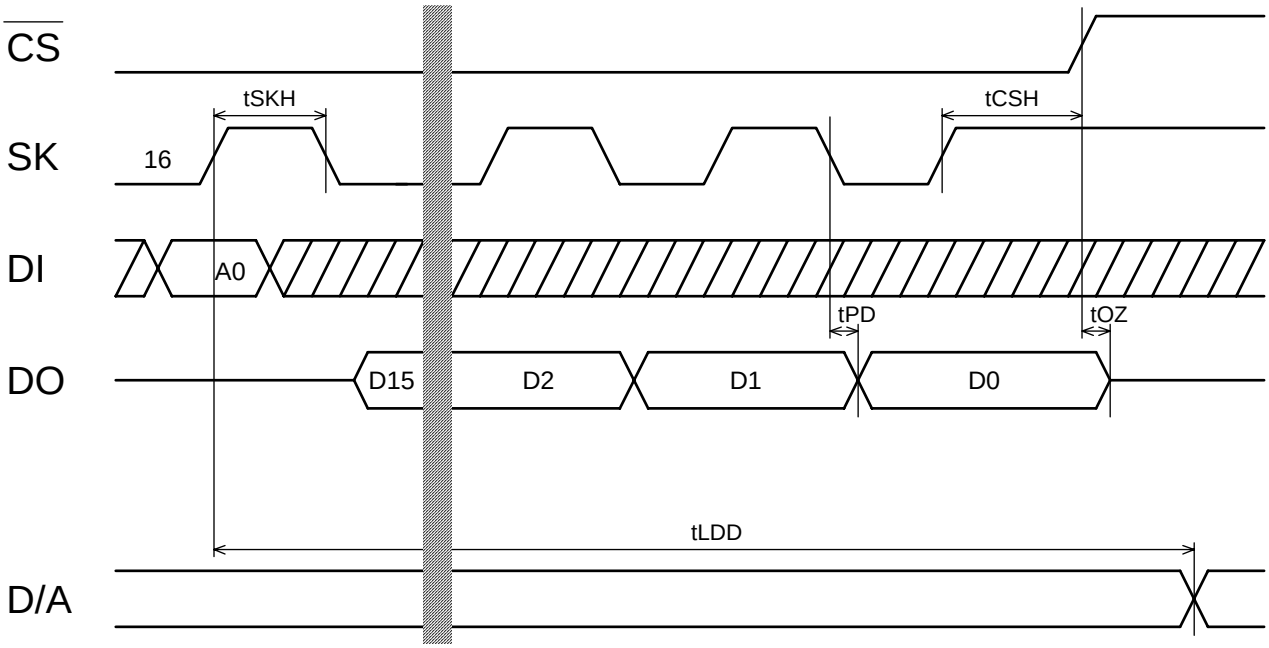


Figure 2. DAC output characteristics (IAO=0.0μA)

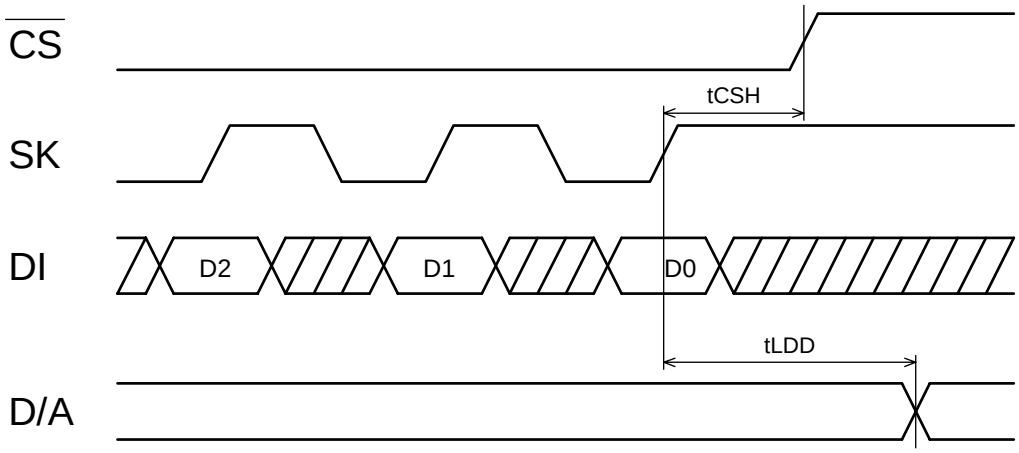
■ Timing Waveform



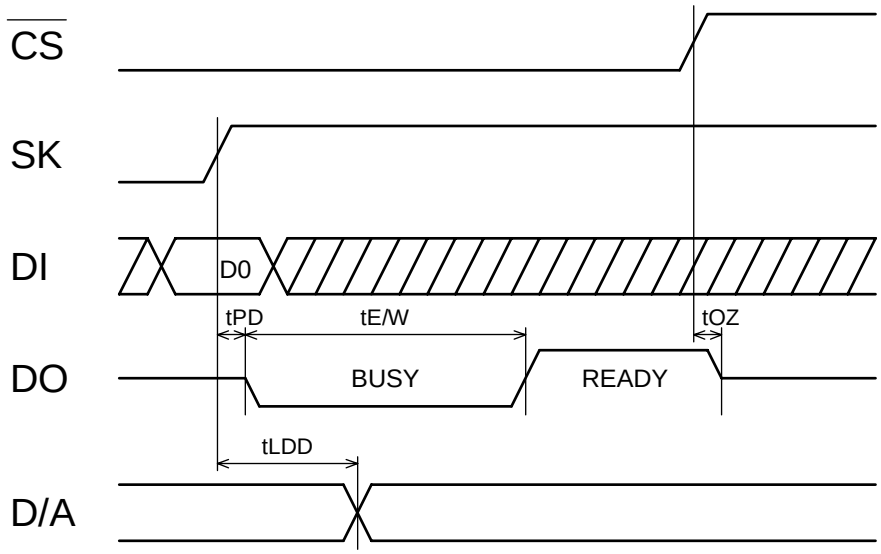
Input Waveform



Waveform in READ instruction

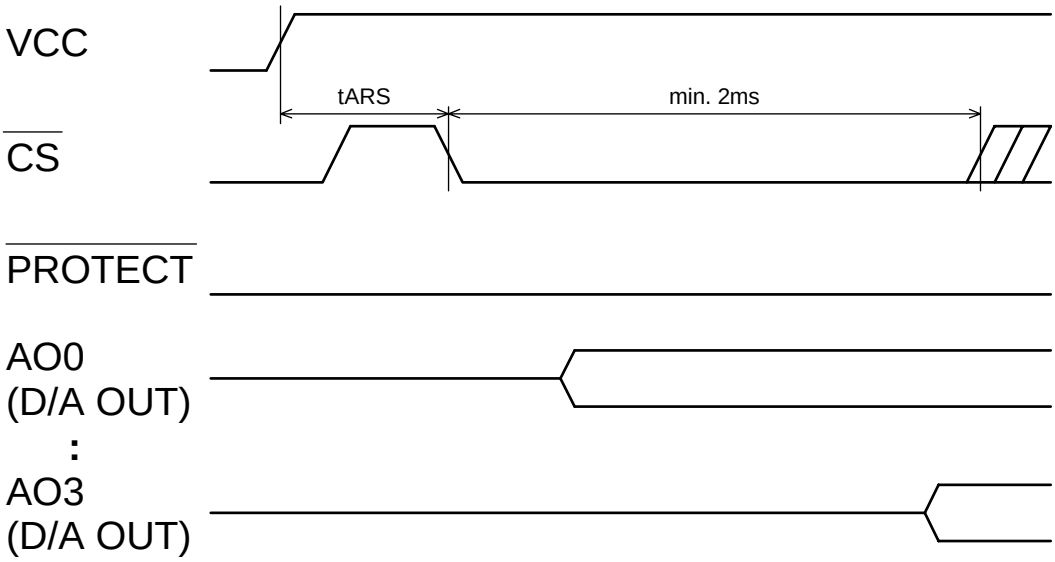


Programming Waveform in WRITE instruction



Status Output

(Note) In case that the data of the DAC section is not changed and the output of the DAC is changed, Ready/Busy signal does not output on DO pin.



Waveform in AUTO READ

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