AKD4522

Evaluation board Rev.A for AK4522

General description

AKD4522 is an evaluation board for audio codec, AK4522. A/D converter and D/A converter can be evaluated separately in addition to loopback mode(A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards(AKD4319, AKD4320, AKD4321 and AKD4324) directly. The AKD4522 has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards(AKD5391/2, AKD5330 and AKD5351/2). Therefore, it is easy to evaluate the D/A section. The AKD4522 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector

■ Ordering guide

AKD4522 --- Evaluation board of AK4522

Function

- ☐ On-Board analog input buffer circuit
- ☐ On-board clock generator
- ☐ Compatible with the following 2 types of interface
  - 1)Direct interface with AKM's A/D and D/A converter, direct interface with a signal generator(AKD43XX) by 10pin Header
  - 2)DIR/DIT with optical input/output
- ☐ A BNC connector for an external clock input

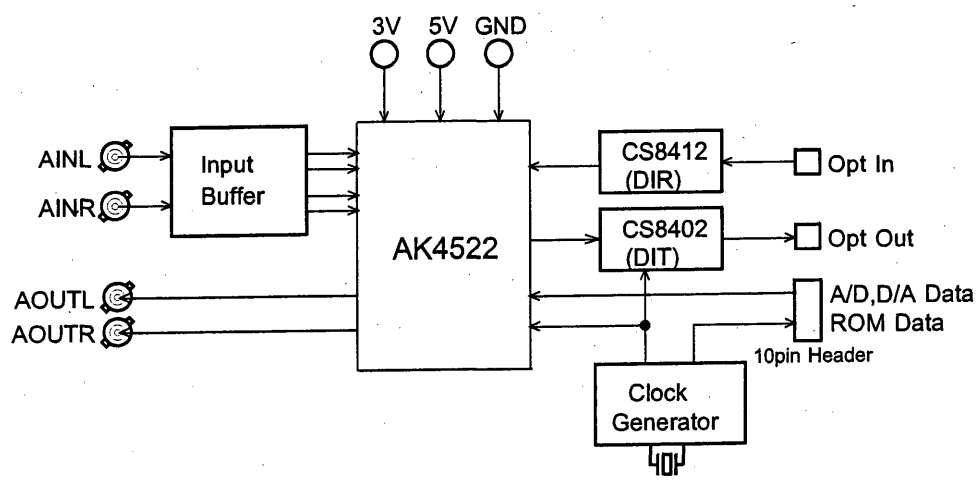
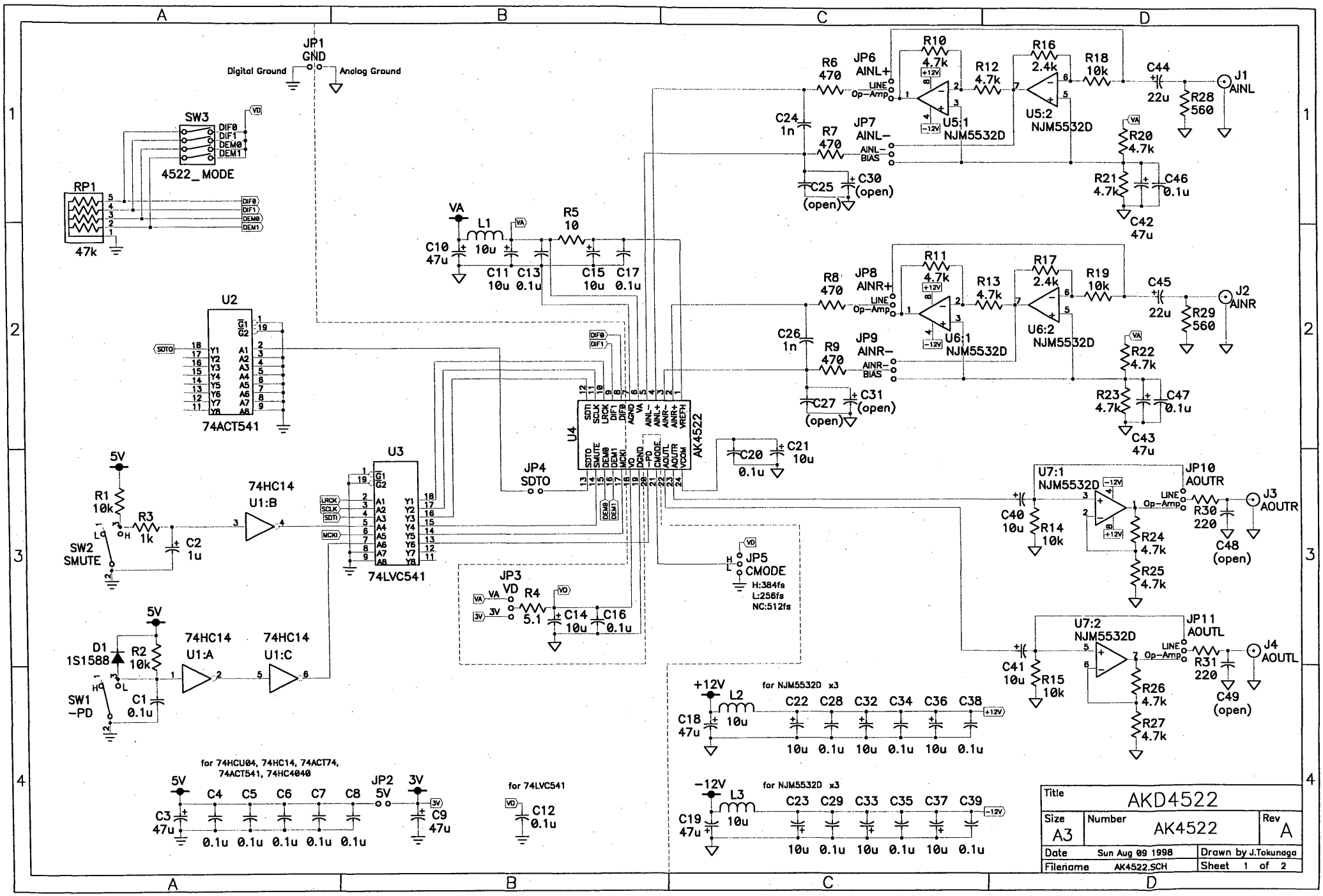
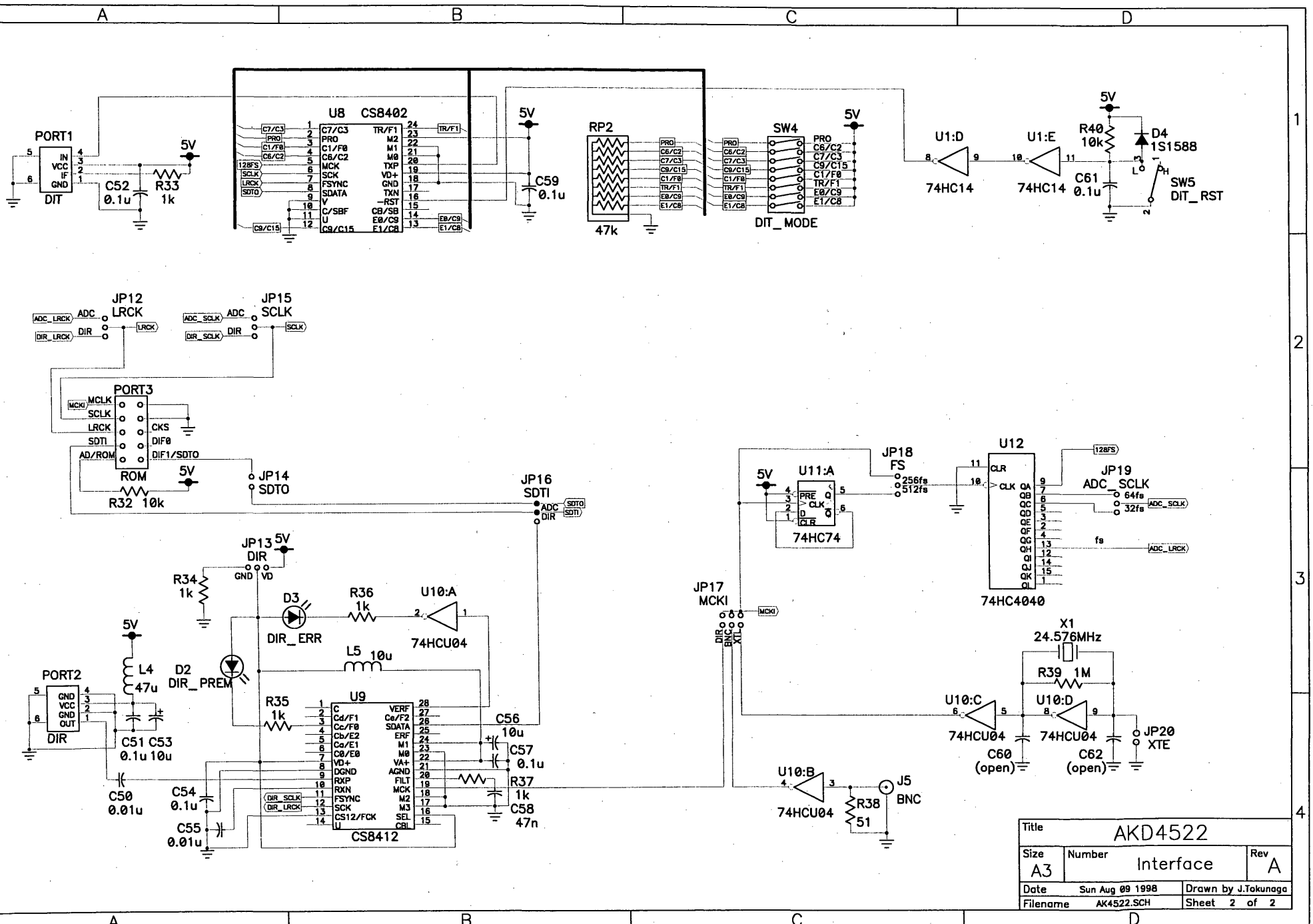


Figure 1. AKD4522 Block Diagram


JP1
GND
Digital Ground
Analog Ground
SW3
4522_MODE
DIF0
DIF1
DEM0
DEM1
RP1
47k
U2
74ACT541
SDTO
U3
74LVC541
U4
AK4522
SDTI
SCLK
LRCK
MCKI
SMUTE
AINL+
AINL-
AINR+
AINR-
VREFH
VCOM
AOUTL
AOUTR
CMODE
DGND
AGND
VA
VD
JP4
SDTO
JP5
CMODE
H:384fs
L:256fs
NC:512fs
JP3
VD
R4
5.1
C14
10u
C16
0.1u
5V
R1
10k
R3
1k
C2
1u
SW2
SMUTE
74HC14
U1:B
D1
1S1588
R2
10k
C1
0.1u
SW1
-PD
74HC14
U1:A
74HC14
U1:C
C10
47u
L1
10u
R5
10
C11
10u
C13
0.1u
C15
10u
C17
0.1u
C20
0.1u
C21
10u
JP6
AINL+
JP7
AINL-
R6
470
R7
470
C24
1n
C25
(open)
C30
(open)
R10
4.7k
R12
4.7k
U5:1
NJM5532D
R16
2.4k
U5:2
NJM5532D
R18
10k
C44
22u
J1
AINL
R28
560
R20
4.7k
R21
4.7k
C46
0.1u
C42
47u
JP8
AINR+
JP9
AINR-
R8
470
R9
470
C26
1n
C27
(open)
C31
(open)
R11
4.7k
R13
4.7k
U6:1
NJM5532D
R17
2.4k
U6:2
NJM5532D
R19
10k
C45
22u
J2
AINR
R29
560
R22
4.7k
R23
4.7k
C47
0.1u
C43
47u
U7:1
NJM5532D
JP10
AOUTR
C40
10u
R14
10k
R24
4.7k
R25
4.7k
R30
220
J3
AOUTR
C48
(open)
U7:2
NJM5532D
JP11
AOUTL
C41
10u
R15
10k
R26
4.7k
R27
4.7k
R31
220
J4
AOUTL
C49
(open)
LINE
Op-Amp
+12V
-12V
L2
10u
C18
47u
C22
C28
C32
C34
C36
C38
10u
0.1u
for NJM5532D x3
L3
10u
C19
47u
C23
C29
C33
C35
C37
C39
for 74HCU04, 74HC14, 74ACT74,
74ACT541, 74HC4040
JP2
C3
47u
C4
C5
C6
C7
C8
C9
47u
for 74LVC541
C12
0.1u
Title
AKD4522
Size
A3
Number
AK4522
Rev
A
Date
Sun Aug 09 1998
Drawn by J.Tokunaga
Filename
AK4522.SCH
Sheet 1 of 2


PORT1
DIT
C52 0.1u
R33 1k
5V
U8 CS8402
C59 0.1u
RP2
47k
SW4
DIT_MODE
U1:D
74HC14
U1:E
74HC14
R40 10k
D4 1S1588
C61 0.1u
SW5 DIT_RST
JP12 LRCK
JP15 SCLK
PORT3
ROM
R32 10k
JP14 SDTO
JP16 SDTI
JP13 DIR
R34 1k
D3 DIR_ERR
R36 1k
U10:A
74HCU04
L4 47u
D2 DIR_PREM
L5 10u
PORT2
DIR
C51 0.1u
C53 10u
C50 0.01u
C54 0.1u
C55 0.01u
U9
CS8412
R35 1k
C56 10u
C57 0.1u
R37 1k
C58 47n
JP17 MCKI
U11:A
74HC74
JP18 FS
256fs
512fs
U12
74HC4040
JP19 ADC_SCLK
64fs
32fs
fs
X1 24.576MHz
R39 1M
U10:C
74HCU04
U10:D
74HCU04
C60 (open)
C62 (open)
JP20 XTE
U10:B
74HCU04
R38 51
J5 BNC
Title AKD4522
Size A3
Number Interface
Rev A
Date Sun Aug 09 1998
Drawn by J.Tokunaga
Filename AK4522.SCH
Sheet 2 of 2

■ Analog Inputs

The ADC inputs are differential and internally biased to the common voltage(VA/2) with 30k Ω (typ) resistance. The signal can be input from either positive or negative input, and the input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input. The AK4522 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative full scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset is removed by the internal HPF.

1. In case of Full-Differential Inputs (default)

Non-inverted and inverted signal are input to AK4522 via inverted op-amp. Since gain of 1st op-amp is 0.24, maximum ampletude of the input signal can be about 4 times larger than spec of AK4522.

[JP6, JP8]	: Op-amp	C25, C27, C30, C31	: None
[JP7]	: AINL-	C24, C26	: 1nF
[JP9]	: AINR-		

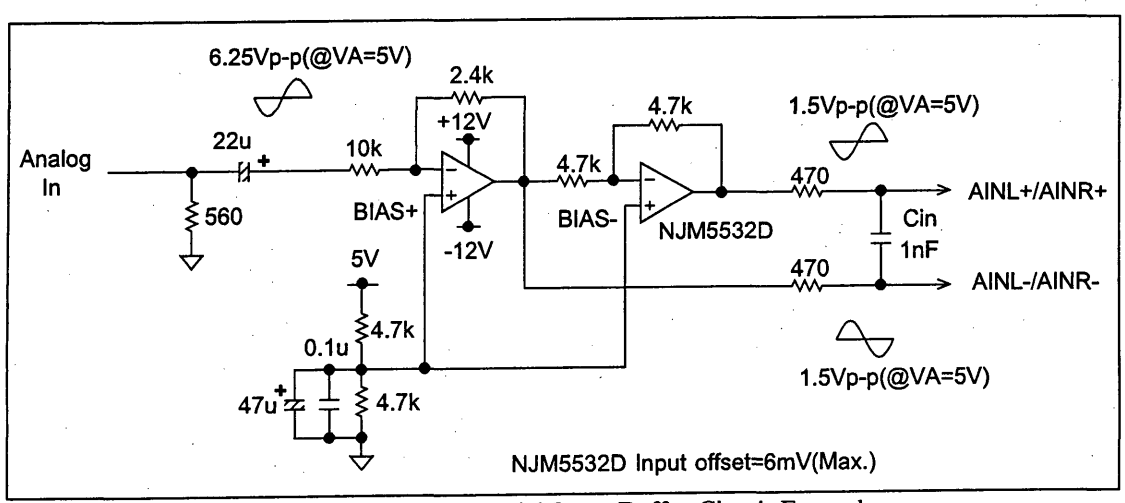


Figure 2. Full-differential Input Buffer Circuit Example

2. In case of Single-ended Input (bias voltage input)

In case of worrying Idle Tone Level, adds offset from external and moves it outside the audio band frequency. The difference between bias voltage of Op-amp and bias voltage(VA/2) of internal device results in the offset. Two inverted op-amps are connected on the evaluation board, however, do not need 2nd op-amp. In this case, if inverted op-amp is input to AINL- or AINR- pin, can be corresponded with polarity. Since gain of 1st op-amp is 0.24, maximum ampletude of the input signal can be about 4 times larger than spec of AK4522.

[JP6, JP8]	: Op-amp	C25, C27, C30, C31	: None
[JP7]	: BIAS	C24, C26	: 1nF
[JP9]	: BIAS		

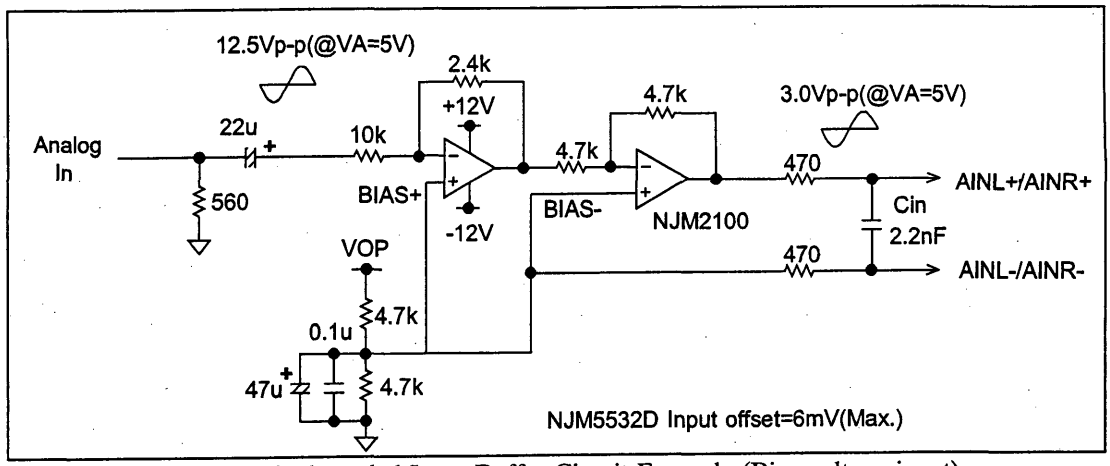


Figure 3. Single-ended Input Buffer Circuit Example (Bias voltage input)

3. In case of Single-ended Input (no input bias)

Analog signal is directly input from BNC connector and this case can reduce the part of input buffer circuit. In case of comparing Full-differential Input circuit(Figure 2.) or Single-ended Input circuit (Figure 3.) with no input buffer circuit shown in Figure 4., external mute should be taken enough time as "pop" noise is large at reset.

[JP6, JP8]	: LINE	C25, C27	: 0.1uF
[JP7]	: BIAS	C30, C31	: 4.7uF
[JP9]	: BIAS	C24, C26	: 2.2nF

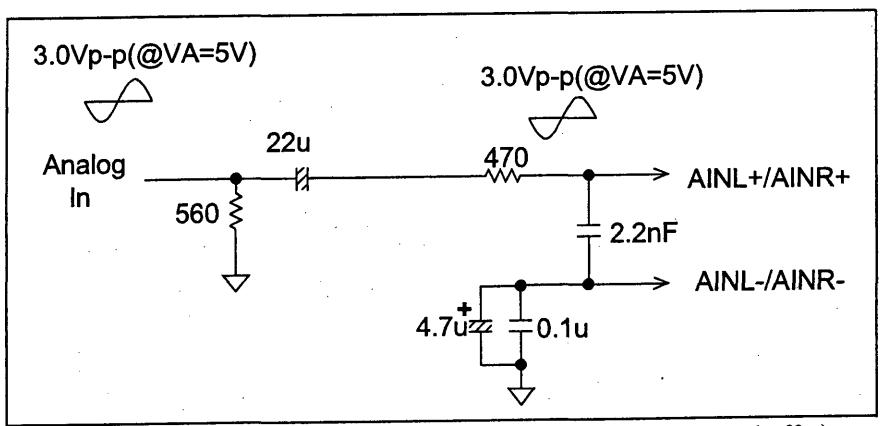


Figure 4. Single-ended Input Buffer Circuit Example (no input buffer)

■ Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.
DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

1. Output via non-inverted op-amp

Gain=6dB.

[JP10, JP11] : Op-amp

2. Output directly

[JP10, JP11] : LINE

■ Grounding and Power Supply Decoupling of AK4522

The AK4522 requires careful attention to power supply and grounding arrangements. VA pin and VD pin are usually supplied from analog supply in system. Alternatively if VA pin and VD pin are supplied separately, the power up sequence is not critical. AGND pin and DGND pin of the AK4522 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4522 as possible, with the small value ceramic capacitor being the nearest.

■ Voltage Reference Inputs of AK4522

The differential Voltage between VREFH pin and AGND pin sets the analog input/output range. VREFH pin is normally connected to VA pin with a 0.1uF ceramic capacitor. VCOM pin is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4522.

■ Operation sequence

① **Set up the power supply lines.**

[VA]	(red)	= 4.5 ~ 5.5V	(VA of AK4522)
[3V]	(orange)	= 2.7 ~ 5.5V	(VD of AK4522)
[5V]	(red)	= 3.5 ~ 5.5V	(Power supply to digital interface)
[+12V]	(orange)	= 12 ~ 15V	(Op-amp)
[-12V]	(blue)	= -12 ~-15V	(Op-amp)
[AGND]	(black)	= 0V	(AGND,DGND of AK4522 and Ground of analog interface)
[DGND]	(black)	= 0V	(Ground of digital interface)

Each supply line should be distributed from the power supply unit.

1. VD of AK4522 and Power supply to digital interface
   - In case of separated [JP2] : open
   - In case of common [JP2] : short
2. VA and VD of AK4522
   - In case of separated [JP3] : 3V
   - In case of common [JP3] : VA
3. Analog ground (includes AGND and DGND of AK4522) and digital ground
   - In case of separated [JP1] : open
   - In case of common [JP1] : short

② **Set up the evaluation modes and jumper pins.** (See p.7 ~)
There are many jumper pins to cover many evaluation mode. Please take care of setting.

③ **Set up the DIP-SW.**
SW3 : Set up AK4522 (See p.9)
SW4 : Set up CS8402 (See p.10)
(Upper side is "ON" and lower side is "OFF".)

④ **Power on.**
The AK4522 should be reset once bringing $\overline{PD}$ (SW1)"L" upon power-up.

■ Evaluation modes and jumper pins

Applicable Evaluation Mode

① Loopback mode (Default)
② Evaluation of D/A using ideal sine wave generated by ROM data.
③ Evaluation of D/A using A/D converted data
④ Evaluation of D/A using DIR(Optical Link)
⑤ Evaluation of A/D usingUsing D/A converted data
⑥ Evaluation of A/D DIT(Optical Link)
⑦ All interface signals including master clock are fed externally.

※① and ⑥ can be evaluated at the same time by the same set up.

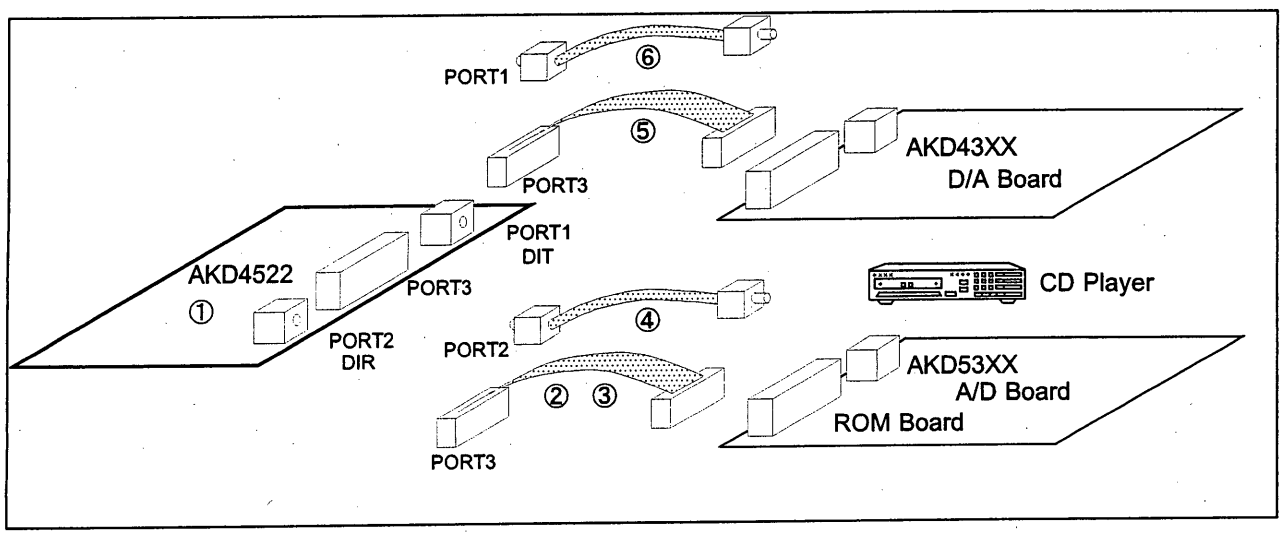


Figure 5. Wiring cables corresponded some evaluation modes

① **Loopback mode** (Default)
Nothing should be connected to PORT2, PORT3.

[JP13] (DIR)	: GND	[JP12] (LRCK)	: ADC
[JP17] (MCKI)	: XTL	[JP15] (SCLK)	: ADC
[JP20] (XTE)	: open	[JP16] (SDTI)	: ADC

② **Evaluation of D/A using A/D converted data from ideal sine wave generated by ROM data**
Digital signals generated by AKD43XX are used. PORT3 is used for the interface with AKD43XX. Master clock is sent from AKD4522 to AKD43XX and SCLK, LRCK, SDATA are sent from AKD43XX to AKD4522. Nothing should be connected to PORT2.

[JP13] (DIR)	: GND	[JP12] (LRCK)	: open
[JP17] (MCKI)	: XTL	[JP15] (SCLK)	: open
[JP20] (XTE)	: open	[JP16] (SDTI)	: open

③ **Evaluation of D/A using A/D converted data**
It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5391/2, AKD5330 and AKD5352/1) with PORT3. Master clock, SCLK, LRCK and SDATA are sent from A/D board to AKD4522. Nothing should be connected to PORT2.

[JP13] (DIR)	: GND	[JP12] (LRCK)	: open
[JP17] (MCKI)	: open	[JP15] (SCLK)	: open
[JP20] (XTE)	: short	[JP16] (SDTI)	: open

④ **Evaluation of D/A using DIR (Optical Link)**

PORT2 is used. DIR generates MCLK, SCLK LRCK and SDATA from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT3. CS8412(DIR) needs the operating voltage of VD+≧ 3.2V.

[JP13] (DIR)	: VD	[JP12] (LRCK)	: DIR
[JP17] (MCKI)	: DIR	[JP15] (SCLK)	: DIR
[JP20] (XTE)	: short	[JP16] (SDTI)	: DIR

⑤ **Evaluation of A/D using D/A converted data**

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards (AKD4319, AKD4320 AKD4321 and AKD4324) with PORT3. Nothing should be connected to PORT2.

[JP13] (DIR)	: GND	[JP12] (LRCK)	: ADC
[JP17] (MCKI)	: XTL	[JP15] (SCLK)	: ADC
[JP20] (XTE)	: open	[JP16] (SDTI)	: ADC

⑥ **Evaluation of A/D using DIT (Optical Link)**

PORT1 is used. DIT generates SDATA from received data and which is output through optical connector (TOTX174). It is possible to connect AKM's evaluation boards (AKD4319, AKD4320, AKD4321 and AKD4324), digital-amplifier and etc. Nothing should be connected to PORT2, PORT3. This set-up is same as that of ①. CS8402(DIT) needs the operating voltage of VD+≧ 3.2V. SW5 should be kept "H" during normal operation.

[JP13] (DIR)	: GND	[JP12] (LRCK)	: ADC
[JP17] (MCKI)	: XTL	[JP15] (SCLK)	: ADC
[JP20] (XTE)	: open	[JP16] (SDTI)	: ADC

⑦ **All interfacing signals including master clock are fed externally.**

Under the following set-up, all external signals needed for the AK4522 to operate could be fed through PORT3.

[JP13] (DIR)	: GND	[JP12] (LRCK)	: open
[JP17] (MCKI)	: open	[JP15] (SCLK)	: open
[JP20] (XTE)	: short	[JP16] (SDTI)	: open

■ Master clock set-up

① **256fs**

[JP5] (CMODE) : L [JP18] (FS) : 256fs

② **512fs**

[JP5] (CMODE) : open [JP18] (FS) : 512fs

■ SCLK set-up

SCLK can be selected 64fs or 32fs by JP19(ADC_SCLK).

■ Other jumpers set-up

[JP4] : short (always)
[JP14] : open (always)

■ The function of the toggle SW.

[SW1] : Resets the AK4522. Keep "H" during normal operation.
[SW2] : Initiates soft mute cycle of AK4522. If this switch goes "H", soft mute cycle is initiated. Keep "L" during normal operation.
[SW5] : Resets the CS8402. "L" resets the internal counter of CS8402, then Bi-phase signal is not output. Keep "H" during normal operation.
(Upper-side is "H" and lower-side is "L".)

■ The indication content for LED.

[D3] : Monitors VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.
[D2] : Indicates whether the input data of CS8412 is pre-emphasized or not. LED turns on when the data is pre-emphasized.

■ DIP switch set-up

[SW3] : This switch sets up the operation mode of the AK4522.
Confirm the set-up of the DIP-SW before evaluation starts.
Refer to AK4522 data-sheet about detail information. ON means "H" and OFF, "L".
Since formats of CS8402, CS8412 are fixed IIS(I2S), set DIF1,0 ON if use them.

Mode	DIF1	DIF0	SDTO(ADC)	SDTI(DAC)	L/R	SCLK	
0	OFF	OFF	20bit, MSB justified	16bit, LSB justified	H/L	64fs, 32fs	
1	OFF	ON	20bit, MSB justified	20bit, LSB justified	H/L	64fs	
2	ON	OFF	20bit, MSB justified	20bit, MSB justified	H/L	64fs	
3	ON	ON	IIS(I2S)	IIS(I2S)	L/H	64fs, 32fs	(default)

Table 1. Serial Data Interface Format Mode

DEM1	DEM0	Mode	
OFF	OFF	44.1kHz	
OFF	ON	OFF	(default)
ON	OFF	48kHz	
ON	ON	32kHz	

Table 2. De-emphasis filter control

[SW4] : This switch sets the C-bit of CS8402. (Default is the consumer mode)
This set-up does not affect the evaluation of the AK4522. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data-sheet.

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=0	Professional mode, C0=1
2,3	$\overline{C6}$,$\overline{C7}$	C6,C7 - Sampling frequency
	1 1	00 - Not indicated. Receiver default to 48kHz.
	1 0	01 - 48kHz
	0 1	10 - 44.1kHz
	0 0	11 - 32kHz
4	$\overline{C9}$	C8,C9,C10,C11 - 1bit of channel mode
	1	0000 - Mode not indicated. Receiver default to
	0	2-channel mode.
		0100 - Stereophonic.
5	$\overline{C1}$	C1 - Audio mode
	1	0 - Normal audio
	0	1 - Non-audio
6	TRNPT	Transparent mode * CS8402 is CRE
	0	Normal mode
	1	Transparent mode
8,7	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1	000 - Emphasis not indicated. Receiver defaults to no
	1 0	emphasis with manual override enabled.
	0 1	100 - None
	0 0	110 - 50/15usec
		111 - CCITT J.17

Table 3. DIP switch set-up of CS8402 (Professional mode)

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=1	Consumer mode, C0=0 (Default)
2	$\overline{C2}$	C2 - Copy
	1	0 - Copy inhibited
Default	0	1 - Copy permitted
3	$\overline{C3}$	C3,C4,C5 - Pre-emphasis
Default	1	000 - None
	0	100 - 50/15usec
4	$\overline{C15}$	C15 - Generation Status
	1	0 - See the standard
Default	0	1 - See the standard
6,5	FC1,FC0	C24,C25,C26,C27- Sampling frequency
	0 0	0000 - 44.1kHz
Default	0 1	0100 - 48kHz
	1 0	1100 - 32kHz
	1 1	0000 - 44.1kHz, CD mode
8,7	$\overline{C8}$,$\overline{C9}$	C8-C14 - Category code
Default	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - CD
	0 0	1100000 - DAT

Table 4. DIP switch set-up of CS8402 (Consumer mode)

AK4522 Measurement Results

[Measurement Condition]

- Measurement unit : ROHDE & SCHWARZ, UPD04
- MCLK : 256fs
- BCLK : 64fs
- Bit : 20bit
- fs : 44.1kHz
- Power Supply : VA=5V, VD=5V/3V
- Interface : DIT/DIR
- Temperature : Room

1. A/D Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	92.2 dB	92.5 dB
Dynamic Range	1kHz, -20dB	20kLPF	96.7 dB	96.9 dB
		20kLPF, A-weight	100.5 dB	100.7 dB
	1kHz, -60dB	20kLPF	96.7 dB	96.9 dB
		20kLPF, A-weight	100.0 dB	100.2 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.0 dB	97.3 dB
		20kLPF, A-weight	101.0 dB	101.1 dB

4. D/A Output

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	90.6 dB	90.7 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.1 dB
		20kLPF, A-weight	100.4 dB	100.5 dB
	1kHz, -60dB	20kLPF	97.1 dB	97.2 dB
		20kLPF, A-weight	100.6 dB	100.5 dB
S/N	1kHz, 0dB / "0"data IN	20kLPF	97.2 dB	97.3 dB
		20kLPF, A-weight	100.6 dB	100.6 dB

[Measurement Condition]

- Measurement unit : Audio Precision System two
- MCLK : 256fs
- BCLK : 64fs
- Bit : 20bit
- fs : 44.1kHz
- Power Supply : VA=5V, VD=5V/3V
- Interface : DIT/DIR
- Temperature : Room

1. A/D Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	94.7 dB	94.9 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.1 dB
		20kLPF, A-weight	99.8 dB	100.0 dB
	1kHz, -60dB	20kLPF	97.0 dB	97.2 dB
		20kLPF, A-weight	99.7 dB	100.0 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.1 dB	97.2 dB
		20kLPF, A-weight	100.1 dB	100.1 dB

2. A/D Output (Single-ended inputs with external bias, refer to Figure 3.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	80.8 dB	82.2 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.2 dB
		20kLPF, A-weight	99.8 dB	100.0 dB
	1kHz, -60dB	20kLPF	97.1 dB	97.4 dB
		20kLPF, A-weight	99.7 dB	100.0 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.3 dB	97.5 dB
		20kLPF, A-weight	100.1 dB	100.5 dB

3. A/D Output (Single-ended inputs without external bias, refer to Figure 4.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, -0.5dB	20kLPF	79.7 dB	81.2 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.1 dB	97.3 dB
		20kLPF, A-weight	99.9 dB	100.2 dB
	1kHz, -60dB	20kLPF	97.2 dB	97.5 dB
		20kLPF, A-weight	100.2 dB	100.4 dB
S/N	1kHz, 0dB/GND IN	20kLPF	97.2 dB	97.6 dB
		20kLPF, A-weight	100.3 dB	100.6 dB

4. D/A Output

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	91.4 dB	91.5 dB
Dynamic Range	1kHz, -20dB	20kLPF	97.0 dB	97.0 dB
		A-weight	99.6 dB	99.6 dB
	1kHz, -60dB	20kLPF	97.0 dB	97.0 dB
		A-weight	99.5 dB	99.6 dB
S/N	1kHz, 0dB / "0"data IN	20kLPF	97.0 dB	97.1 dB
		A-weight	99.6 dB	99.7 dB

5. A/D→D/A Loopback Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	89.3 dB	89.5 dB
Dynamic Range	1kHz, -20dB	20kLPF	93.9 dB	94.0 dB
		A-weight	96.6 dB	96.8 dB
	1kHz, -60dB	20kLPF	93.9 dB	94.0 dB
		A-weight	96.5 dB	96.7 dB
S/N	1kHz, 0dB/GND IN	20kLPF	93.9 dB	93.9 dB
		A-weight	96.7 dB	96.7 dB

6. A/D→D/A Loopback Output (Single-ended inputs with external bias, refer to Figure 3.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	79.1 dB	80.3 dB
Dynamic Range	1kHz, -20dB	20kLPF	94.0 dB	94.0 dB
		A-weight	96.6 dB	96.8 dB
	1kHz, -60dB	20kLPF	93.9 dB	94.0 dB
		A-weight	96.4 dB	96.7 dB
S/N	1kHz, 0dB/GND IN	20kLPF	94.0 dB	94.1 dB
		A-weight	96.8 dB	96.9 dB

7. A/D→D/A Loopback Output (Single-ended inputs without external bias, refer to Figure 4.)

Parameter	Input signal	Measurement Filter	VD = 5V	VD = 3V
S/(N+D)	1kHz, 0dB	20kLPF	78.2 dB	79.4 dB
Dynamic Range	1kHz, -20dB	20kLPF	94.0 dB	94.1 dB
		A-weight	96.6 dB	96.8 dB
	1kHz, -60dB	20kLPF	94.0 dB	94.1 dB
		A-weight	96.9 dB	97.0 dB
S/N	1kHz, 0dB/GND IN	20kLPF	93.9 dB	94.0 dB
		A-weight	96.8 dB	97.0 dB

AK4522 ADC part

Conditions :

AVDD = DVDD = 5.0V

fs = 44.1kHz, MCLK = 256fs, BICK = 64fs,

Measurement unit = ROHDE & SCHWARZ UPD04

Interface = DIT

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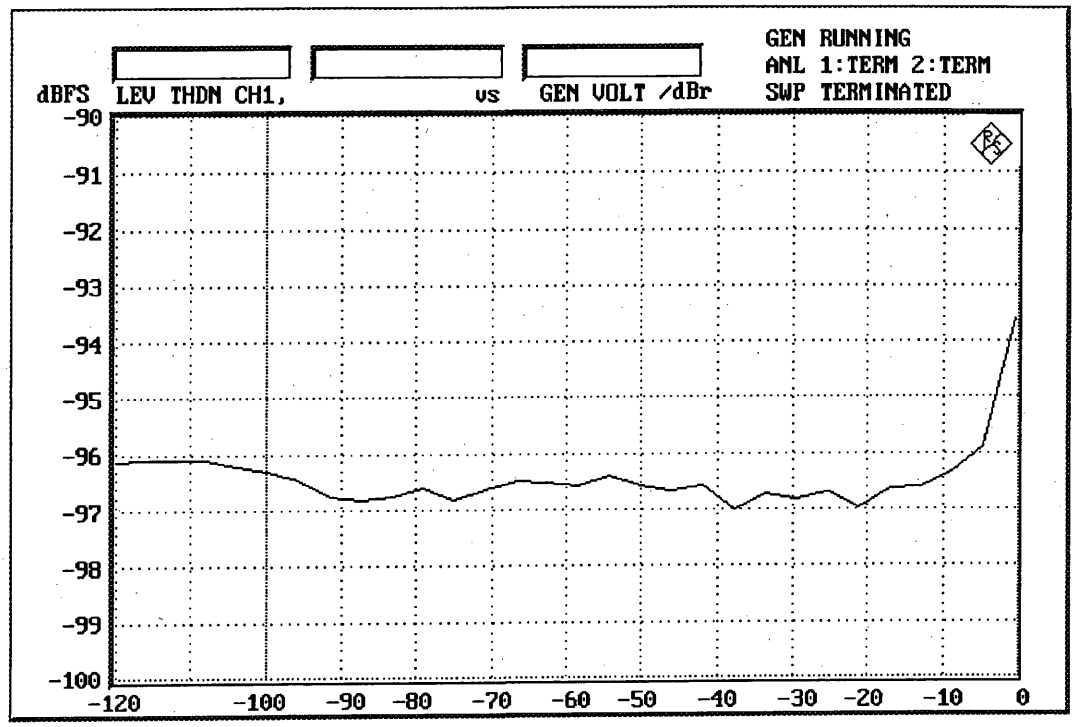


Figure 34 : THD+N vs. Input level (fin : 1kHz (Full-differential input))

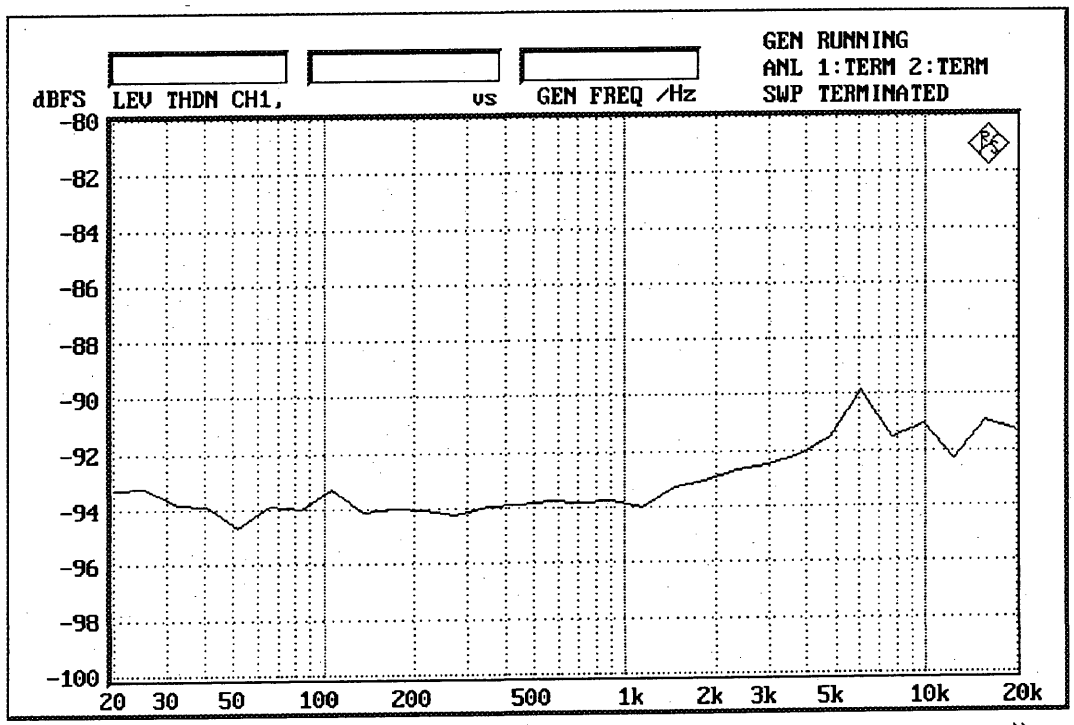


Figure 35 : THD+N vs. Input frequency (input level : -0.5dBFS (Full-differential input))

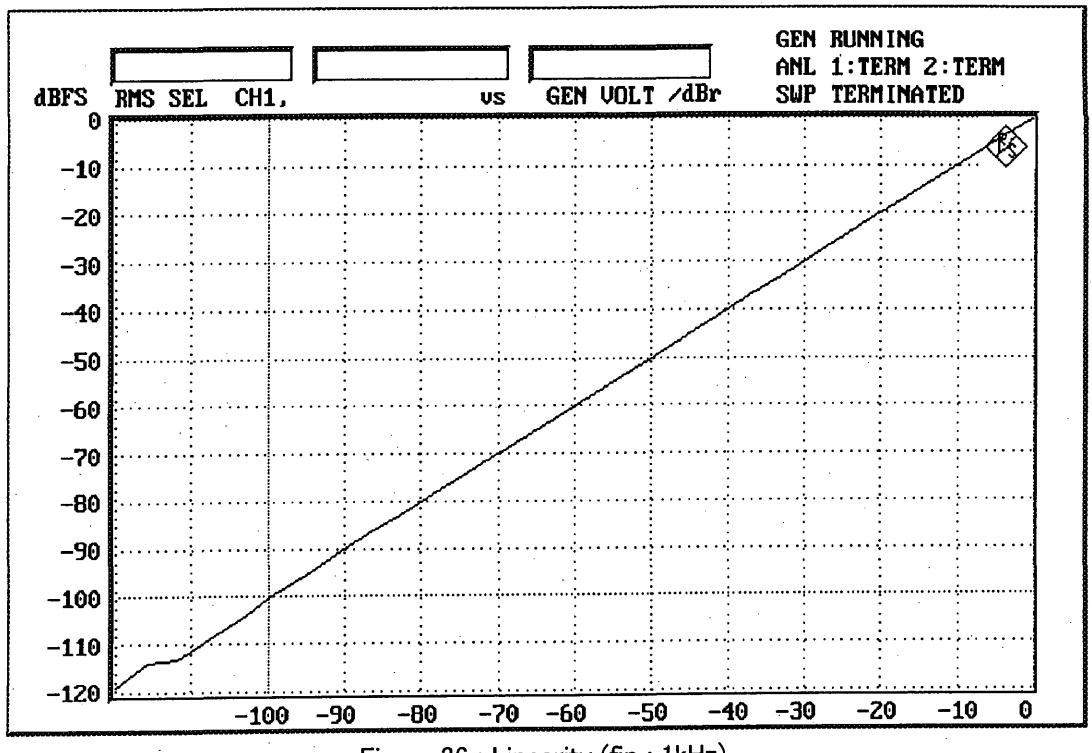


Figure 36 : Linearity (fin : 1kHz)

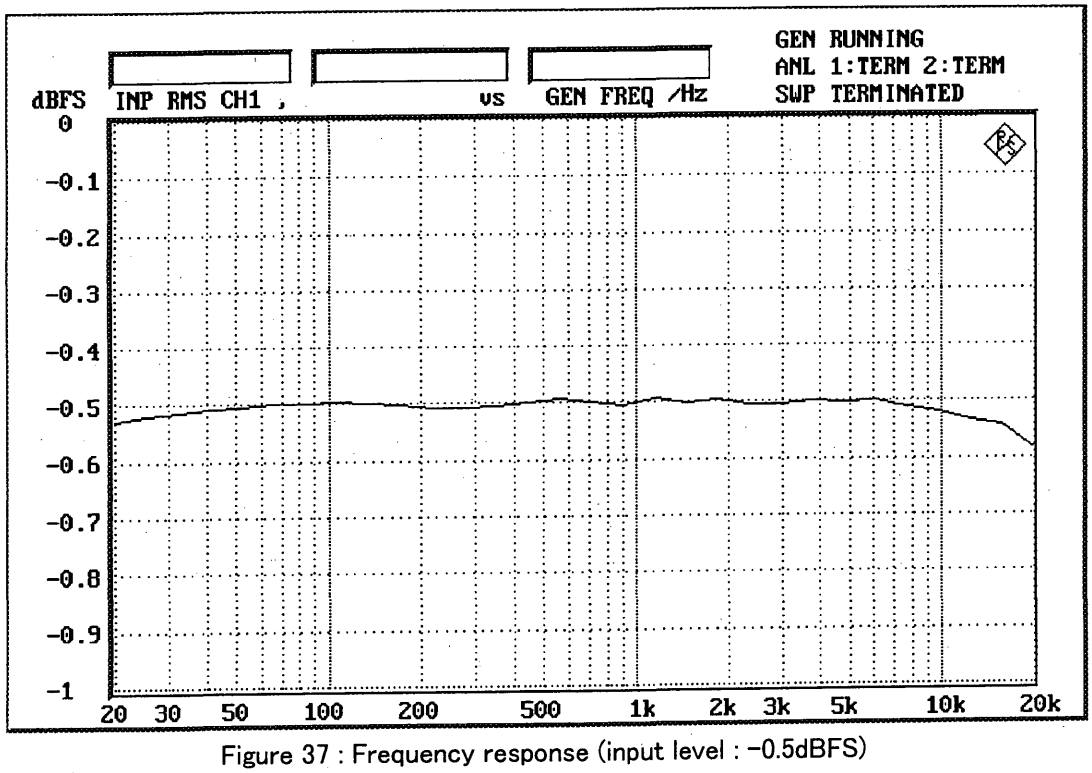


Figure 37 : Frequency response (input level : −0.5dBFS)

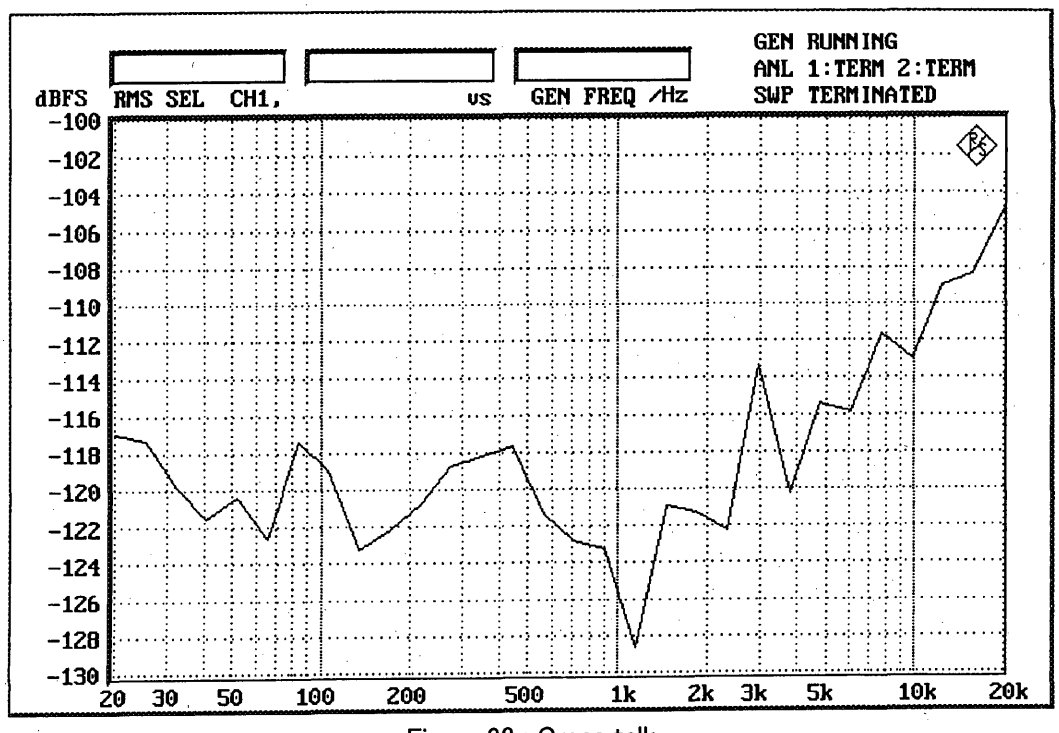


Figure 38 : Cross talk

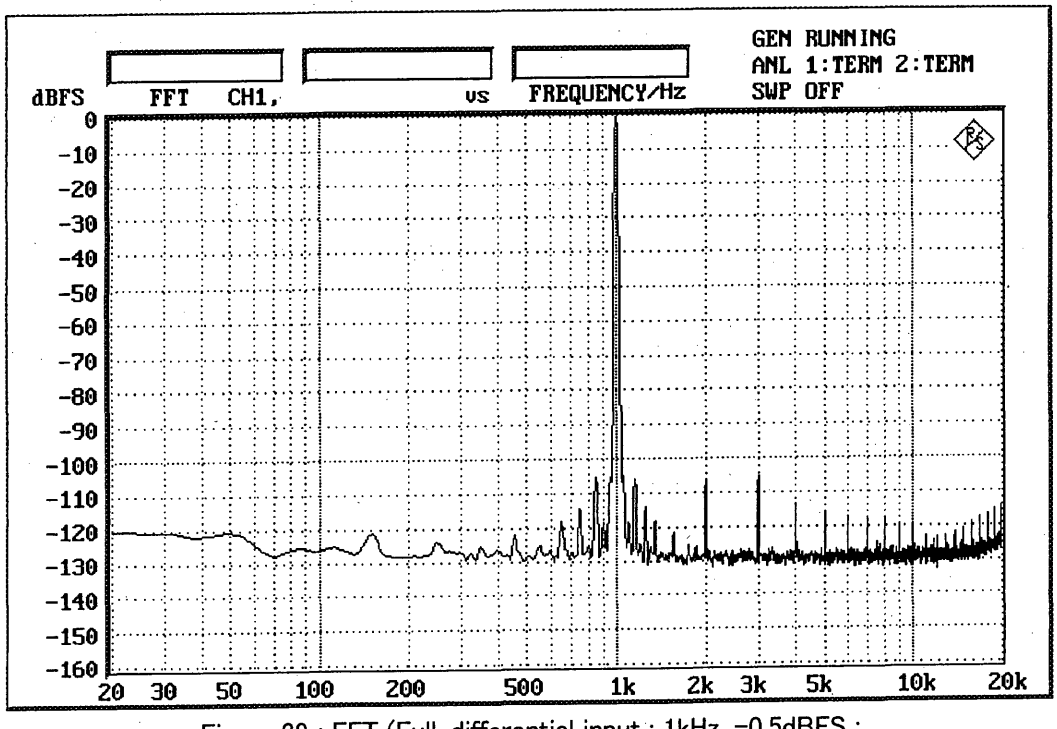


Figure 39 : FFT (Full-differential input : 1kHz, −0.5dBFS ;

FFT points : 8192, averaging : 10)

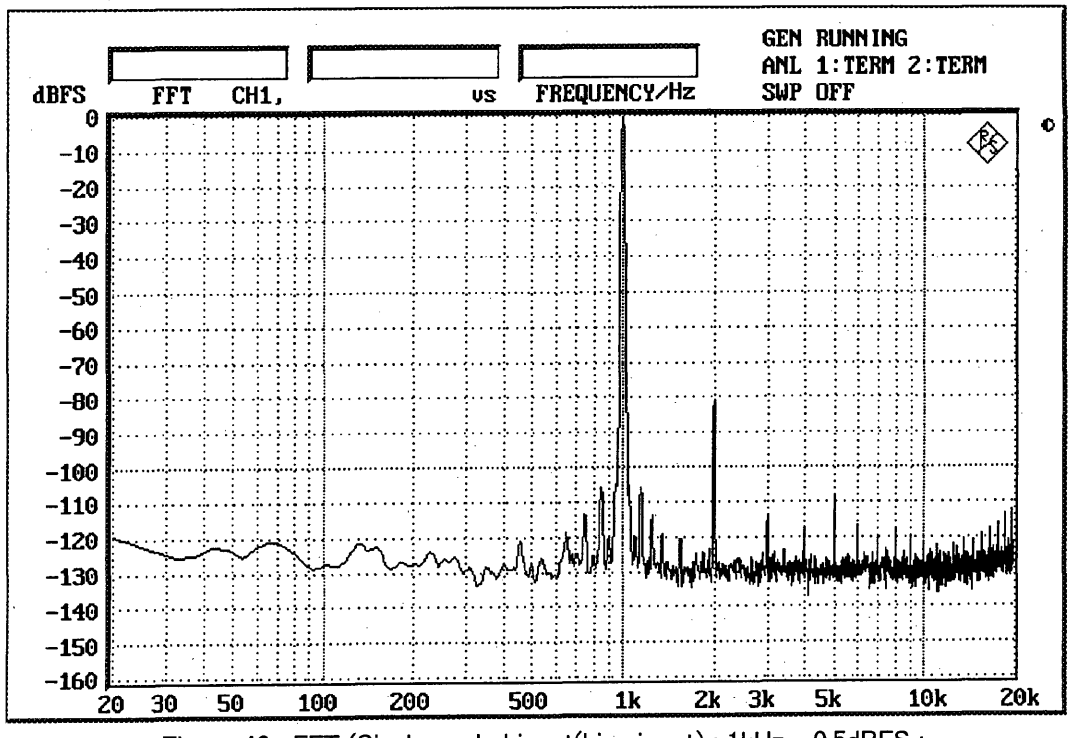


Figure 40 : FFT (Single-ended input(bias input) : 1kHz, -0.5dBFS ;
FFT points : 8192, averaging : 10)

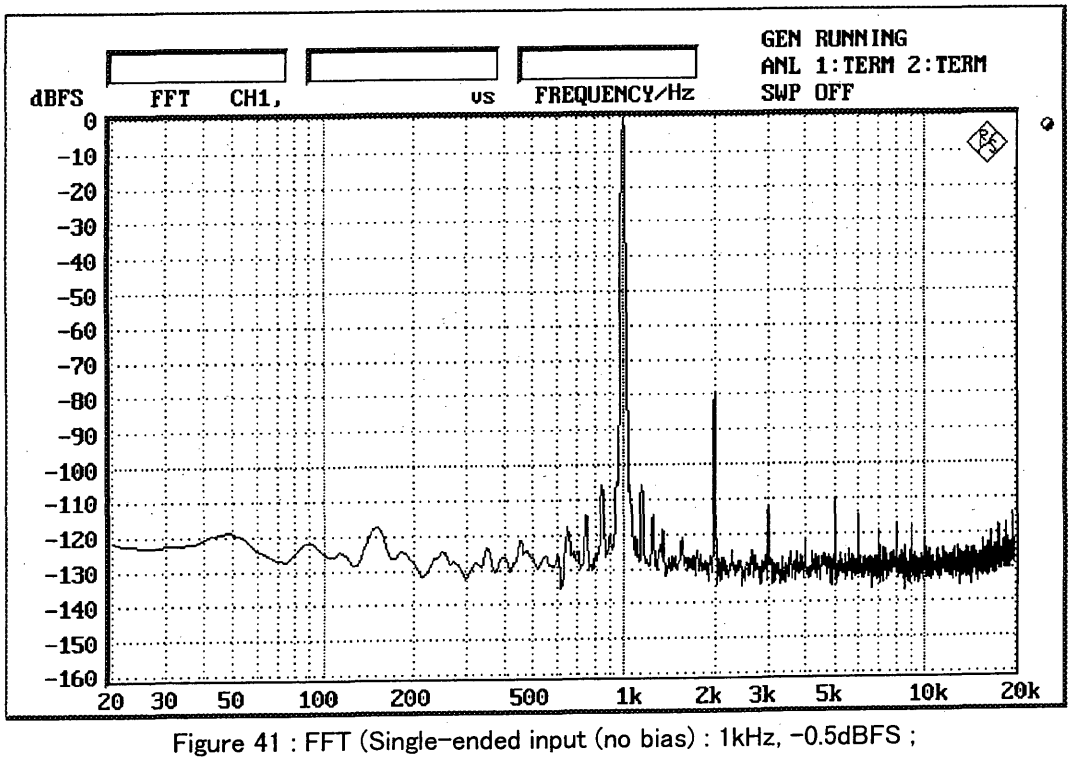


Figure 41 : FFT (Single-ended input (no bias) : 1kHz, -0.5dBFS ;
FFT points : 8192, averaging : 10)

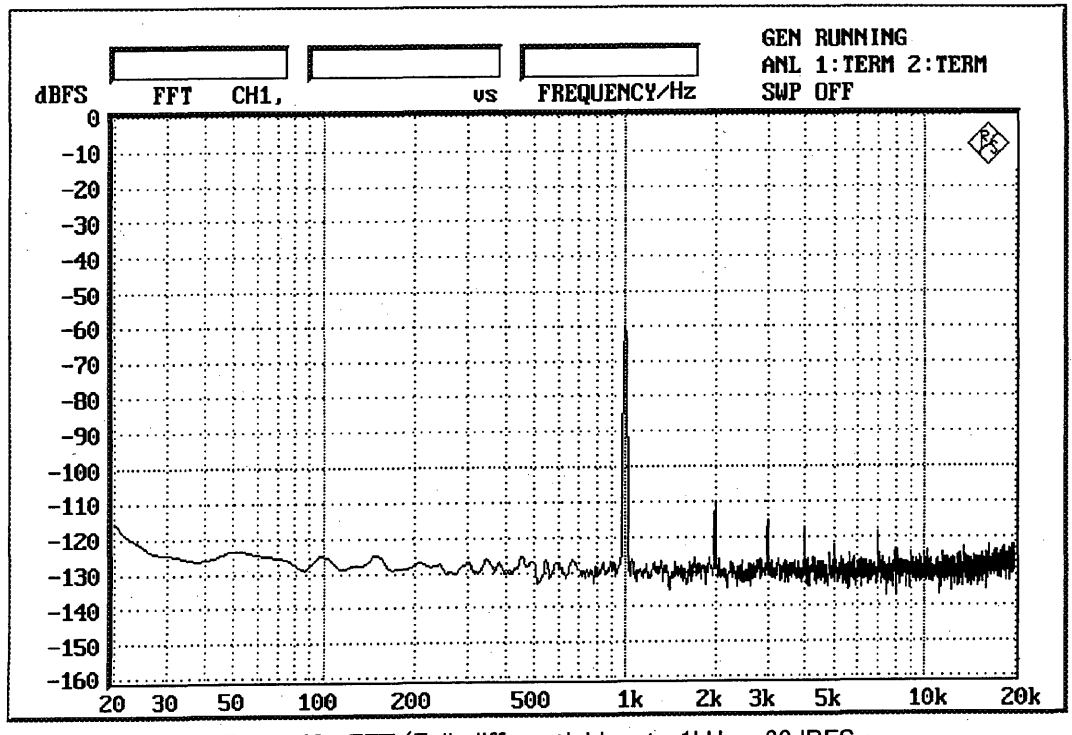


Figure 42 : FFT (Full-differential input : 1kHz, -60dBFS ;
FFT points : 8192, averaging : 10)

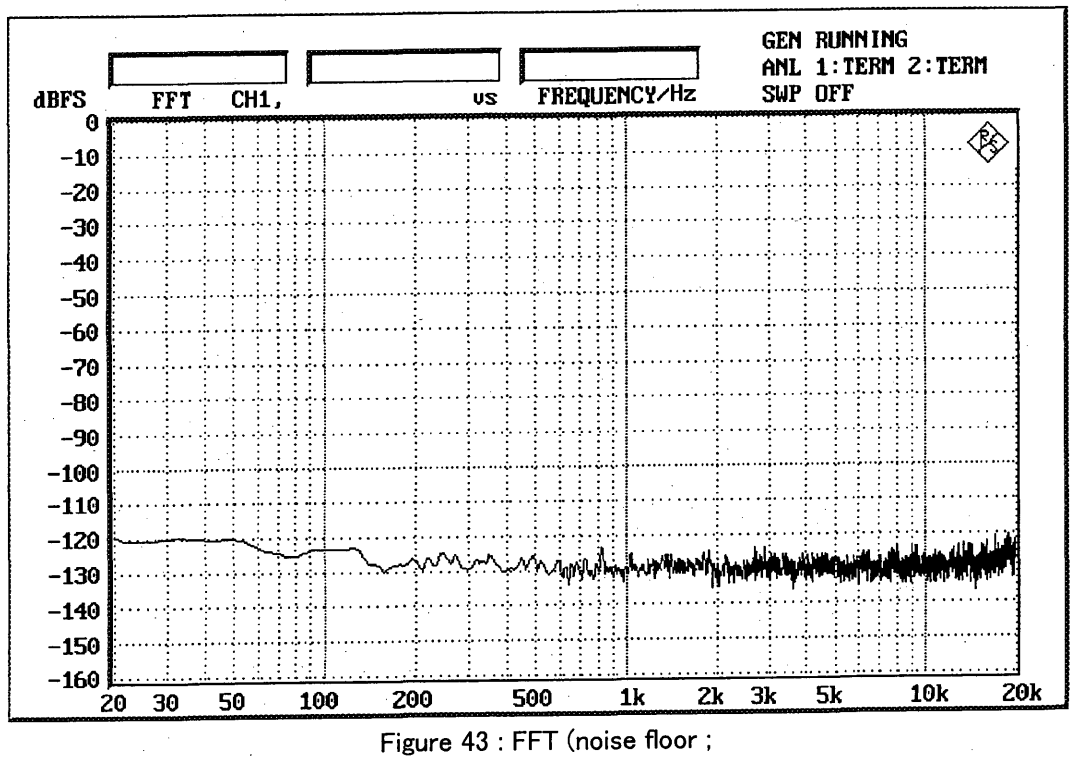


Figure 43 : FFT (noise floor ;
FFT points : 8192, averaging : 10)

AK4522 DAC part

Conditions :

AVDD = DVDD = 5.0V

fs = 44.1kHz, MCLK = 256fs, BICK = 64fs,

Measurement unit = ROHDE & SCHWARZ UPD04

Interface = DIR

Contents :

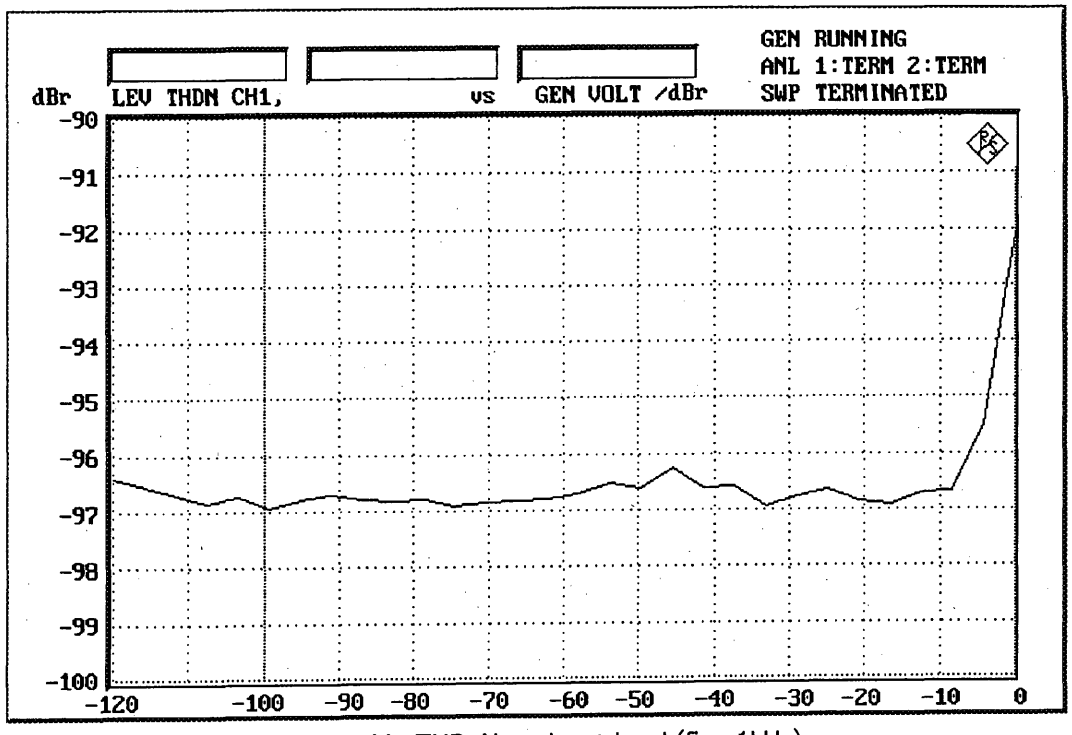


Figure 44 : THD+N vs. Input level (fin : 1kHz)

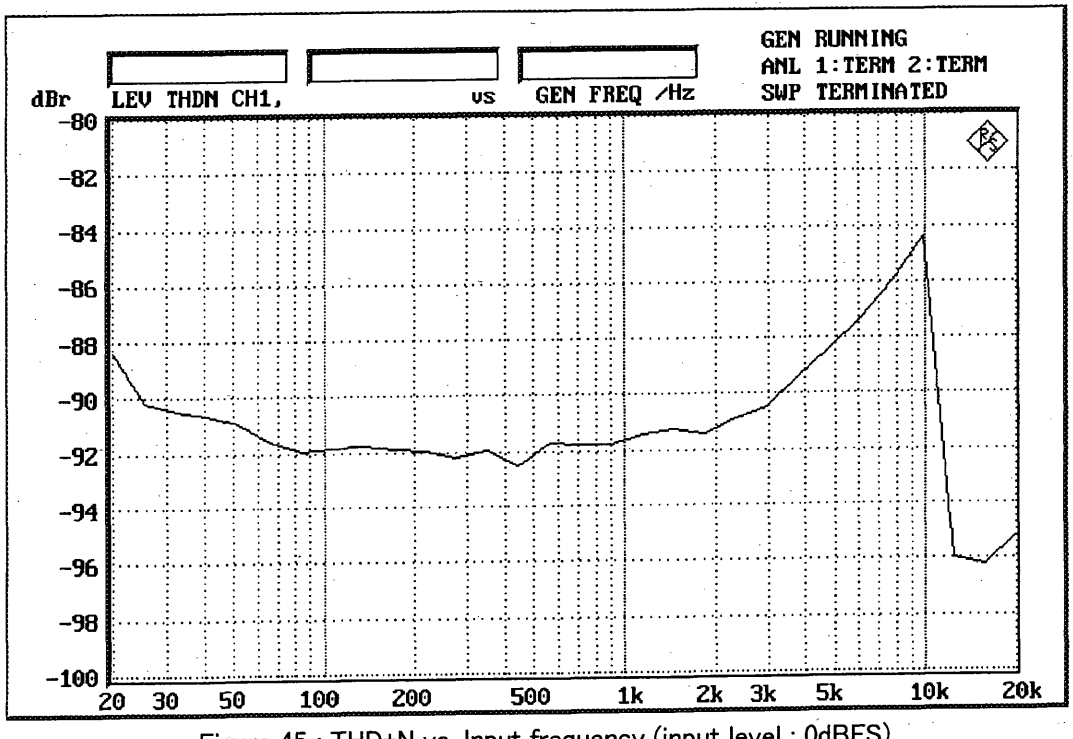


Figure 45 : THD+N vs. Input frequency (input level : 0dBFS)

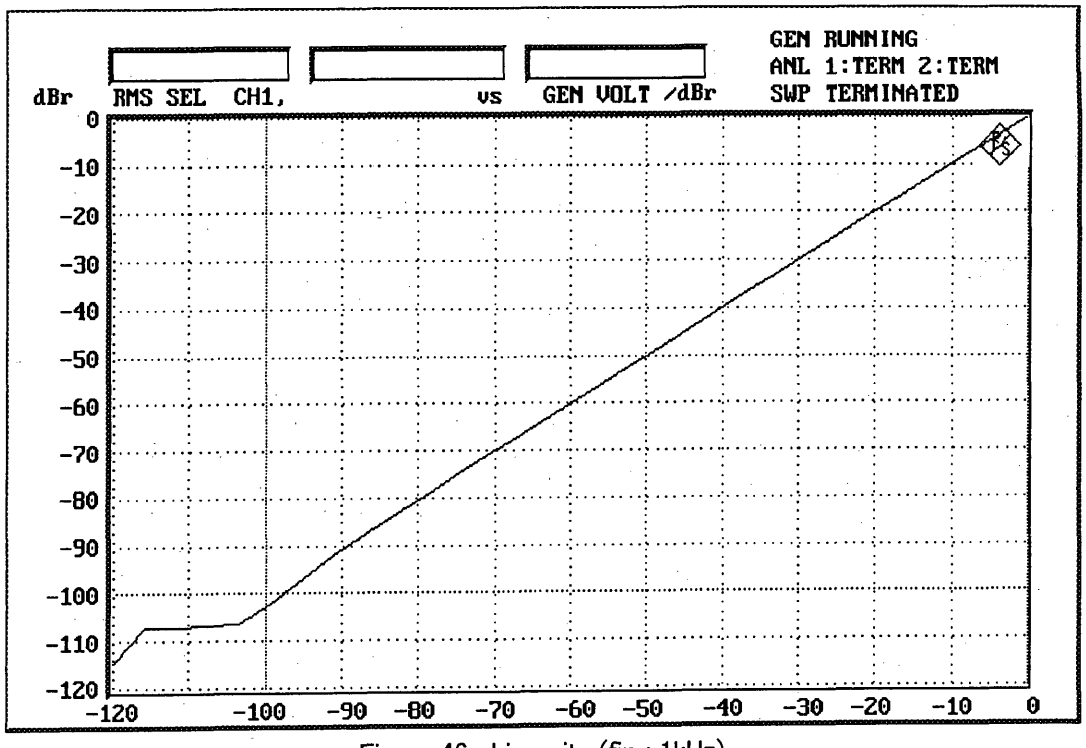


Figure 46 : Linearity (fin : 1kHz)

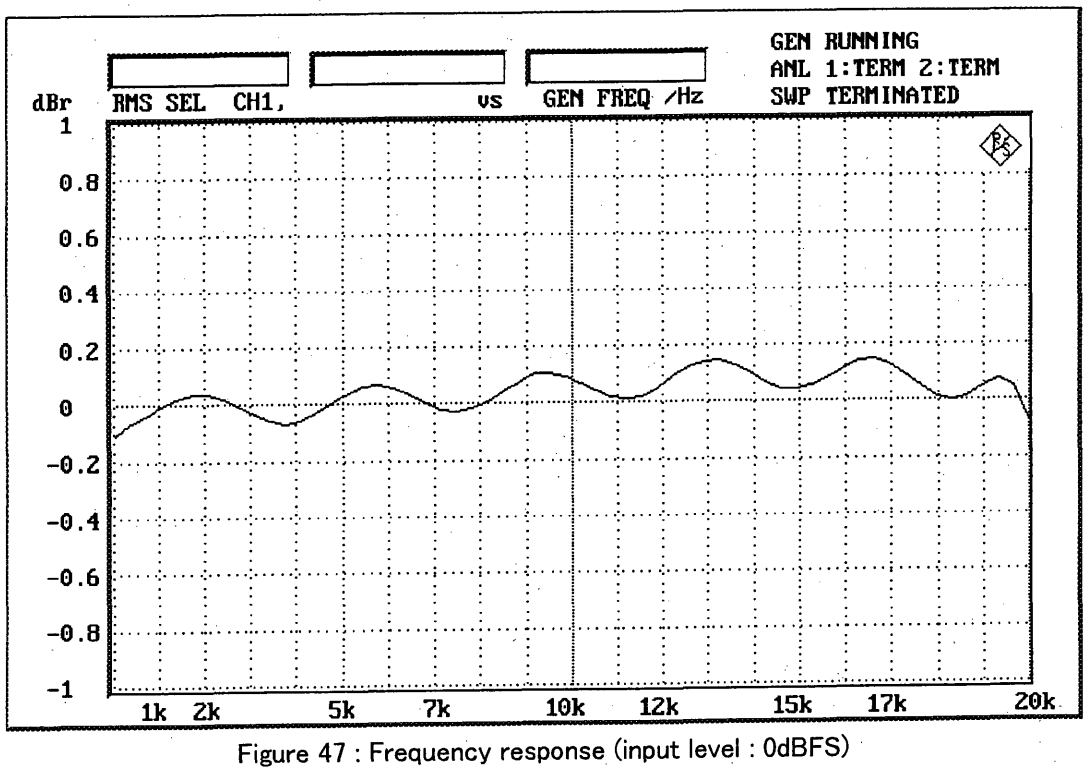


Figure 47 : Frequency response (input level : 0dBFS)

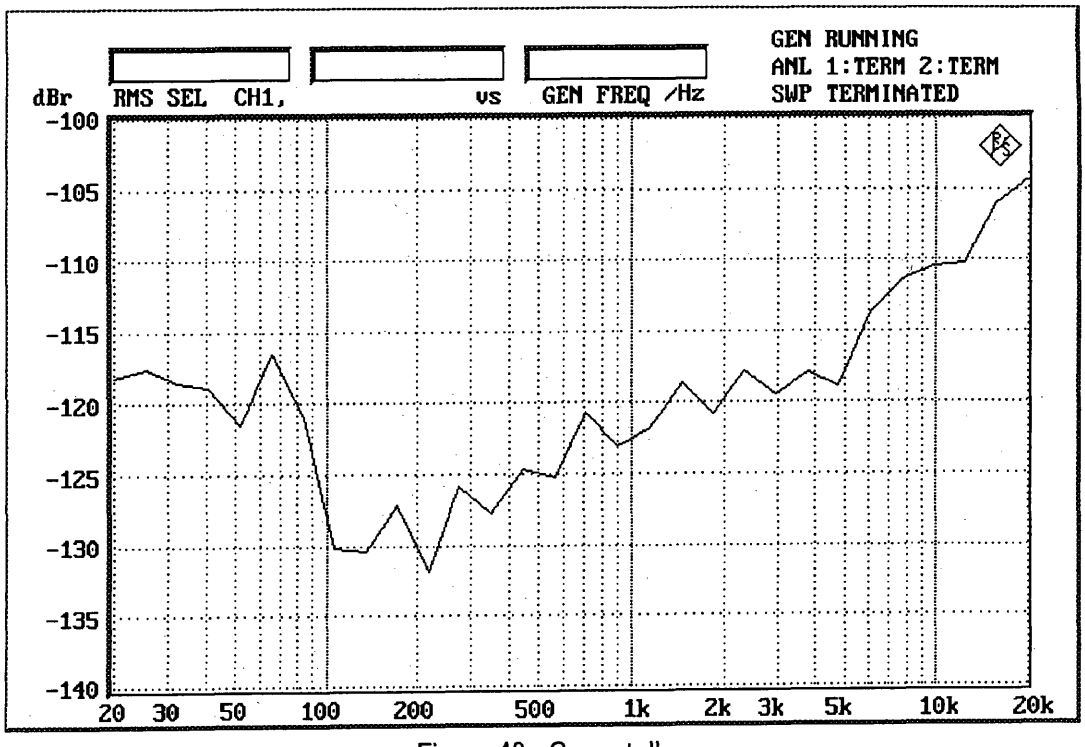


Figure 48 : Cross talk

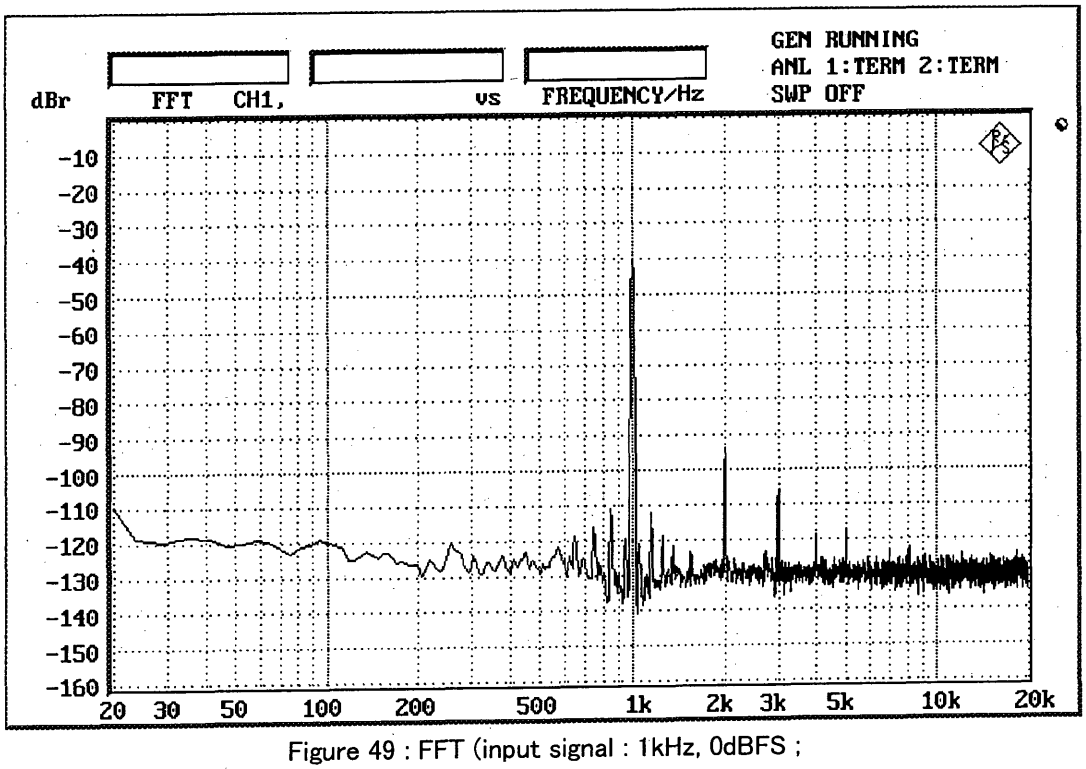


Figure 49 : FFT (input signal : 1kHz, 0dBFS ;
FFT points : 8192, averaging : 10, 30dBFS Notch filter : on)

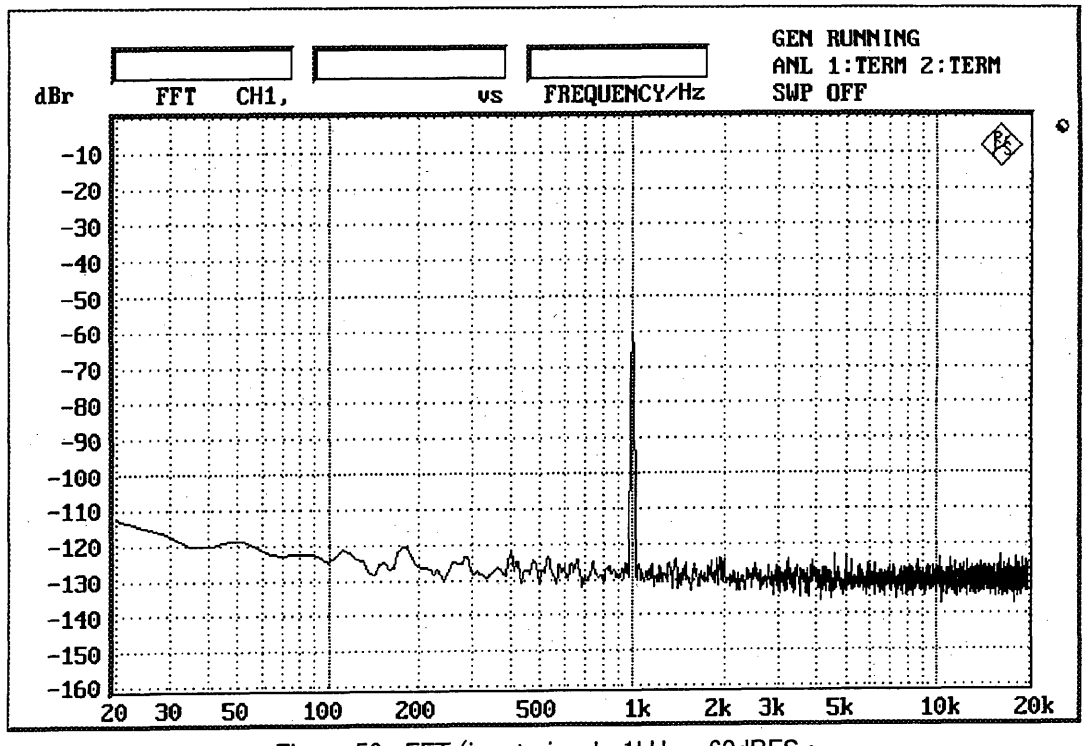


Figure 50 : FFT (input signal : 1kHz, −60dBFS ;
FFT points : 8192, averaging : 10, 30dBFS Notch filter : off)

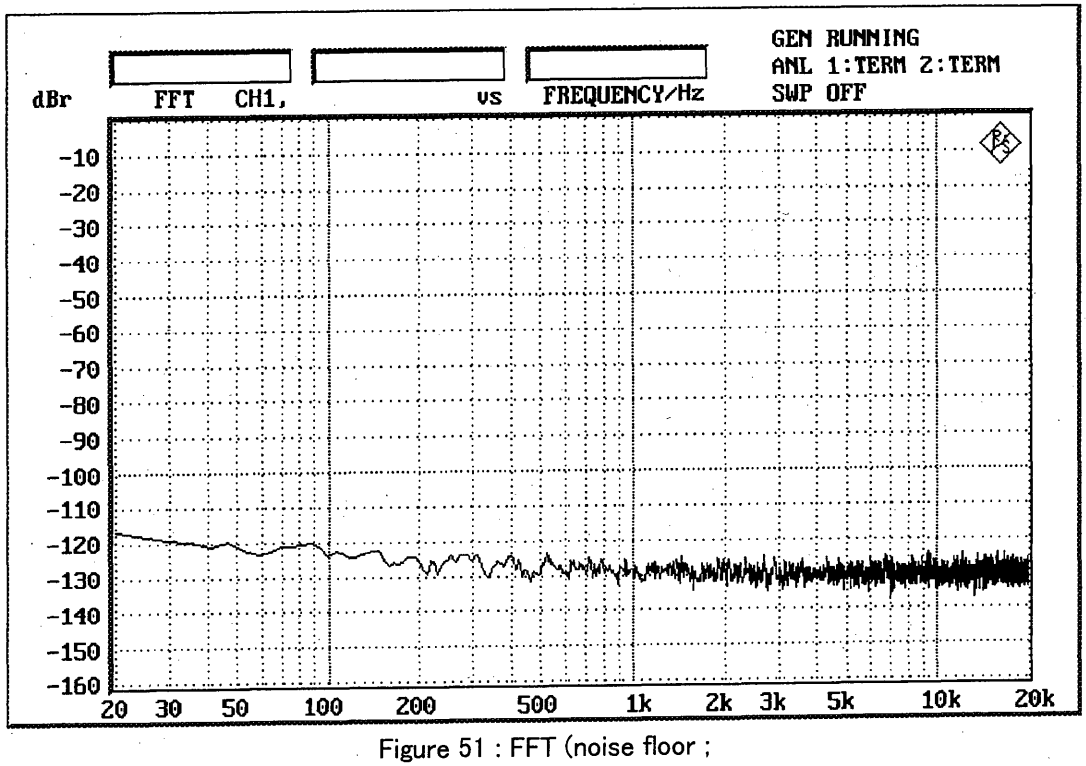


Figure 51 : FFT (noise floor ;
FFT points : 8192, averaging : 10, 30dBFS Notch filter : off)

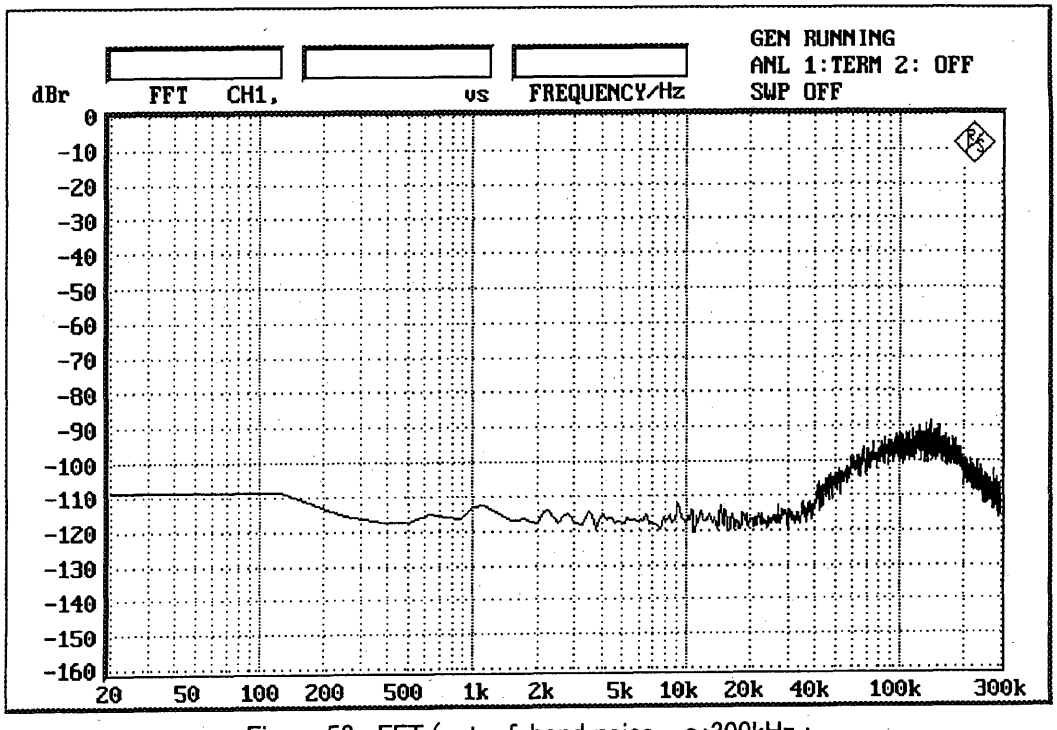
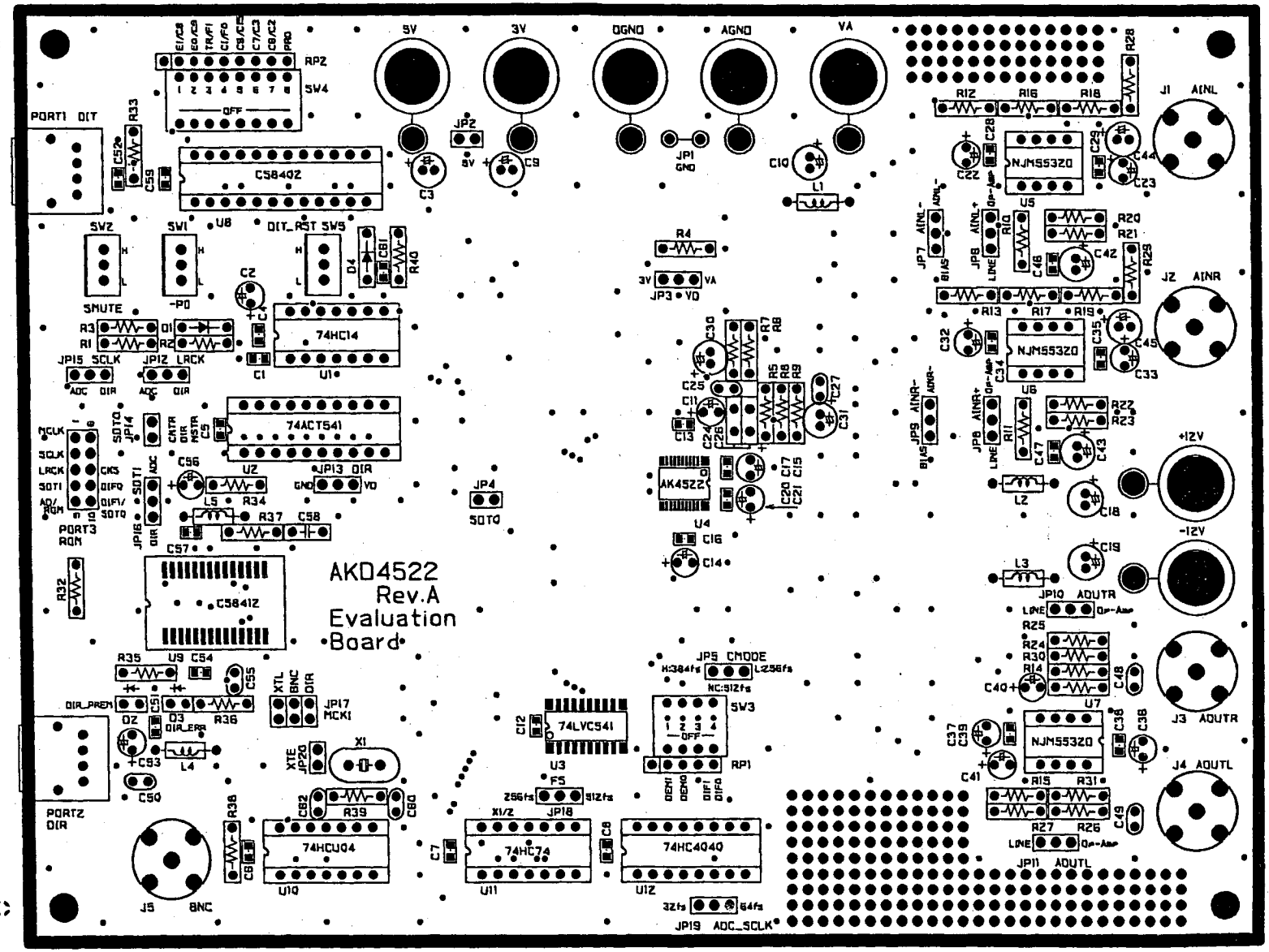
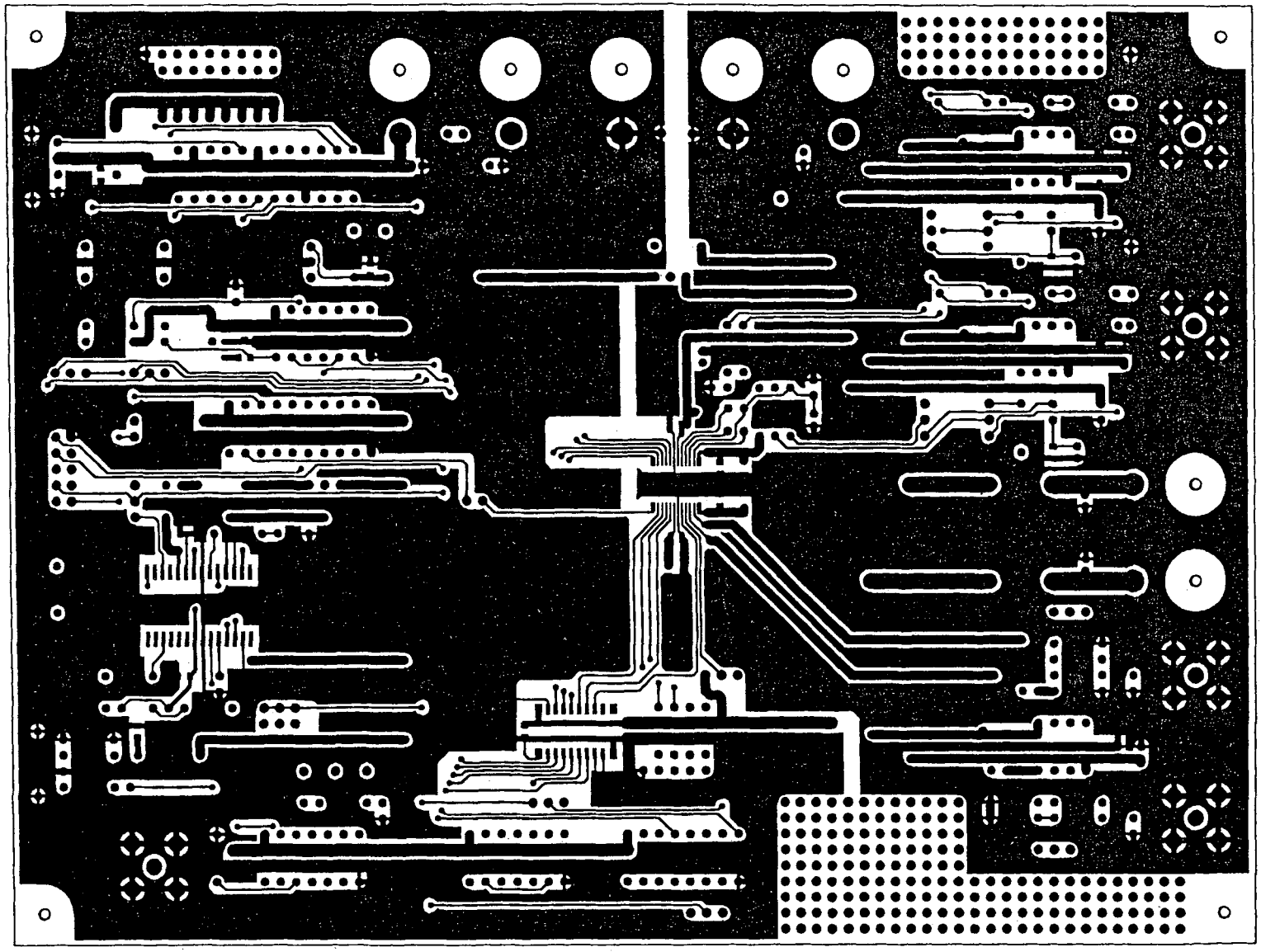


Figure 52 : FFT (out-of-band noise ~300kHz ;
FFT points : 8192, averaging : 10)



L1 部品面　　レジスト シルク　AKD4522 Rev.A



L1 部品面 パターン　　AKD4522 Rev.A

L2 半田面 パターン　　AKD4522 Rev.A

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