T-46-13-29

Am27H256

32,768 x 8-Bit High Speed CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Industry's fastest**
  - -35ns 256K-bit CMOS EPROM
- **Pin compatible with Am27C256**
- **High speed Flashrite™ programming**
  - -Typically less than 5 seconds
- **Versions available in industrial and military temperature ranges**
- **± 10% power supply tolerance available**

GENERAL DESCRIPTION

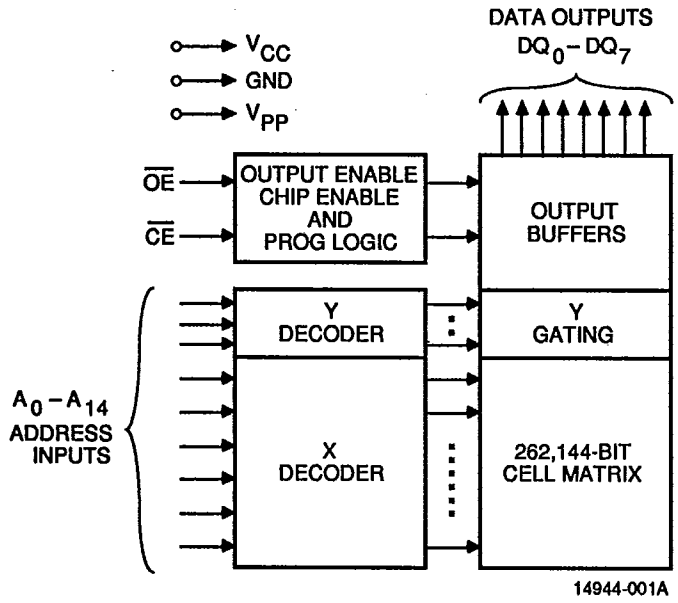
The Am27H256 is an ultra-high speed 256K-bit CMOS UV EPROM. It utilizes the standard JEDEC pinout making it functionally compatible with the Am27C256, but with significantly faster access capability. This superior random access capability results from a focused high-speed design implemented with AMD's advanced CMOS process technology. This offers users bipolar speeds with higher density, lower cost and proven reliability.

This device is ideal for use with the fastest processors. At 35ns, the Am27H256 completely eliminates performance-draining wait states without using bank-interleaving and caching techniques. Designers may take full advantage of high speed digital signal processors and microprocessors by allowing code to be executed at full speed directly out of EPROM. Typical applications include laser printers, switching networks, graphics, workstations and digital signal processing.

The Am27H256 supports AMD's Flashrite programming algorithm which allows the entire chip to be programmed in typically less than 5 seconds.

It is available in DIP as well as surface mount packages and is offered in commercial, industrial, and extended temperature ranges.

BLOCK DIAGRAM



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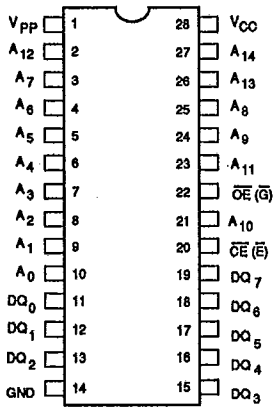
PRODUCT SELECTOR GUIDE

Family Part No.	Am27H256			
Ordering Part No:				
$V_{CC} \pm 5\%$	-35V05	–	–	–
$V_{CC} \pm 10\%$	-35	-45	-55	-70
Max. Access Time (ns)	35	45	55	70
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	35	45	55	70
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	20	20	25	35

CONNECTION DIAGRAMS

Top View

DIPs



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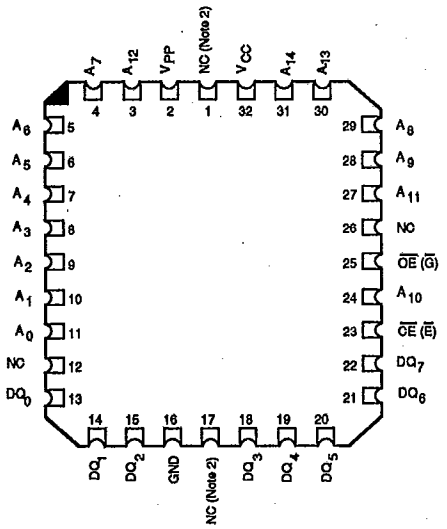
LCC*



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Notes:

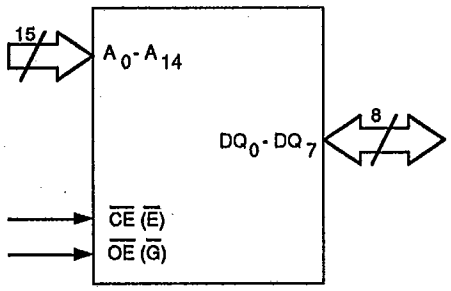
1. JEDEC nomenclature is in parentheses.
2. Don't Use (DU) for PLCC.

* Also available in 32-pin rectangular plastic leaded chip carrier

PIN DESCRIPTION

$A_0 - A_{14}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection

LOGIC SYMBOL



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ORDERING INFORMATION
Standard Information

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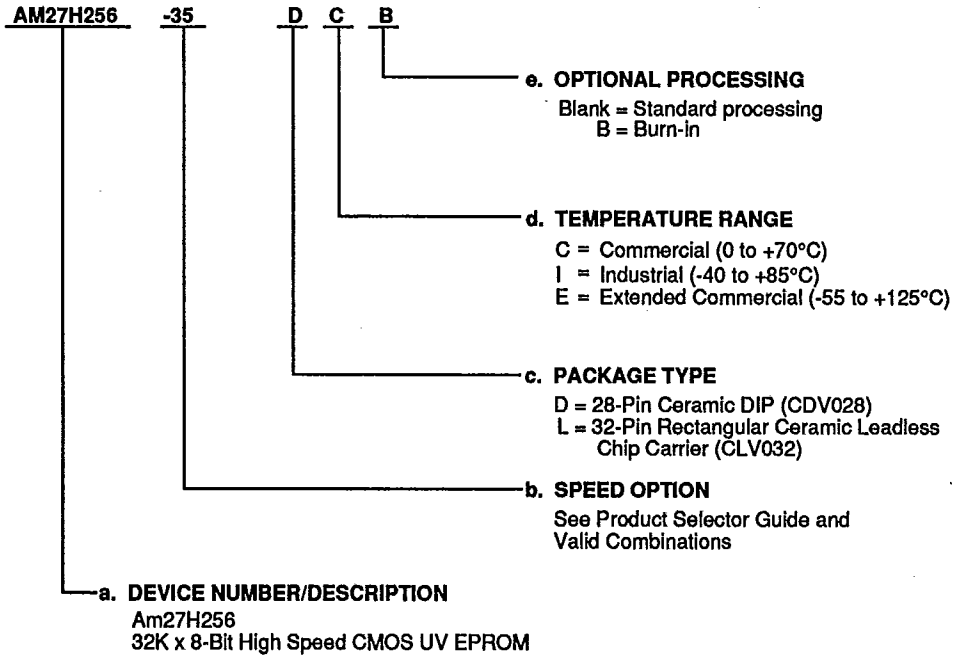
AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27H256-35 AM27H256-35V05	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27H256-45 AM27H256-55 AM27H256-70	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

ORDERING INFORMATION (Cont'd.)

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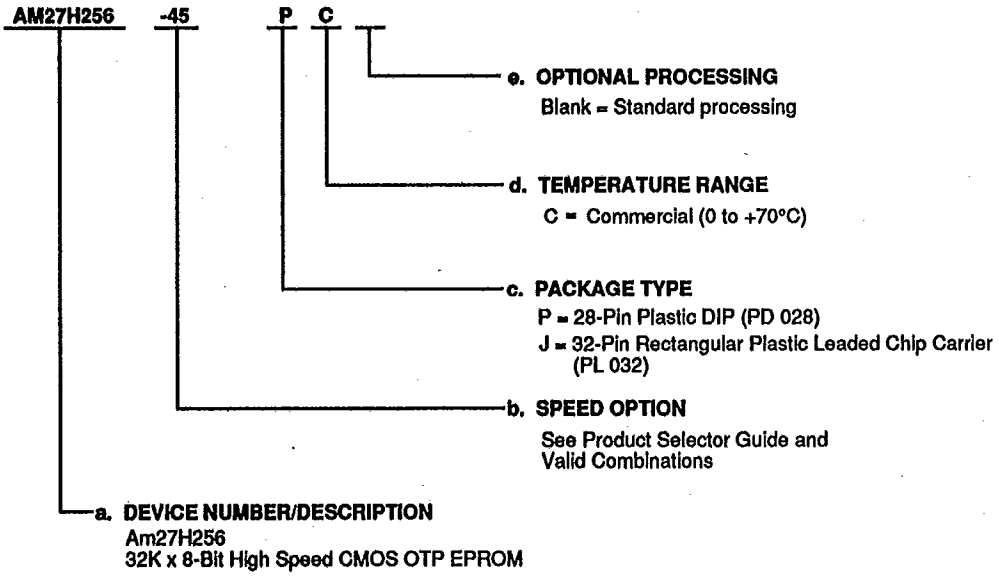
OTP Products (Preliminary)

OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27H256-45	PC, JC
AM27H256-55	
AM27H256-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

ORDERING INFORMATION (Cont'd.)

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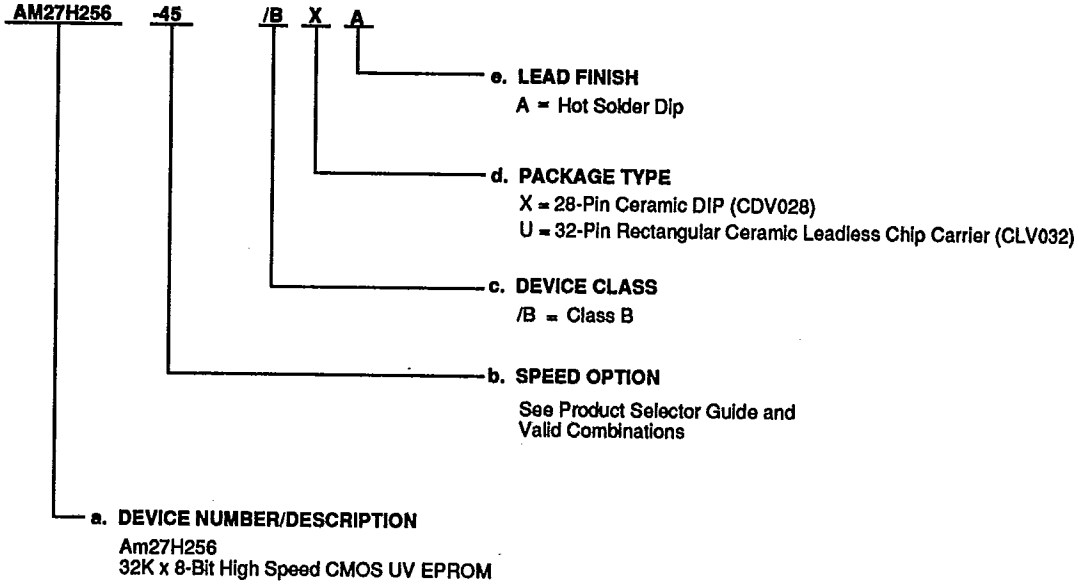
APL Products

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27H256-45	/BXA, /BUA
AM27H256-55	
AM27H256-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27H256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27H256 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27H256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm² for 15 to 20 minutes. The Am27H256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27H256, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27H256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27H256

Upon delivery, or after each erasure, the Am27H256 has all bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27H256 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied 8 bits in parallel to the data input/output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27H256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27H256 may be common. A TTL low-level program pulse applied to an Am27H256 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V and $\overline{OE}$ HIGH will program that Am27H256. A high-level $\overline{CE}$ input inhibits the other Am27H256 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27H256.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27H256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1($A_0 = V_{IH}$), the device identifier code. For the Am27H256, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27H256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27H256 has a standby mode which reduces the maximum V_{CC} current to 50% of the active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27H256 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in

their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

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MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	A_9	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Standby		V_{IH}	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	V_{CC}	01H
(Note 3 & 5)	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	10H

Notes:
1. V_H = 12.0 V ± 0.5 V
2. X = Either V_{IH} or V_{IL}
3. $A_1 - A_8 = A_{10} - A_{14} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.
5. The Am27H256 uses the same Flashrite algorithm during program as the Am27C256.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
OTP product	–65 to 125°C
All other products	–65 to 150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC}	–0.6 to V_{CC} +0.5 V
A_9 and V_{PP}	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Minimum DC voltage on input or I/O is –0.5 V. During transitions, the inputs may overshoot GND to –2.0V for periods of up to 10 ns. Maximum DC voltage on input and I/O is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.
2. For A_9 and V_{PP} the minimum DC input is –0.5 V. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 10 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27H256-XXV05	+4.75 to + 5.25 V
V_{CC} for Am27H256-XX	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

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Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA			0.45	V
V_{IH}	Input HIGH Voltage (Note 9)			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (Note 9)			−0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to + V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to + V_{CC}			10	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C Devices		50	mA
			I/E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	C Devices		25	mA
			I/E/M Devices		35	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Capacitance (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV028		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	10	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	10	10	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	6	9	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27H256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 10 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods less than10 ns.
9. Tested under static DC conditions.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, & 4) (for APL Products, Group A, Subgroups 9, 10, and 11 are specified unless otherwise noted)

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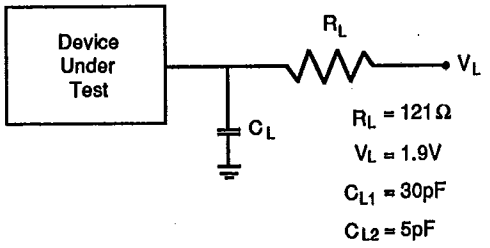
Parameter Symbols		Parameter Description	Test Conditions		Am27H256				Unit
JEDEC	Standard				-35, -35V05	-45	-55	-70	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	35	45	55	70	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	35	45	55	70	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	20	20	25	35	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, Whichever Comes First, to Output Float	$C_L = C_{L2}$	Min.	0	0	0	0	ns
				Max.	20	20	25	35	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occured First		Min.	0	0	0	0	ns
				Max.	–	–	–	–	

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27H256 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C = C_L$
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0 to 3 V
   Timing Measurement Reference Level – 1.5 V for inputs and outputs

SWITCHING TEST CIRCUIT



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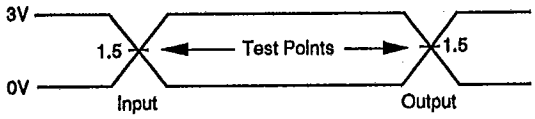
SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤5 ns.

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KEY TO SWITCHING WAVEFORMS

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WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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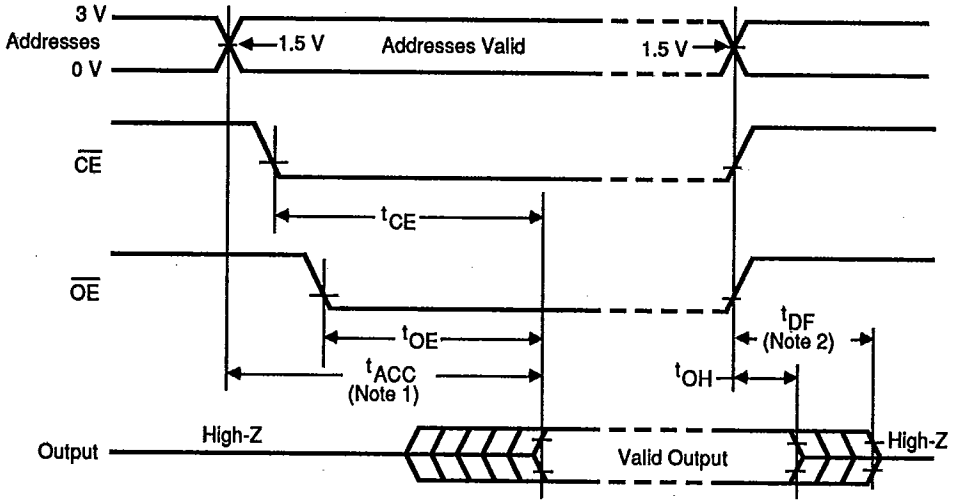
SWITCHING WAVEFORMS



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Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.