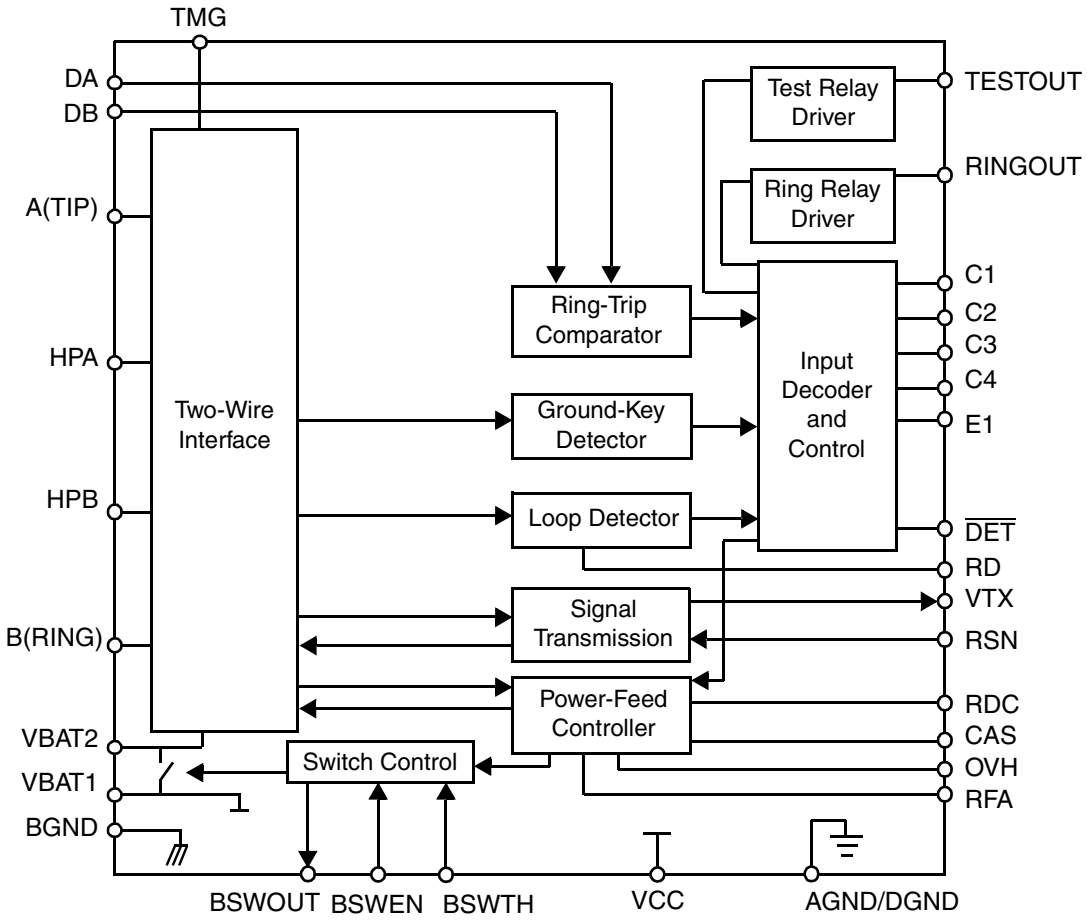
Am79489

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Ideal for low power sensitive applications**
- **Low standby power (normal and reverse)**
- **Automatic on-chip battery switching**
- **On-chip thermal management**
- **On-chip thermal shutdown**
- **–20 V to –60 V battery operation**
- **Programmable current limit**
- **Programmable resistive feed**
- **Programmable loop-detect threshold**
- **Selectable overhead for metering applications**
- **Two-wire impedance set by single external impedance**
- **On-chip ring and test relay drivers and relay snubber circuits**
- **Polarity reversal (full transmission)**
- **Loop and ground-key detector**
- **Comparator for ring-trip detection**
- **Ground-start capability**
- **On-hook transmission**

BLOCK DIAGRAM

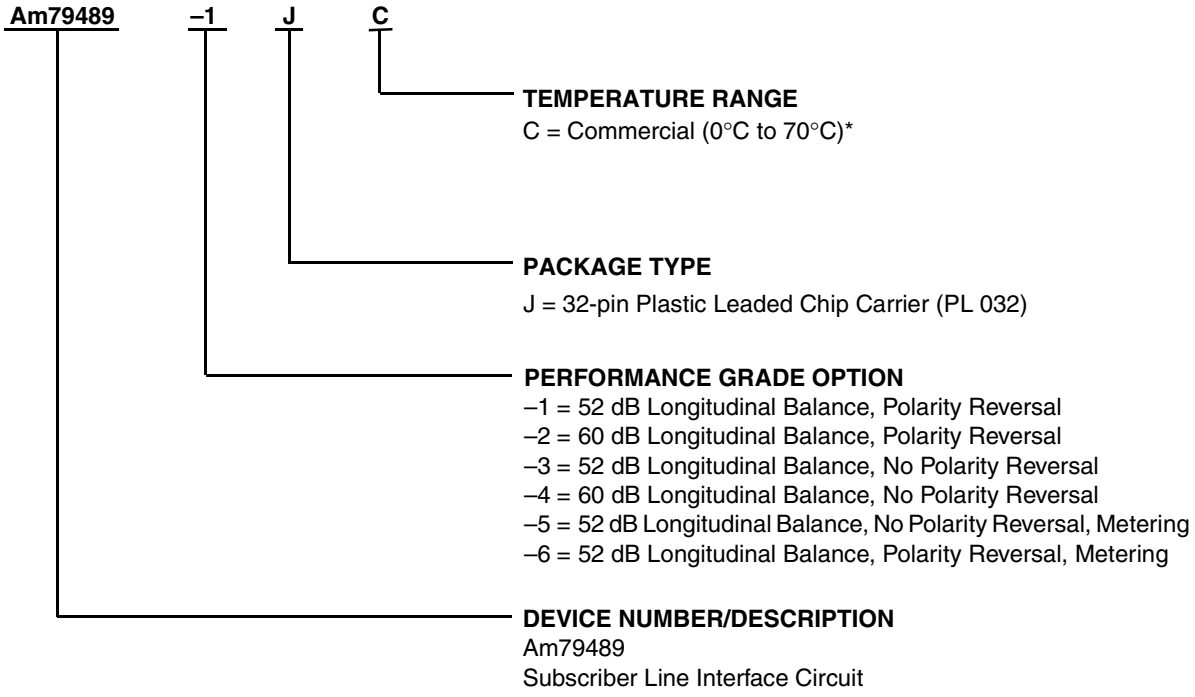


Publication# **080201** Rev: **E** Amendment: **/0**
Issue Date: **October 1999**

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79489	–1 –2 –3 –4 –5 –6	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations and to check on newly released combinations, and to obtain additional data on Legerity's standard military–grade products.

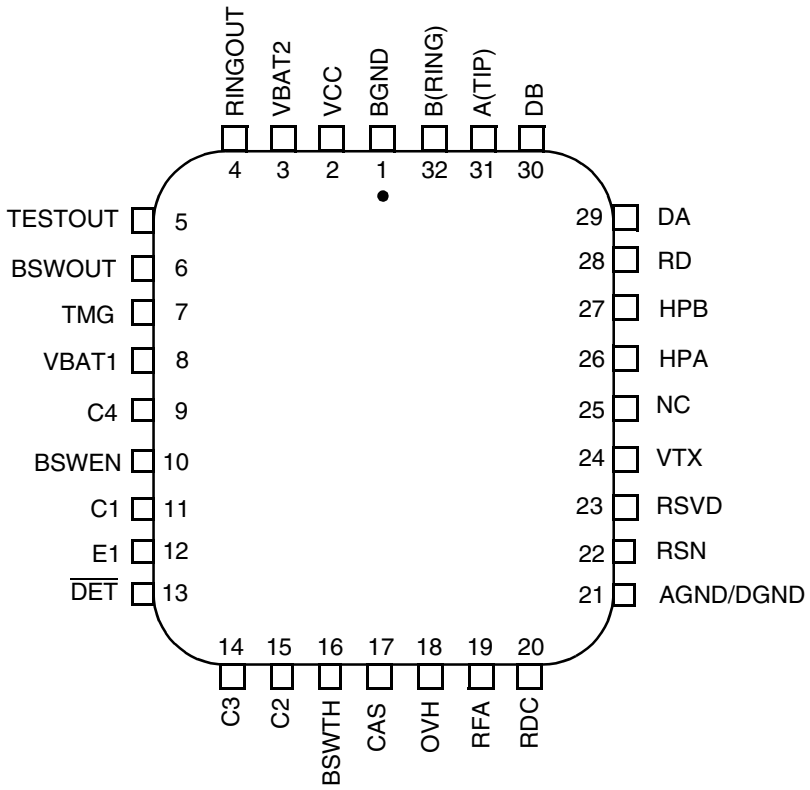
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM

Top View

32-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No Connect*
3. *RSVD = Reserved. Do not connect to this pin.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
BSWEN	—	Battery Switch Control. Internally connected to automatic battery switch circuitry. BSWEN can be overridden by external logic. BSWEN Low connects VBAT1 to VBAT2. BSWEN High disconnects VBAT1 from VBAT2.
BSWOUT	Output	Buffered Output. Internally connected to battery switch circuitry. The output is open-collector with a built-in pull-up resistor. BSWOUT Low indicates VBAT1 is connected to VBAT2. BSWOUT High indicates VBAT1 is disconnected from VBAT2. This output is valid only in the Active states.
BSWTH	Input	Input for setting automatic battery switch threshold. Normally tied to Battery 2. Tie to ground for manual switching.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
C4	Input	Test Relay Input – Active Low. 1 = Off. 0 = On.
CAS	Capacitor	Anti-sat pin for capacitor to filter reference voltage when operating in anti-sat region.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-Key Detect Select. E1 = 1 selects the hook switch detector. E1 = 0 selects the ground-key detector. In the Tip Open state, ground key is selected independent of E1.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. This pin not internally connected.
OVH	Input	Overhead Control. Logic High enables minimized nonmetering overhead. Logic Low enables 2.2 V metering DC overhead. TTL-compatible.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). Connection point for the DC feed current programming network. The other end of the network connects to RSN. V_{RDC} is negative for normal polarity and positive for reverse polarity.
RFA	—	Resistive feed adjust. Adjust the DC feed resistance gain coefficient, GDC, with external resistor connected to ground.
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
RSVD	—	Reserved. These pins are reserved for Legerity use. Make no connection to these pins.
TESTOUT	Output	Test Relay Driver. Open collector driver with emitter internally connected to AGND.
TMG	—	Thermal Management. External resistor connects this pin to VBAT2 to offload power dissipation from SLIC. Functions during normal polarity, Active state.
VBAT1	Battery	Most negative battery supply and substrate connection.
VBAT2	Battery	Battery supply for output power amplifiers. Switched to VBAT1 by BSWEN.
VCC	Power	+5 V power supply.
VTX	Output	Transmit Audio. This output is a 0.5066 unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

With respect to AGND/DGND:

V_{CC} . . . . . –0.4 V to +7.0 V

V_{BAT1}

Continuous . . . . . +0.4 V to –70 V

10 ms . . . . . +0.4 V to –75 V

V_{BAT2} and BSWTH . . . . . +0.4 V to V_{BAT1}

BGND . . . . . +3 V to –3 V

A(TIP) or B(RING) with respect to BGND:

Continuous . . . . . V_{BAT1} to +1 V

10 ms (f = 0.1 Hz) . . . . . –70 V to +5 V

1 µs (f = 0.1 Hz) . . . . . –80 V to +8 V

250 ns (f = 0.1 Hz) . . . . . –90 V to +12 V

Current from A(TIP) or B(RING) . . . . . ±150 mA

TESTOUT/RINGOUT/current . . . . . 80 mA

TESTOUT/RINGOUT/voltage . . . . . BGND to +7 V

TESTOUT/RINGOUT/transient . . . . . BGND to +10 V

DA and DB inputs

Voltage on ring-trip inputs . . . . . V_{BAT1} to 0 V

Current on ring-trip inputs . . . . . ±10 mA

C4–C1, BSWEN, OVH, E1

Input voltage . . . . . –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous

T_A = 70°C, No heat sink (see note):

In 32-pin PLCC package . . . . . 1.7 W

Thermal data . . . . . θ_{JA}

In 32-pin PLCC package . . . . . 43°C/W typ

ESD immunity/pin (HBM) . . . . . 1500 V

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations section for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . –40°C to +85°C*

V_{CC} . . . . . 4.75 V to 5.25 V

BAT1 . . . . . –40.5 V to –60 V

BAT2 . . . . . –20 V to BAT1

AGND/DGND . . . . . 0 V

BGND with respect to GND . . . –100 mV to +100 mV

Load resistance on VTX to GND . . . . . 20 kΩ min

Operating ranges define those limits over which the functionality of the device is guaranteed by production testing.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss (See Test Circuit D)	200 Hz to 3.4 kHz	26			dB	4, 6
Analog output (V_{TX}) impedance			3	20	Ω	4
Analog output (V_{TX}) offset voltage		–50		+50	mV	
Overload level, 2-wire	Active state	2.5			Vpk	2a, 3
	Active state, OVH = 0 –5, –6*	7				
Overload level	Open loop, R_{LAC} = 900 Ω, OVH = 0 –5, –6*	3.86			Vrms	2b, 3
THD, Total Harmonic Distortion	0 dBm		–64	–50	dB	3
	+7 dBm		–55	–40		
THD, open loop	0 dBm, R_{LAC} = 600 Ω			–36		4
Longitudinal Capability (See Test Circuit C)						
Longitudinal to metallic L-T 200 Hz to 1 kHz	Normal and reverse polarity –1, –6*	52			dB	8
	Normal polarity –3, –5	52				
	Normal polarity 0°C to +70°C –2, –4	60				
	Normal polarity –40°C to +85°C –2, –4	58				
	Reverse polarity –40°C to +85°C –2	54				
Longitudinal to metallic L-T 1 kHz to 3.4 kHz	Normal and reverse polarity –1, –6*	52				
	Normal polarity –3, –5	52				
	Normal polarity 0°C to +70°C –2, –4	54				
	Normal polarity –40°C to +85°C –2, –4	54				
	Reverse polarity –40°C to +85°C –2	54				
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40			dB	
Longitudinal current per pin (A or B)	Active state	15	27		mArms	7
Longitudinal impedance at A or B	0 to 100 Hz		25		Ω/pin	4
Longitudinal Induction				23	dBrnc	4
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω		+7	+12	dBrnC	4, 8
Psophometric weighted noise	R_L = 600 Ω		–83	–78	dBmp	8
Insertion Loss (See Test Circuits A and B)						
Gain, 4- to 2-wire	0 dBm, 1 kHz 0°C to 70°C	–0.15	0	+0.15	dB	
	0 dBm, 1 kHz –40°C to 85°C	–0.20	0	+0.20		4
Gain, 2- to 4-wire, 4-to-4-wire	0 dBm, 1 kHz 0°C to 70°C	–6.05	–5.90	–5.75		
	0 dBm, 1 kHz –40°C to 85°C	–6.10	–5.90	–5.70		4
Gain, 4- to 2-wire	Open loop	–0.35		+0.35		4
Gain, 2- to 4-wire, 4- to 4-wire	Open loop	–6.25	–5.90	–5.55		4
Gain over frequency	300 to 3.4 kHz, relative to 1 kHz	–0.10		+0.10		
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.10		+0.10		
Gain tracking open loop	0 dB to –15 dB	–0.35		+0.35		4
Group delay	0 dBm, 1 kHz		4		µs	4, 6

Note:
** P.G. = Performance Grade*

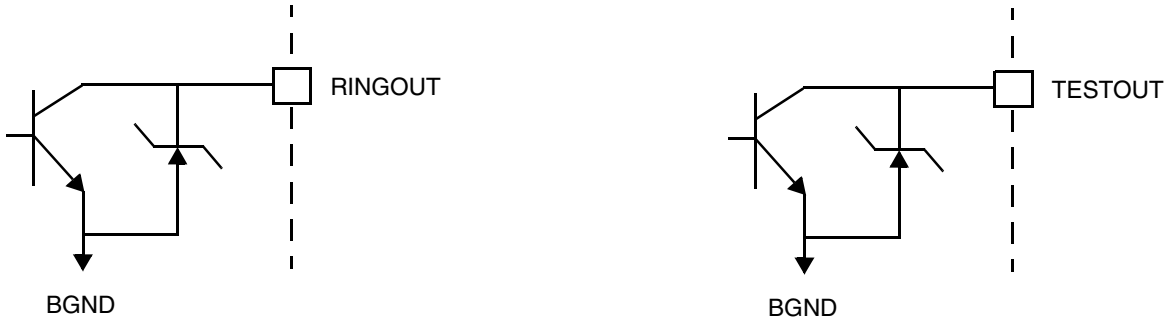
ELECTRICAL CHARACTERISTICS (CONTINUED)

Description		Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics							
I_L, Active	Short loop	R_{LDC} = 250 Ω	44.2	48.6	54.0	mA	
	Medium loop	R_{LDC} = 700 Ω	33.4	37.1	40.8		
	Long loop	R_{LDC} = 2 kΩ	17.2	19.2	21.2		
I_L, Active OVH = 0	Short loop	R_{LDC} = 250 Ω	44.2	48.6	54.0		
	Medium loop	R_{LDC} = 700 Ω –5, –6*	33.4	37.1	40.8		
	Long loop	R_{LDC} = 2 kΩ	16.0	18.0	20.0		
I_L, Accuracy, Standby state		$I_L = \frac{\lvert V_{BAT1} \rvert - 3\ V}{R_L + 400}$ T_A = 25°C	0.7 I_L	I_L	1.3 I_L		
		Current limited region	18	30			
I_L, Loop current, Disconnect state		R_L = 0			100	µA	
I_LLIM		Active, A and B to GND		95	135	mA	
$V_{apparent}$				52		V	4
V_{AB}, Open loop voltage		Active, Normal	40.3	41.7			
		Reverse Polarity	39.8	41.7			
		OVH = 0	37	39			
BAT SW hysteresis				1150		mV	
BAT SW threshold				BAT2 + 8.5		V	
(from V_{BAT1} to V_{BAT2})		OVH = 0 –5, –6*		BAT2 + 11.7			
I_A, Leakage, Tip Open state		R_L = 0			100	µA	
I_B, Current, Tip Open state		B to GND	18	30	56	mA	
V_A, Active		RA to BAT1 = 7 kΩ, RB to GND = 100 Ω	–7.5	–5		V	4
Power Supply Rejection Ratio (Vripple = 100 mVrms), Active Normal State							
V_{CC}		50 Hz to 3.4 kHz	30	45		dB	3
V_{BAT1}		50 Hz to 3.4 kHz	28	50			
V_{BAT2}		50 Hz to 3.4 kHz	35	50			4
V_{BAT1}, Open loop, R_{LAC} = 600 Ω (Anti-sat region)		50 Hz	8	14			4
		100 Hz	15	22			
		200 Hz	20	29			
		500 Hz to 3.4 kHz	28	40			
Effective internal resistance		CAS pin to GND	85	170	255	kΩ	4
Device Power Dissipation							
Open loop, Disconnect state				35	70	mW	
Open loop, Standby state				50	85		
Open loop, Active state		OVH = 1		150	250		
Open loop, Active state		OVH = 0		550	620		9
Off hook, Standby state		R_L = 600 Ω		1000	1300		
Off hook, Active state		R_L = 250 Ω		880	1200		
		R_L = 700 Ω		800	1000		

ELECTRICAL CHARACTERISTICS (CONTINUED)

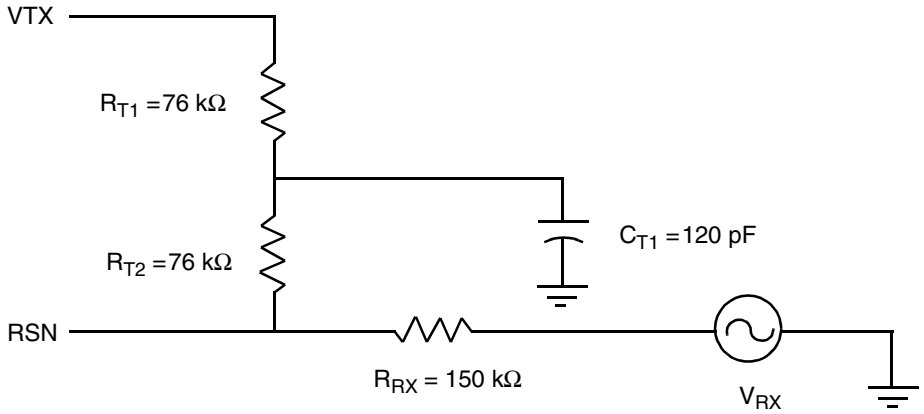
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents, Battery						
I_{CC}, Open Loop V_{CC} supply current	Disconnect state Standby state Active state		2.5 3.0 6.3	4.5 4.5 9.5	mA	
I_{BAT1}, Open Loop V_{BAT1} supply current	Disconnect state Standby state Active state		0.5 0.7 2.8	1.0 1.5 4.8	mA	
RFI Rejection						
RFI rejection	100 kHz to 30 MHz (See Figure E)			0.7	mVrms	4
Logic Inputs (C4–C1, E1, BSWEN, OVH [–5, –6 only])						
V_{IH}, Input High voltage C3 C1, C2, C4, BSWEN, OVH, E1		 2.5 2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current C4–C1, OVH, E1		–75		40	µA	
I_{IH}, Input High current, BSWEN		–75		1200		
I_{IL}, Input Low current, except C1		–400				
I_{IL}, Input Low current, C1		–600	–300			
Logic Output ($\overline{DET}$, BSWOUT)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.05 mA	2.4				
Ring-Trip Comparator Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	5
Loop Detector						
I_T, Loop-detect threshold tolerance	Active state, Off-hook to On-hook R_D = 35.4 kΩ, I_T = 368/R_D On-hook to Off-hook R_D = 35.4 kΩ, I_T = 414/R_D	 –15 –20		 +15 +20	%	
	Standby state, Off-hook to On-hook R_D = 35.4 kΩ, I_T = 425/R_D On-hook to Off-hook R_D = 35.4 kΩ, I_T = 471/R_D	 –15 –20		 +15 +20	%	
Loop-detect threshold hysteresis	Active state		1.3		mA	4
	Standby state					
IGK, GND key-detector threshold	R_L from BX to GND Active, Standby, and Tip Open states	5	9	13	mA	
Relay Driver Output (RINGOUT/TESTOUT)						
On voltage	I_{OL} = 40 mA		+0.3	+0.7	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.5		V	
Zener On voltage	I_Z = 40 mA		7.9	10		

RELAY DRIVER SCHEMATICS



Notes:

1. *Unless otherwise specified, test conditions are V_{CC} = +5 V, BAT1 = –50 V, BAT2 = –34 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 5.833 kΩ, R_{TMG} = 570 Ω, R_D = 35.4 kΩ, RFA = 0 Ω, no fuse resistors, C_{HP} = 0.22 µF, C_{DC} = 0.5 µF, C_{CAS} = 0.33 µF, C_{VBAT12} = 220 nF, D_1 = D_2 = 1N400x, OVH = 1, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level exists when THD = 1%.*
   b. Overload level exists when THD = 1.5%.
3. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
6. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the DSLAC™ or QSLAC™ device.*
7. *Minimum current level is guaranteed not to cause a false Loop Detect. The SLIC must be functional in this condition.*
8. *Four-wire performance is 5–9 dB better than the specified two-wire values.*
9. *Open loop, Active state, Metering mode power dissipation may be reduced from a typical of 550 mW to a typical of 150 mW by connecting the $\overline{DET}$ pin to the OVH pin. This connection will force the SLIC into the nonmetering mode while on hook. With this connection, a metering signal sent after the SLIC goes on hook may be distorted on the 2W line because the SLIC is forced into the nonmetering mode. To eliminate this distortion, a delay can be added between the time the SLIC goes on hook and the time the SLIC switches to nonmetering mode by using an RC circuit for the $\overline{DET}$ pin to OVH pin connection.*

Table 1. SLIC Decoding

				$\overline{\text{DET}}$ Output	
State	**C3**	**C2**	**C1**	**2-Wire Status**	**E1 = 1**	**E1 = 0**
0	0	0	0	Standby, Reverse Polarity	Loop detector	GK
1	0	0	1	Reserved	X	X
2	0	1	0	Active, Reverse Polarity	Loop detector	GK
3	0	1	1	Tip Open	GK or loop detector	GK
4	1	0	0	Disconnect	Ring trip	Ring trip
5	1	0	1	Ringing	Ring trip	Ring trip
6	1	1	0	Active, Normal	Loop detector	GK
7	1	1	1	Standby, Normal	Loop detector	GK

Table 2. User-Programmable Components

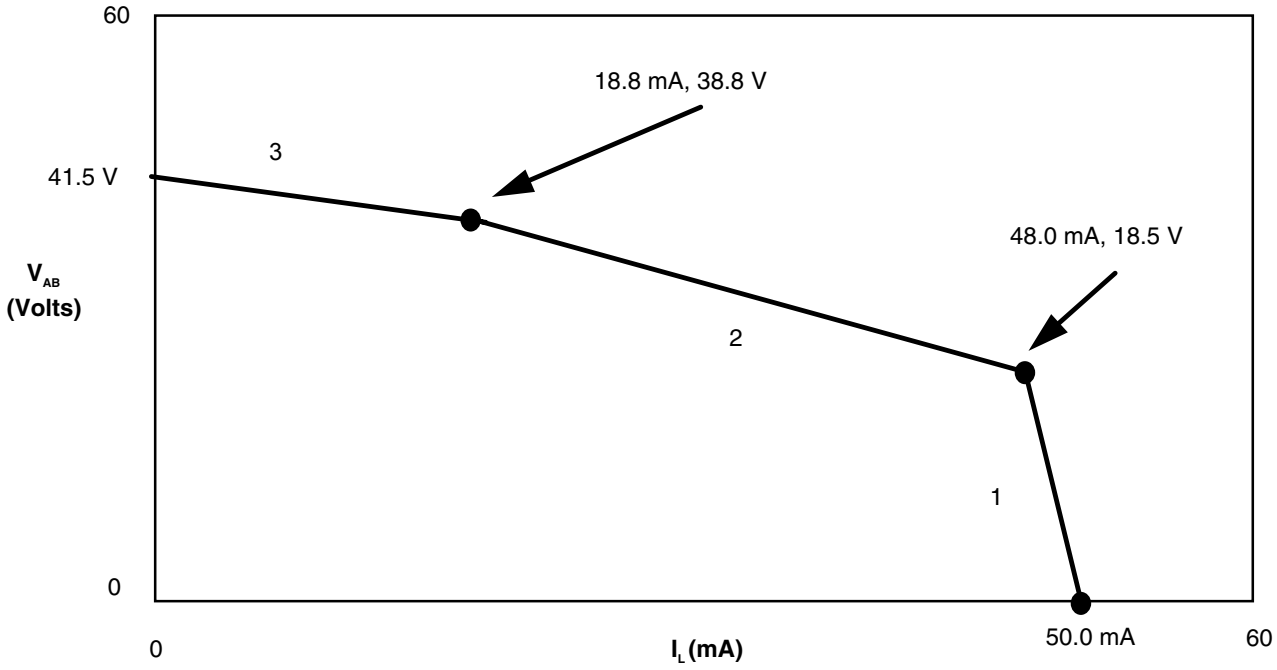
$Z_T = 253(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account. The internal amplifier pole is: $\frac{22\ \text{kHz} \bullet R_{LAC}}{600\ \Omega\ \pm 10\%}$
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500(Z_T)}{Z_T + 253(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain. Z_L is the 2-wire load impedance.
$I_{LIMIT} = \frac{625(GFA)}{R_{DC1} + R_{DC2}}$ $C_{DC} = 1.5\ \text{ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$ $GFA = 0.99 \bullet \frac{(RFA + 30.1\ \text{k}\Omega)}{(RFA + 32\ \text{k}\Omega)}$ $RCL = 1.4 \bullet (R_{DC1} + R_{DC2}) \bullet \frac{(RFA + 60\ \text{k}\Omega)}{(RFA + 100\ \text{k}\Omega)}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LIMIT} is the desired loop current in the constant-current region.
$R_D = \frac{365}{I_T}$, $C_D = \frac{0.5\ \text{ms}}{R_D}$	R_D and C_D form the network connected from R_D to AGND/DGND and I_T is the threshold current between on hook and off hook in the Active state.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cutoff frequency.
$I_{Standby} = \frac{\lvert V_{BAT1} \rvert - 3\ \text{V}}{400\ \Omega + R_L}$	Standby loop current (resistive region).

Table 2. User-Programmable Components (continued)

$C_{BSWEN} = 5\ \mu mhos \bullet T_D(ms)$	C_{BSWEN} is connected from BSWEN to GND for automatic switching. T_D is the delay in switching from BAT1 to BAT2. The delay from BAT2 to BAT1 is about 0.1 T_D.
$R_{FEED} = 2 \bullet R_{FUSE} + \left(\frac{R_{DC1} + R_{DC2}}{GDC}\right)$ $GDC = 47.9\left(\frac{40\ k\Omega + RFA}{120\ k\Omega + RFA}\right)$	The DC feed resistance can be adjusted with a resistance (RFA) from the RFA pin to ground.
Thermal Management Equations (Active, Normal, and Reverse Polarity States)	
$R_{TMG} \geq \frac{\lvert V_{BAT2}\rvert - 6\ V}{I_{LOOPmax}}$ (OVH = 1) $R_{TMG} \geq \frac{\lvert V_{BAT2}\rvert - 7.5\ V}{I_{LOOPmax}}$ (OVH = 0)	R_{TMG} is connected from TMG to VBAT2 and is used to limit power dissipation within the SLIC in Active states only.
$P_{RTMG} = \frac{(\lvert V_{BAT2}\rvert - 6\ V - (I_L \bullet R_L))^2 (R_{TMG})}{(R_{TMG} + 40)^2}$ (OVH = 1) $P_{RTMG} = \frac{(\lvert V_{BAT2}\rvert - 7.5\ V - (I_L \bullet R_L))^2 (R_{TMG})}{(R_{TMG} + 40)^2}$ (OVH = 0)	Power dissipated in the thermal management resistor, R_{TMG}, during the Active states.
$P_{SLIC} = (\lvert V_{BAT2}\rvert \bullet I_L) - P_{RTMG} - R_L \bullet (I_L)^2 + 0.22\ W$	Power dissipated in the SLIC while in the Active states.

DC FEED CHARACTERISTICS

$R_{DC} = R_{DC1} + R_{DC2} = 11.67\ k\Omega$, RFA = 0 Ω, No fuse resistors, OVH = 1, BAT1 = –50 V



Notes:

Graph is for illustration only.

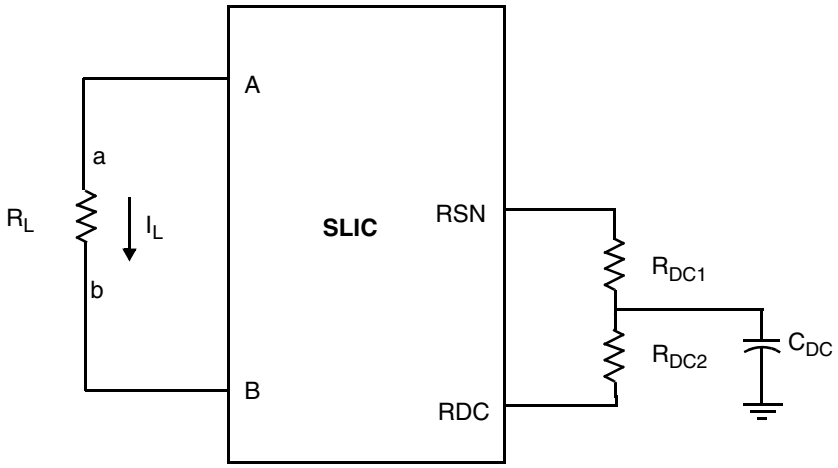
1. $V_{AB} = I_{LIMIT} \bullet RCL - I_L \bullet RCL$

2. $V_{AB} = 52\ V - I_L\left(\frac{RDC}{GDC}\right)$

3a. $V_{AB} = 0.8|V_{BAT1}| + 2.2 - I_L\left(\frac{RDC}{5 \bullet GDC}\right), OVH = 1$

3b. $V_{AB} = 0.8|V_{BAT1}| - 1.0 - I_L\left(\frac{RDC}{5 \bullet GDC}\right), OVH = 0$

a. Load Line (Typical)

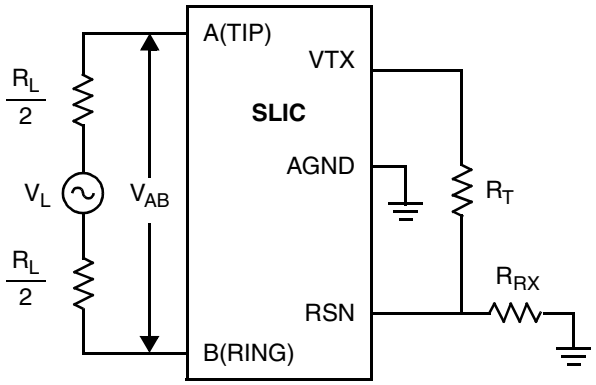


Feed current programmed by R_{DC1} and R_{DC2}

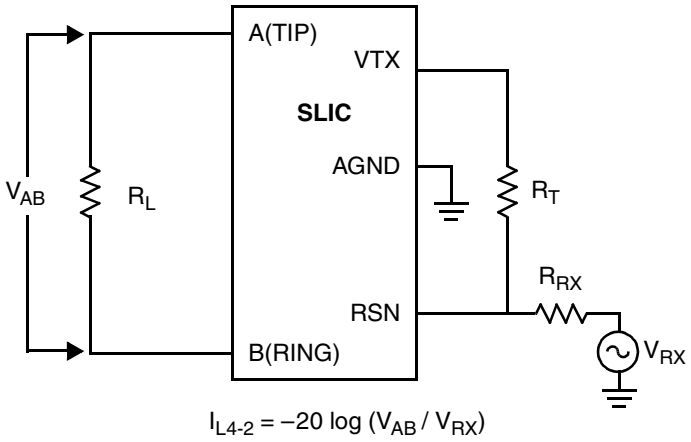
b. Feed Programming

Figure 1. DC Feed Characteristics

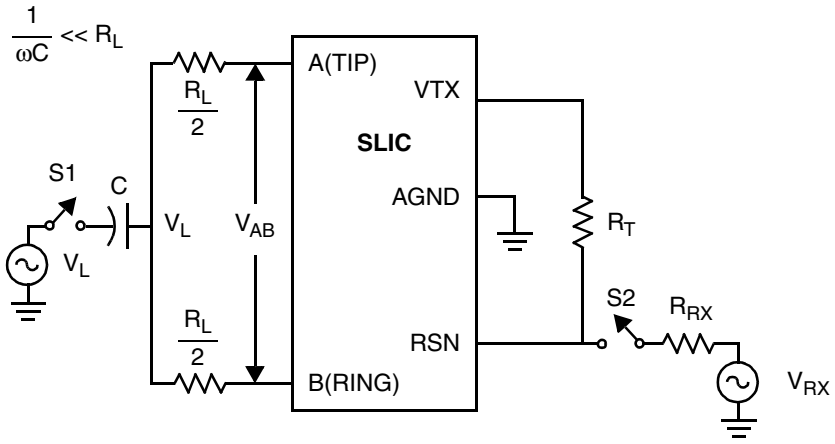
TEST CIRCUITS



A. Two- to Four-Wire Insertion Loss



B. Four- to Two-Wire Insertion Loss

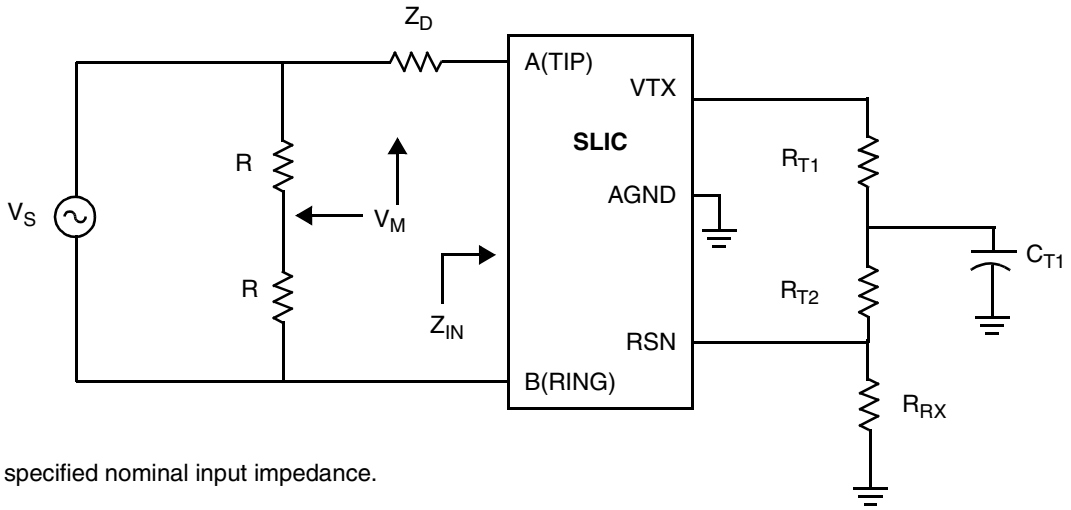


S2 Open, S1 Closed
L-T Long. Bal. = 20 log (V_{AB} / V_L)
L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance

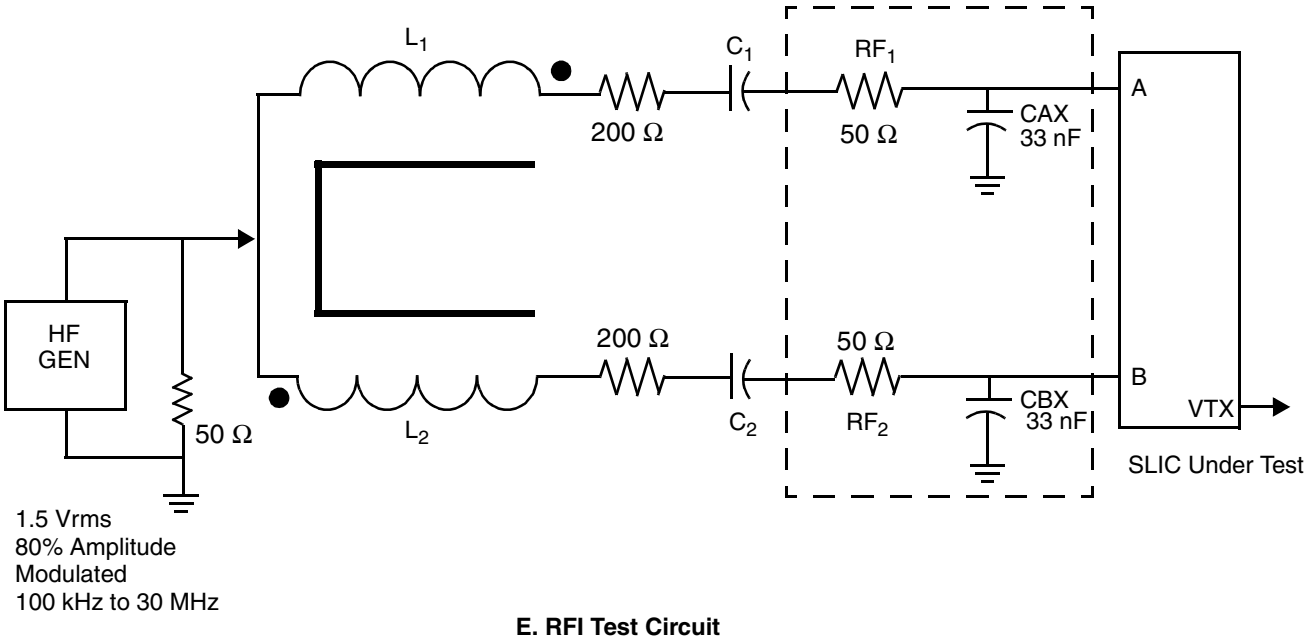
TEST CIRCUITS (continued)



Z_D is the specified nominal input impedance.

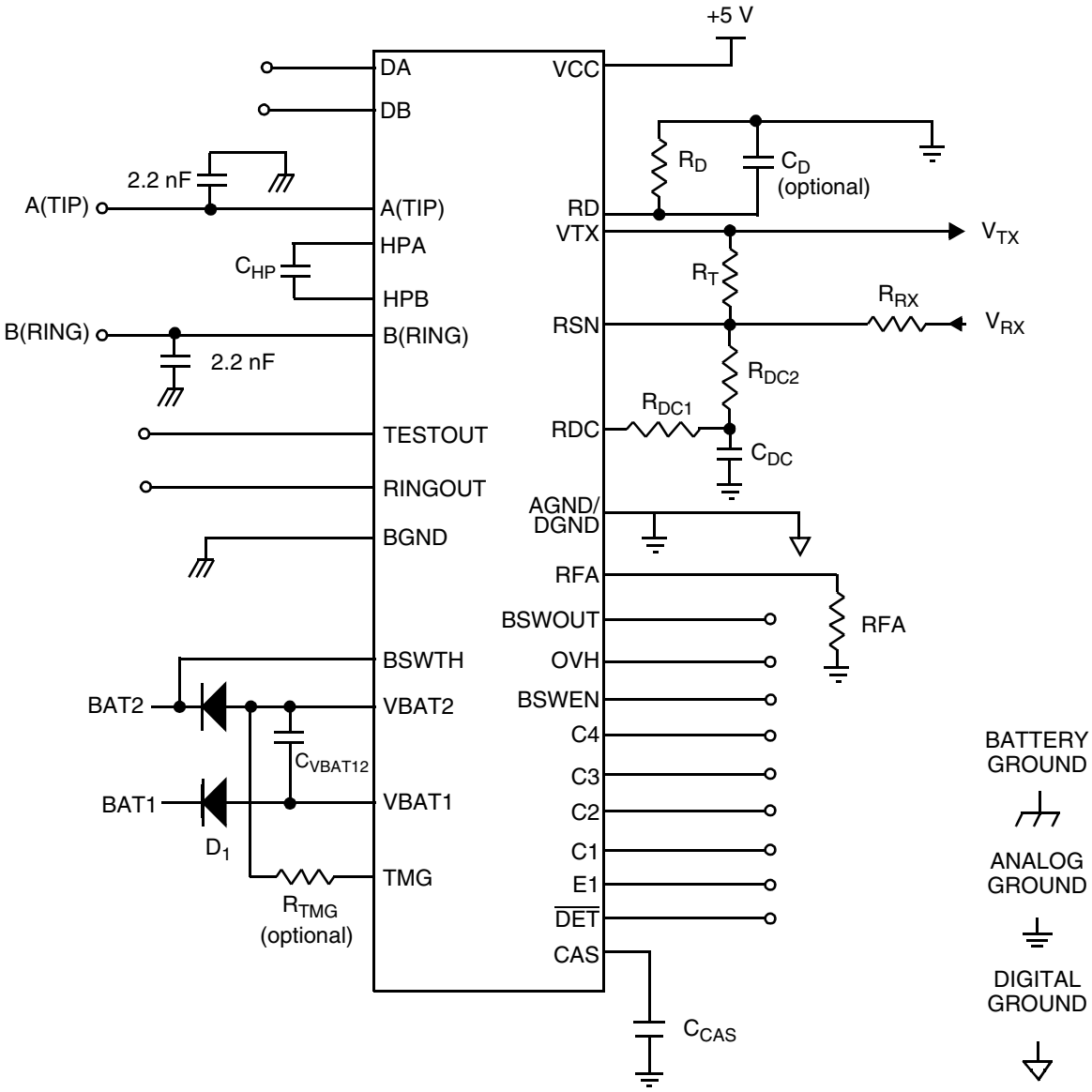
Return loss = –20 log (2 V_M / V_S)

D. Two-Wire Return Loss Test Circuit



E. RFI Test Circuit

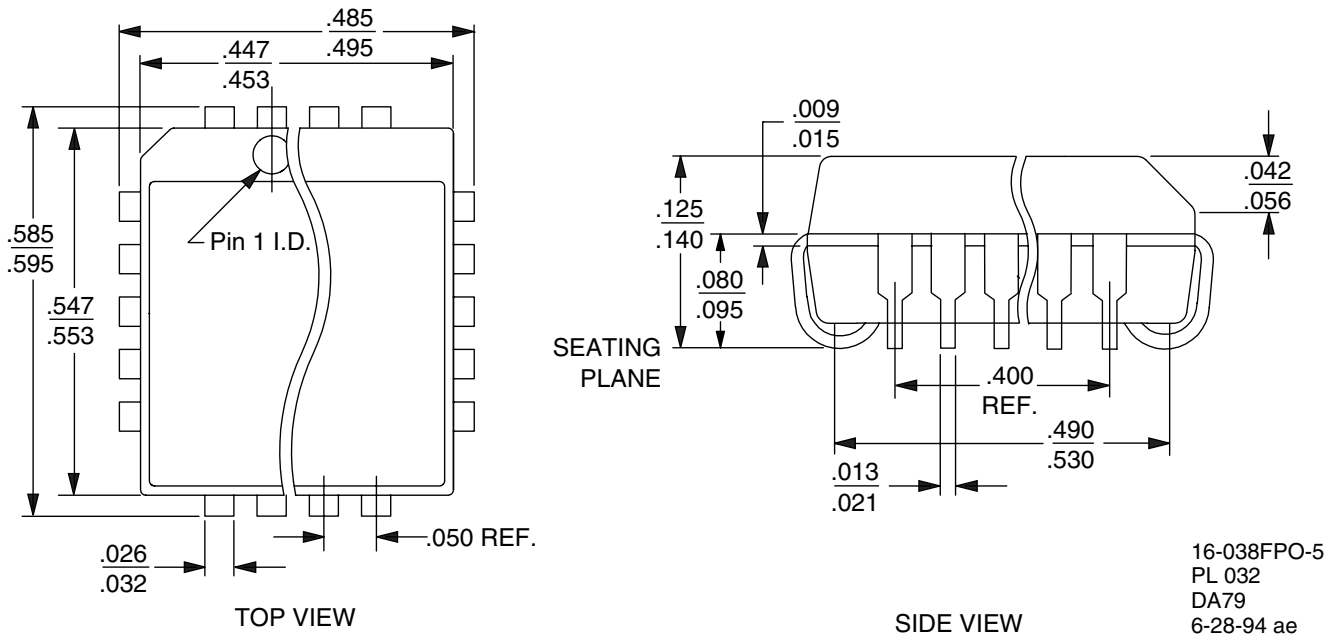
TEST CIRCUITS (continued)



F. Am79489 Test Circuit

PHYSICAL DIMENSIONS

PL032



REVISION SUMMARY

Revision C to Revision D

- In the Electrical Characteristics table on page 8, some information was changed in the Test Conditions column in the Loop Detector section and the “Loop-detect threshold hysteresis” row was added to this section.

Revision D to Revision E

- The physical dimensions (PL032) were added to the Physical Dimensions section.
- Updated the Pin Description table to correct inconsistencies.

Notes:

Legerity provides silicon solutions that enhance the performance, speeds time-to-market, and lowers the system cost of our customers' products. By combining process, design, systems architecture, and a complete set of software and hardware support tools with unparalleled factory and worldwide field applications support, Legerity ensures its customers enjoy a smoother design experience. It is this commitment to our customers that places Legerity in a class by itself.

P.O. Box 18200
Austin, Texas 78760-8200

Telephone: (512) 228-5400
Fax: (512) 228-5510
North America Toll Free: (800) 432-4009

To contact the Legerity Sales Office nearest you, or to download or order product literature, visit our website at ***www.legerity.com.***

To order literature in North America, call:
(800) 572-4859
or email:
americalit@legerity.com

To order literature in Europe or Asia, call:
44-0-1179-341607
or email:
Europe — eurolit@legerity.com
Asia — asialit@legerity.com