Analog Microelectronics, Inc.

AME811/AME811A/AME811R

3-1/2 Digit A/D Converter - Low Power With HOLD And Differential Reference Inputs

■ Key Features

- 100µV Resolution
- High Impedance Differential Inputs
- Differential Reference
- Drive LCD Directly
- Three New Convenient Features (AME811A Only)
  - Low-Battery Indication
  - Integration Status Indication
  - De-Integration Status Indication

■ Applications

- Digital multimeter
- pH meter
- Capacitance meter
- Thermometer
- Digital Panel meter
- Photometer

■ General Description

The AME811 family are high performance, low power. 3-1/2 digit, dual-slope integrating A/D converters, with on-chip display drivers. The AME811 is designed for a single battery operated system, will drive non-multiplexed LCD display directly.

These A/D converters are inherently versatile and accurate. They are immune to the high noise environments. The true differential high impedance inputs and differential reference are very useful for making ratiometric measurement, such as resistance, strain gauge and bridge transducers. The built-in auto-zero feature automatically corrects the system offset without any external adjustments.

Low-battery flag, integration and de-integration status flags are three additional features which are available in the 44-pin package, AME811ACKW.

■ Typical Operating Circuit

* For the operating circuit of the reverse-pins version, please refer to pin configuration on page 4 and pin description on page 5 & 6.

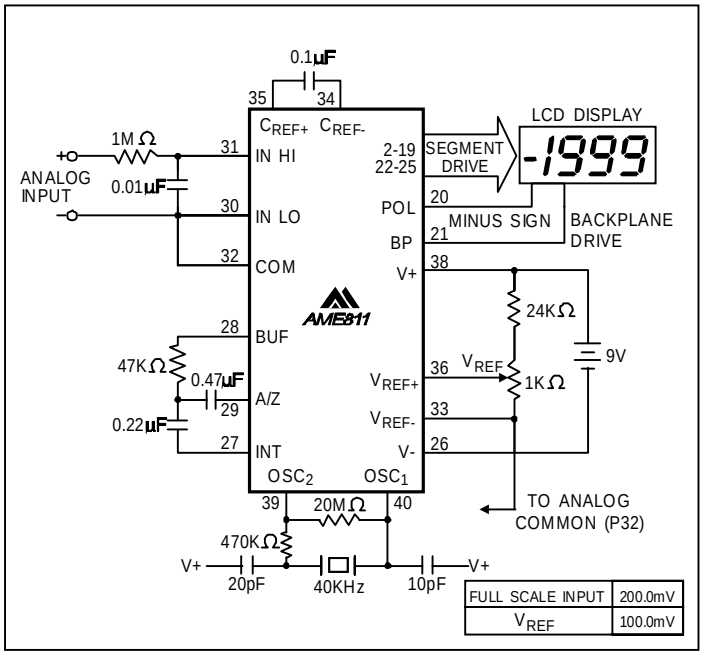

Figure 1. AME811 Typical Operating Circuit

■ Absolute Maximum Ratings

AME811

Supply Voltage (V+ to V-)	12V
Analog Input Voltage (Either inputs)	V+ to V-
Reference Input Voltage (Either inputs)	V+ to V-
Clock Input	Test to V+
Power Dissipation	800mW
Operating Temperature	0^oC to 70^oC
Storage Temperature	-55^oC to 150^oC
Lead Temperature (Soldering 60 seconds)	300^oC

Static sensitive device. Unused devices must be stored in the conductive material.
Protect device from static discharge and static field. Stresses exceed the above Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating Conditions for extended periods may affect the reliability of the device.

■ Ordering Information

Part Number	Display	Marking	Package	Pin Layout	Temp.Range
AME811CPL	LCD	AME811CPL YYWW	40 Pin PDIP	Normal	0^oC to 70^oC
AME811RCPL	LCD	AME811RCPL YYWW	40 Pin PDIP	Reverse	0^oC to 70^oC
AME811ACKW	LCD	AME811ACKW YYWW	44 Pin PQFP	Normal	0^oC to 70^oC

■ Electrical Characteristics

Unless otherwise noted, AME811 is specified at TA = 25°C, fclock = 48KHz. Supply voltage = 9V (V+ to V-)

Parameter	Conditions	Min	Typ	Max	Unit
Zero Input Reading	Vin = 0V Full-Scale = 200.0mV	-0	w 0	+0	Digital Reading
Ratiometric Reading	Vin = Vref = 100.0mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	-Vin = +Vin ≈ 200.0mV	-1	–0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200.0mV	-1	–0.2	+1	Counts
Common-Mode Rejection Ratio	Vcm = –1V, Vin =0V Full-Scale = 200.0mV		50		µV/V
Noise (Pk-Pk Value Not Exceeded 95% of Time)	Vin = 0V Full-Scale = 200.0mV		15		µV
Leakage Current at Input	Vin = 0V		1	10	pA
Zero Reading Drift	Vin = 0V, 0°C to 70°C		0.2	1	µV/°C
Analog Common Voltage (With respect to V+)	25KΩ Between Common and V+	2.8	3	3.2	V
Temp. Coeff. of Analog Common (With respect to V+)	25KΩ Between Common and V+ 0°C m T_A m 70°C		50	75	ppm/°C
Low Battery Flag	V+ to V-	6.3	7.0	7.7	V
Test Pin Voltage	With respect to V+	4	5	6	V
LCD Segment Drive Voltage	V+ to V- = 9V	4	5	6	V
Backplane Drive Voltage	V+ to V- = 9V	4	5	6	V

Notes: 1. Input voltage may exceed the supply voltages provided the input current is limited to ±100µA.
2. Dissipation rating assumes a device is mounted with all leads soldered to printed circuit board.

■ Pin Configurations

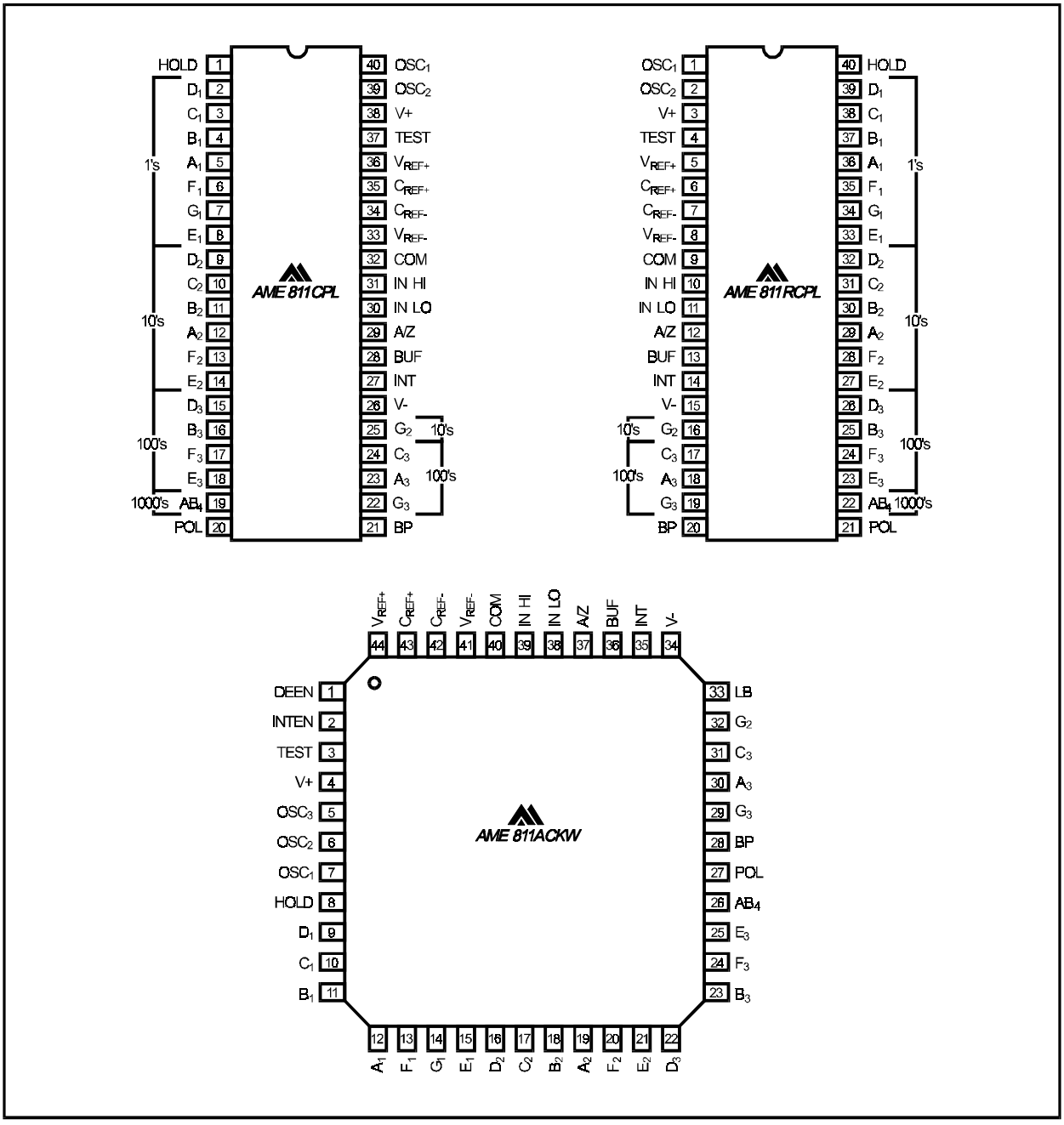

Figure 2. Pin Configurations

■ Pin Description

40-pin DIP Pin Number	40-pin DIP (Reverse)	44-pin PQFP Pin Number	Symbol	Description
1	(40)	8	HOLD	HOLD pin, Logic 1, Holds Display
2	(39)	9	D1	Units-digit D-segment driver
3	(38)	10	C1	Units-digit C-segment driver
4	(37)	11	B1	Units-digit B-segment driver
5	(36)	12	A1	Units-digit A-segment driver
6	(35)	13	F1	Units-digit F-segment driver
7	(34)	14	G1	Units-digit G-segment driver
8	(33)	15	E1	Units-digit E-segment driver
9	(32)	16	D2	Tens-digit D-segment driver
10	(31)	17	C2	Tens-digit C-segment driver
11	(30)	18	B2	Tens-digit B-segment driver
12	(29)	19	A2	Tens-digit A-segment driver
13	(28)	20	F2	Tens-digit F-segment driver
14	(27)	21	E2	Tens-digit E-segment driver
15	(26)	22	D3	Hundreds-digit D-segment driver
16	(25)	23	B3	Hundreds-digit B-segment driver
17	(24)	24	F3	Hundreds-digit F-segment driver
18	(23)	25	E3	Hundreds-digit E-segment driver
19	(22)	26	AB4	Thousands-digit, B&C segments driver
20	(21)	27	POL	Negative-polarity driver
21	(20)	28	BP	LCD backplane driver
22	(19)	29	G3	Hundreds-digit G-segment driver
23	(18)	30	A3	Hundreds-digit A-segment driver
24	(17)	31	C3	Hundreds-digit C-segment driver
25	(16)	32	G2	Tens-digit G-segment driver
¢w		33	LB	Low-battery flag segment driver
26	(15)	34	V-	Negative power supply voltage
27	(14)	35	INT	Integrator output. Connection point for integration capacitor.
28	(13)	36	BUF	Integrator resistor connection-point.
29	(12)	37	A/Z	Auto-zero capacitor connection-point
30	(11)	38	INLO	Analog-input low
31	(10)	39	INHI	Analog-input high
32	(9)	40	COM	Analog-common
33	(8)	41	VREF-	Analog-reference input, negative terminal

■ Pin Description (Cont.)

40-pin DIP Pin Number	40-pin DIP (Reverse)	44-pin PQFP Pin Number	Symbol	Description
34	(7)	42	CREF-	Reference capacitor, negative terminal
35	(6)	43	CREF+	Reference capacitor, positive terminal
36	(5)	44	VREF+	Analog-reference input, positive terminal
¢w		1	DEEN	De-integration status flag
¢w		2	INTEN	Integration status flag
37	(4)	3	TEST	Display-test pin, When pulled to V+, display should read -1888.
38	(3)	4	V+	Positive supply voltage
¢w		5	OSC3	Buffered OSC1
39	(2)	6	OCS2	Crystal oscillator output
40	(1)	7	OCS1	Crystal oscillator input

■ Function Description

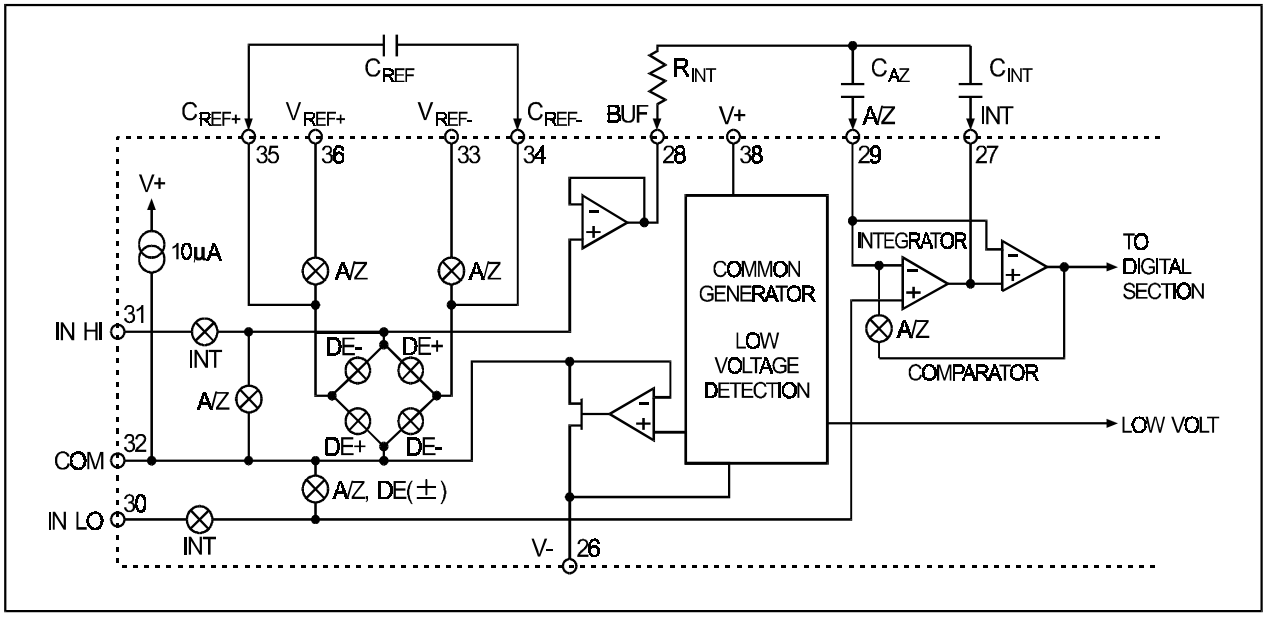

Figure 3. Analog Section

The A/D conversion has the following three phases:
1. Auto-Zero Phase
2. Integration Phase
3. De-integration Phase

Auto-Zero Phase

The INHI and INLO are shorted to analog common internally. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to cancel the offset voltage of buffer, integrator and comparator.

Signal Integration phase

The converter integrates the differential voltage across the INHI and INLO for a fixed time, 1000 system clocks. The polarity of the signal is determined at the end of this phase.

Reference Integration Phase

INLO is internally connected to the Analog Common, INHI is connected across the reference capacitor with appropriate polarity determined by the control circuit. The integrator output will then return to zero. The time it takes to return to zero, 1000 x VIN /VREF, is the digital representation of the analog signal.

Differential Signal Inputs (INHI & INLO)

The AME811 has true differential inputs and accepts input signals within the input common mode voltage range (Vcm). Typical range is from 1V above the V- to 1V below the V+. The integrator output can swing within 0.3 V of V+ or V- without increasing linearity errors. Care must be exercised to make sure the integrator output does not saturate. In a typical application, the common mode is eliminated by connecting the INLO to COM, Analog Common.

Differential Reference (VREF+ & VREF-)

The reference voltage can be generated anywhere within the V+ to V-. Under a large common mode voltage, reference capacitor can gain charge during the de-integration of a positive signal. The reference capacitor will lose charge when de-integrating a negative input signal. The difference in reference voltage for positive or negative input voltages can cause the rollover error. To prevent rollover error from being induced by large common-mode voltages, reference capacitor should be large compared to stray node capacitance.

Analog Common (COM)

The Analog Common is to set a common mode voltage for the analog signal. The analog common is typically 3.0V below V+, set primary for the battery operated application. Analog common is capable to sink 20 mA. It's source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage to override the internal reference. When supply voltage is greater than 7V, analog common can be used as reference source with temperature coefficient of typically 50 ppm/°C.

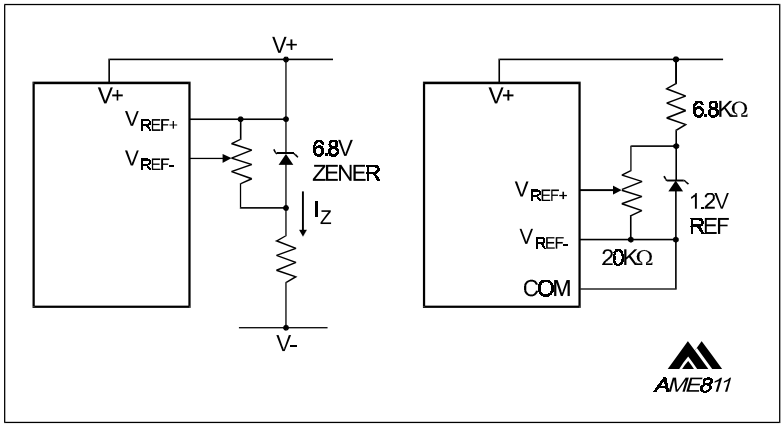

Figure 4. Using an External Reference

■ Digital Block Diagrams

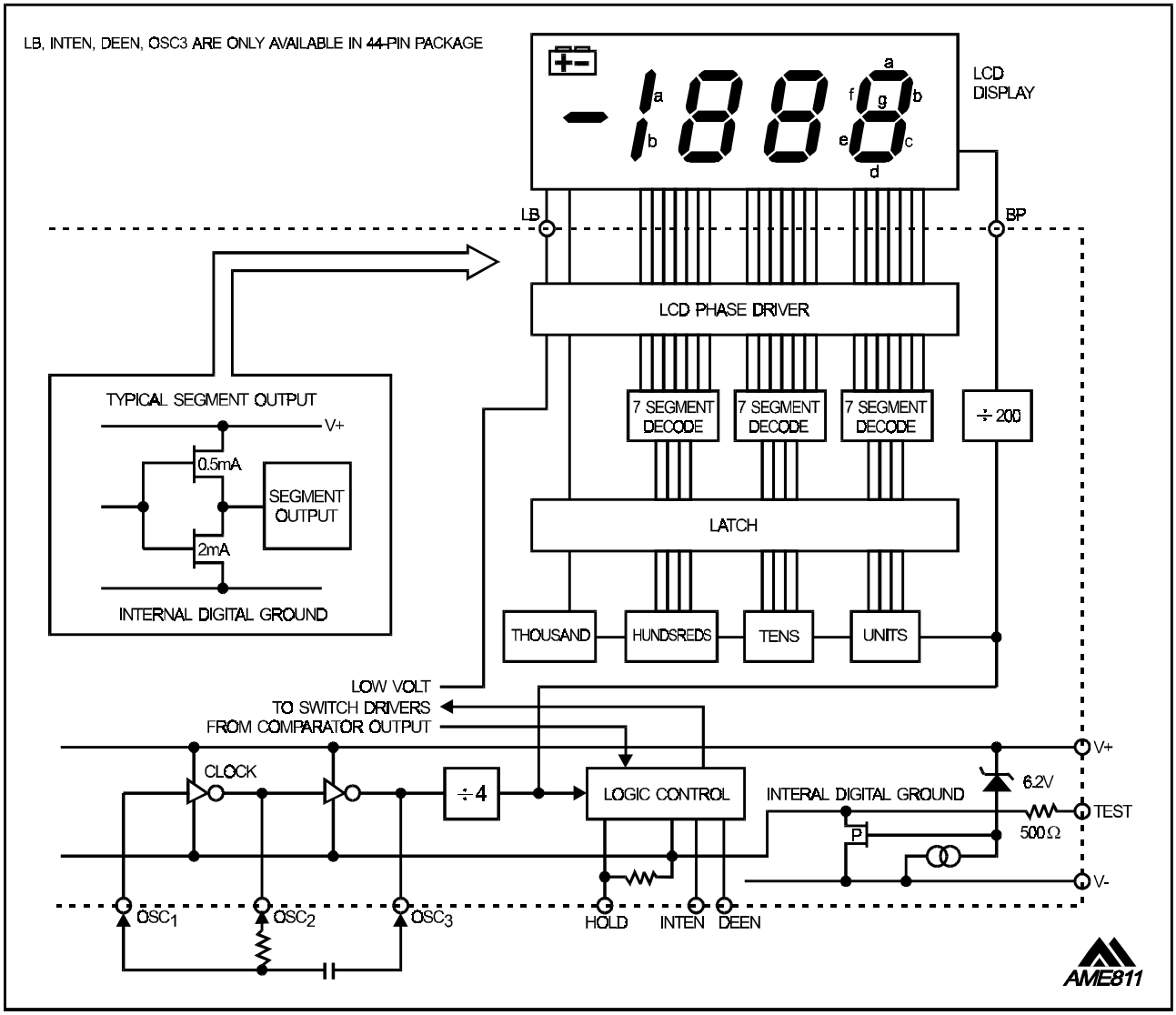

Figure 5. AME811 Digital Section

■ Digital Section

Digital Ground
AME811 generates an internal digital ground, typically 5V below the V+.

Clock Circuit

The clock can be generated in either of the following three methods.
1. An external oscillator connected to “OSC1”
2. A crystal between pins “OSC1” and “OSC2”
3. A R-C oscillator using “OSC1”, “OSC2” and “OSC3”

Notes: There is no on-chip feedback resister across osc1 and osc2.

Systems Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. Each conversion takes 4000 counts or 16000 oscillator clock pulses. The timing of each phase are as follows:

Auto-Zero Phase:	1000 to 3000 Counts
Signal Integration Phase:	1000 Counts (Fixed)
Reference Integration Phase :	0 to 2000 Counts

For signals less than full-scale, the unused reference integration time is assigned to the autozero phase.

Segment Drivers

The backplane frequency is 1/800 of the oscillator clock frequency. For example if the oscillator frequency is 48 KHz (3 conversions per second) the backplane frequency will be 60 Hz. The segment and backplane are at the same frequency with a nominal 5 volt amplitude. The segment is visible (ON) when the segment and the backplane are out of phase, otherwise it is invisible (OFF). The polarity segment is “ON” for negative analog inputs. When the TEST pin on the AME811 is pulled to V+, all segments are turned “ON”. The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. **DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES!** LCD displays may be destroyed if operated with DC levels for extended periods.

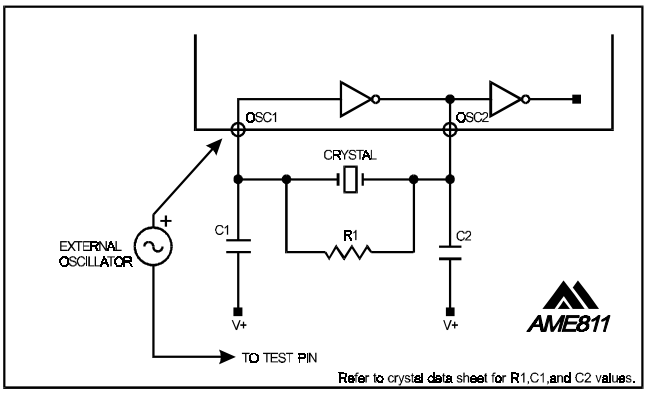

Figure 6a. Clock Circuit

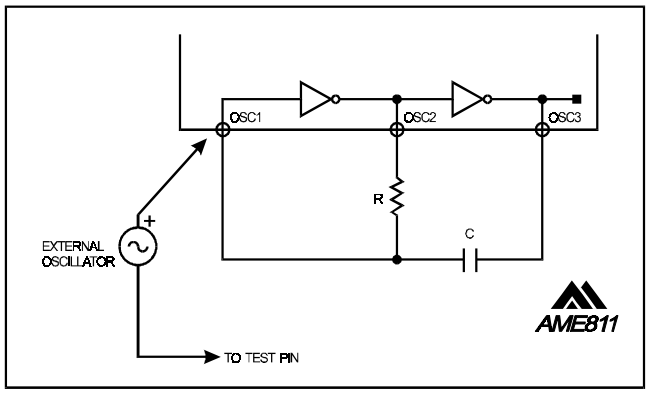

Figure 6b. Clock Circuit (for 44-pin only)

Test
When the TEST is pulled to V+ all segments and the minus sign will be activated. The TEST pin is tied to the internally generated digital ground through a 500Ω resistor in the AME811. It is typically 5V lower than V+. TEST pin may be used as the negative power supply for external CMOS logic at the maximum current of 1 mA.

Data Hold
When the Hold pin is connected to V+ the conversion result will not be updated. The conversion is still free running during the hold mode.

Integration Status (INTEN)
The INTEN is an output signal of the converter, it is "high" during the signal integration phase. This signal can be used as a status indicator or a control to connect the analog signal to the converter for processing. It is available in 44 pin package.

De-integration Status (DEEN)
The DEEN is an output signal of the converter, it is "high" during the reference de-integration phase. The period of the DEEN is proportional to the conversion result. Users may calculate the conversion result by counting the number of clock pulse on the OSC3 pin when DEEN is "high". The conversion result is equal to (N /4) - 1/2 where N is the number of the pulse at the OSC3 pin. It is available in 44 pin package.

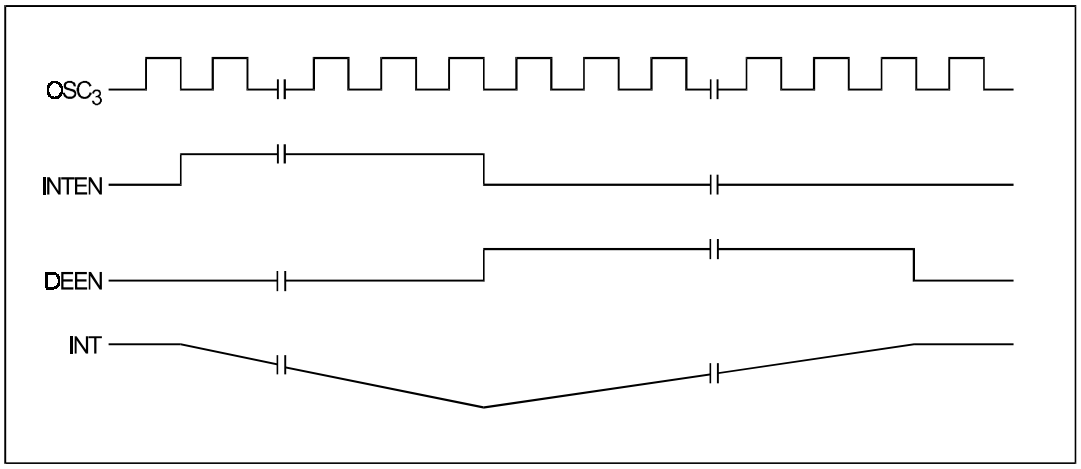

Figure 7. Timing of OSC3, INTEN, DEEN, and INTEGRATOR Output.

■ Component Value Selection

Auto-Zero Capacitor (Caz)
The Caz capacitor size has some influence on system noise. A 0.47μF capacitor is recommended for 200 mV full-scale applications. A 0.047μF capacitor is recommended for 2.0V full-scale applications. A mylar dielectric capacitor is adequate.

Reference Capacitor (Cref)
A 0.1μF capacitor is acceptable when "INLO" is tied to analog common. If a large common-mode voltage exists and the application requires 200 mV full-scale, increase Cref to 1.0 μF. A mylar dielectric capacitor is adequate.

Integrating Capacitor (Cint)

Cint should be selected to maximize the integrator output voltage swing without causing output saturation. A ±2V full-scale integrator output swing is recommended if "ANALOG COMMON" is used as signal reference. For 3 readings/second (fosc = 48 KHz) a 0.22 μF value is suggested. If a different oscillator frequency is used, Cint must be changed in inverse proportion to maintain the nominal ± 2V integrator swing. An exact expression for Cint is:

Cint = [(4000)(1/fosc)(Vfs/Rint)] / Vint

where:
- fosc= Oscillator clock frequency
- Vfs = Full-scale input voltage
- Rint = Integrating resistor
- Vint = Desired full-scale integrator output swing

Cint must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

Integrating Resistor (Rint)

The input buffer amplifier and integrator both have a class A output stage with 100 μA quiescent current. The integrator and buffer can supply 20 μA drive currents with negligible linearity errors. Rint is chosen to keep the output stage in the linear region. For a 200mV full-scale, it is 47KΩ; 2.0V full-scale requires 470KΩ.

Summary of component selection:

Full scale	200.0mV	2.000V
Caz	0.47μF	0.047μF
Rint	47 KΩ	470 KΩ
Cint	0.22μF	0.22 μF
Vref	100.0mV	1.000V

Note: fosc = 48 KHz

Oscillator Components

R-C Oscillator

A 100 KΩ Rosc is recommended for all frequencies. Cosc is selected by using the equation:

fosc = 0.45/(RC)

For fosc of 48KHz, Cosc is 100pF nominally.

To achieve maximum line noise rejection, the signal-integrate period should be a multiple of line period. The optimum oscillator frequencies for 60 Hz and 50 Hz rejection are listed as follows:

For 60 Hz rejection:
40KHz, 48KHz, 60KHz etc.

For 50 Hz rejection:
40KHz, 50KHz, 66-2/3KHz etc.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Full-Scale Voltage	Vref
200.0 mV	100.0 mV
2.000 V	1.000 V

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 600 mV for 2000 lb/in^2. Rather than dividing the input voltage by three the reference voltage should be set to 300 mV. This permits the transducer input to be used directly. The integrator resistor would be 120KΩ. In some temperature and weighting system with variable tare, the offset reading can be generated by connecting the voltage transducer between INHI and COMMON and the variable offset voltage between COMMON and INLO.

Low Battery Flag (LB)

The low battery flag is set when the supply voltage (V+ to V-) is lower than seven volts, typical. Once the LB is set, the waveform of the LB will be out of phase with the BP (Back Plane) to turn on a low battery annunciator for AME811.

■ Typical Applications

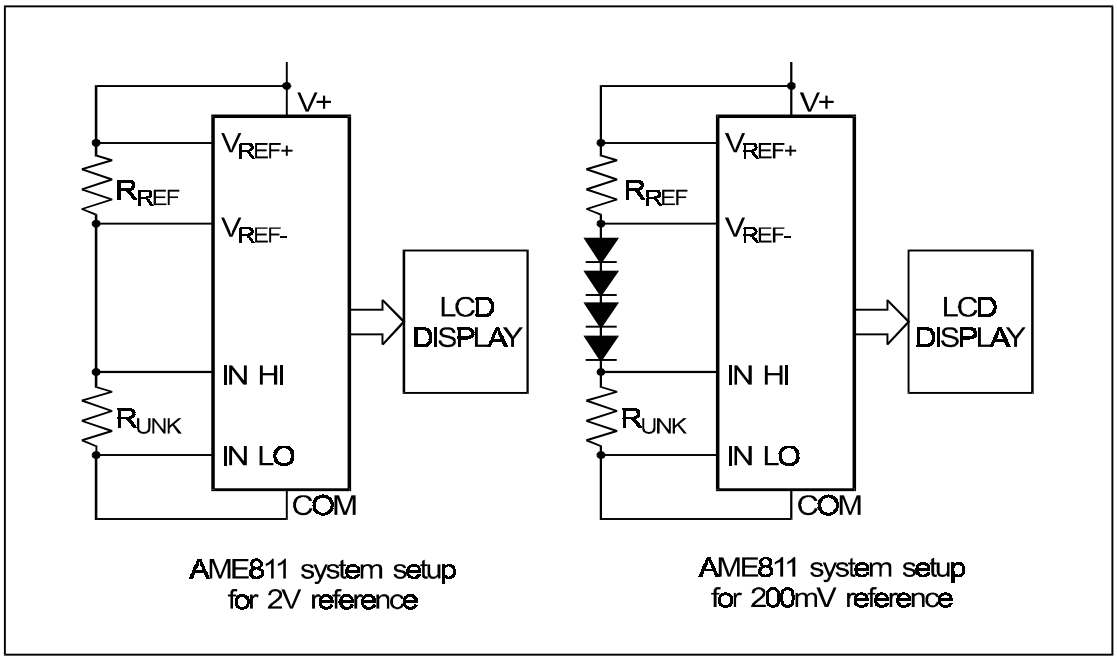

Figure 8. Ratiometric Resistance Measurement

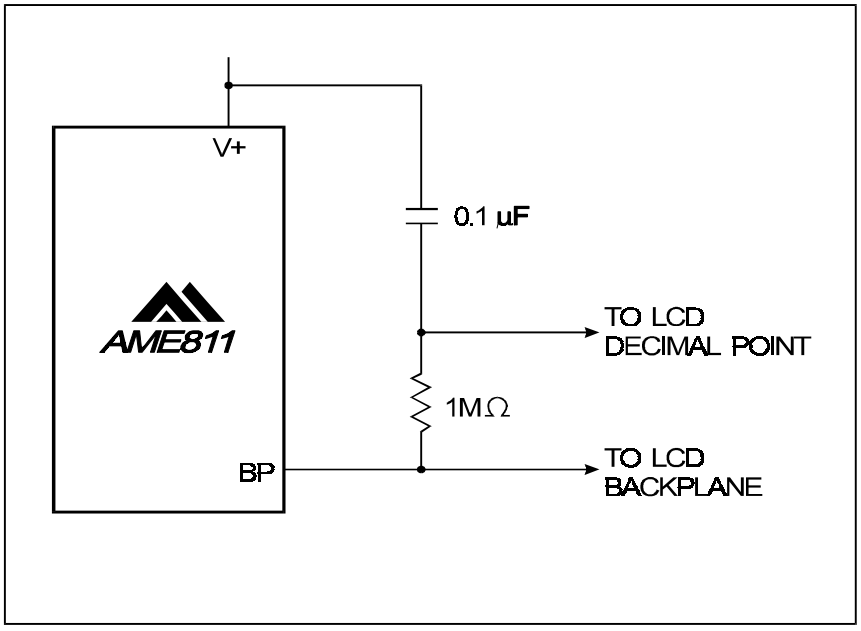

Figure 9. Fixed decimal point drivers

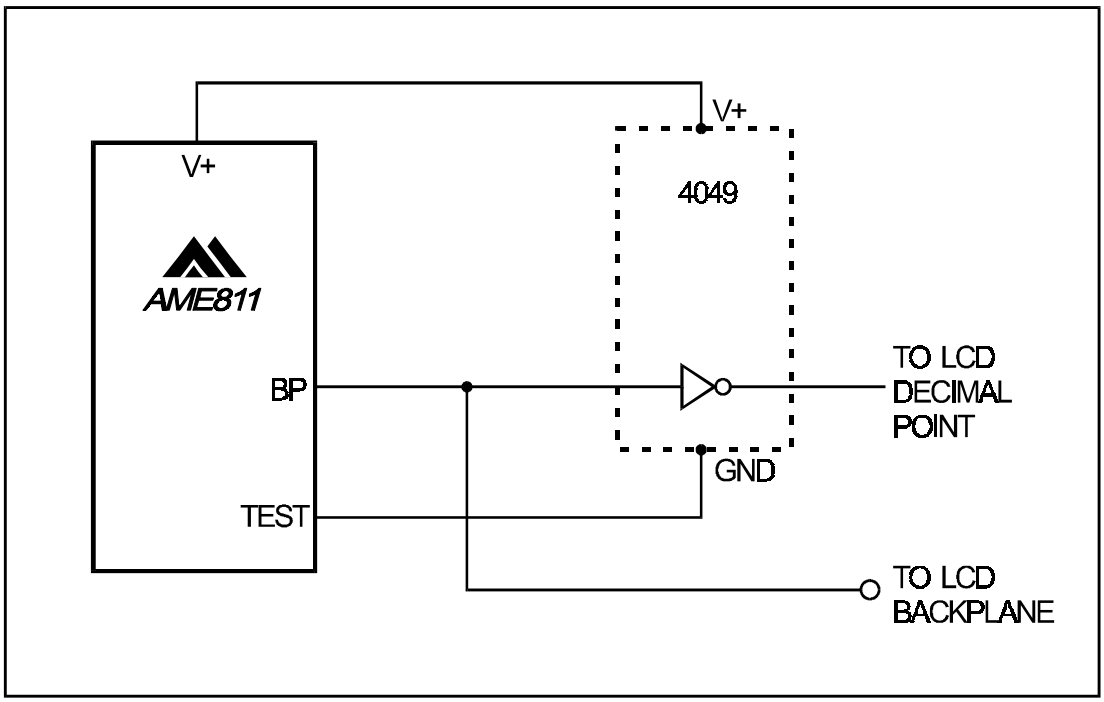

Figure 10. Fixed decimal point drivers

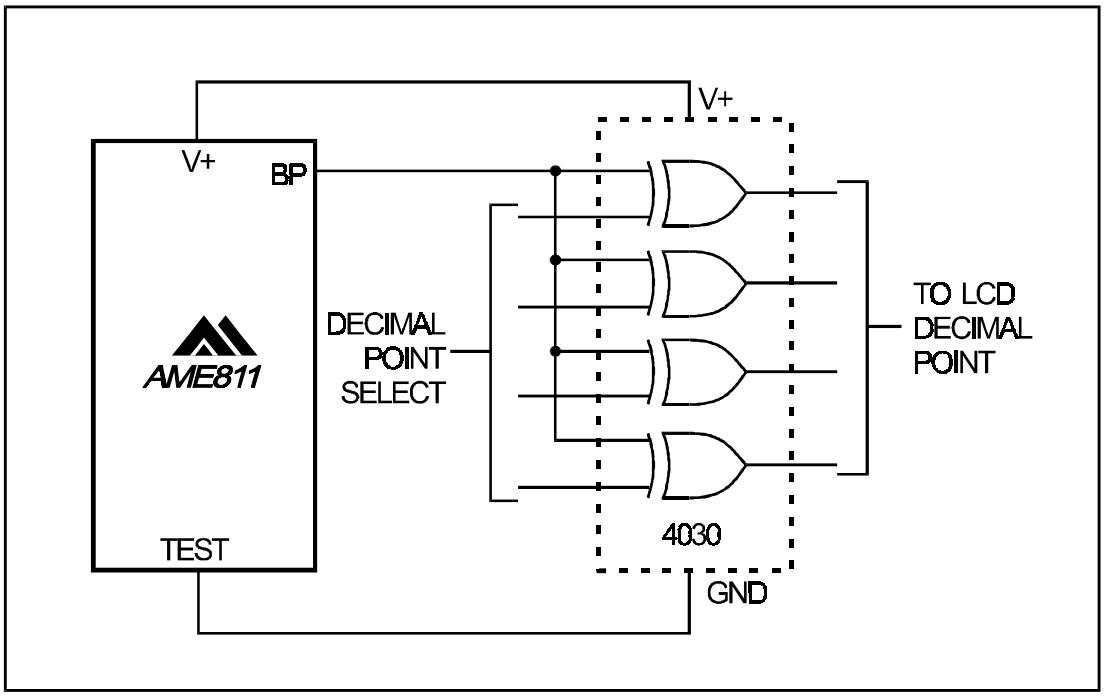

Figure 11. Decimal Point Drivers with Select

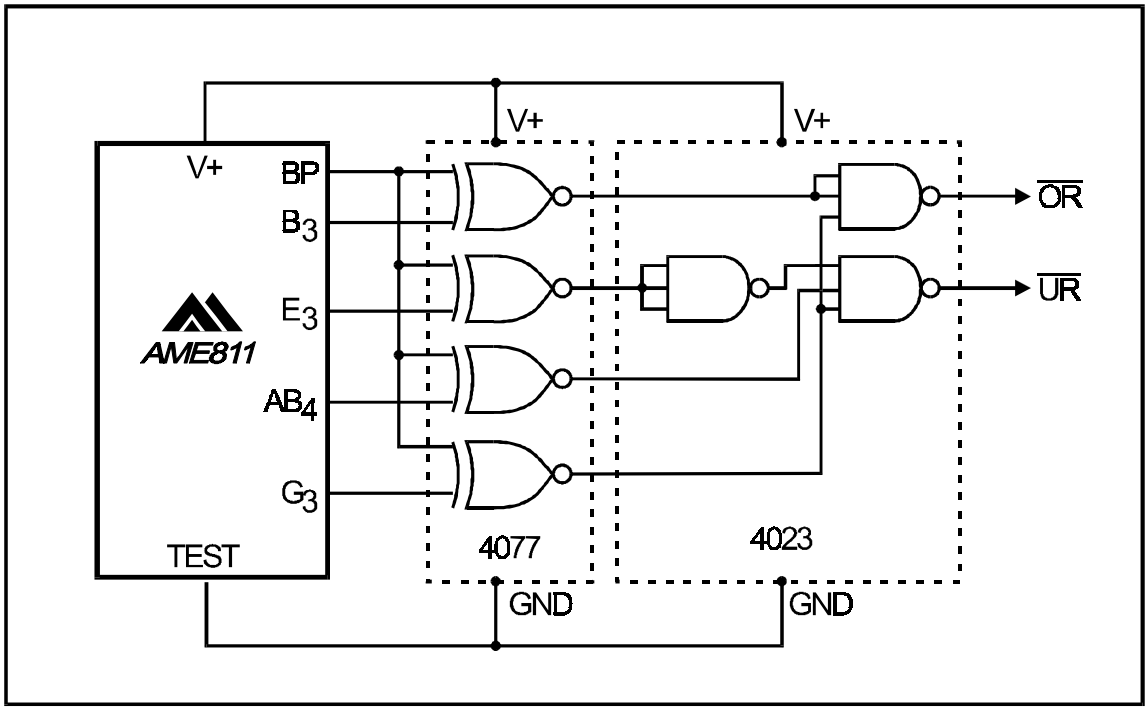

Figure 12. Generating Under Range and Over Range Signals

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