1.0 General Description

The AMIS-720233-B (PI3033B) contact image sensor (CIS) chip is a 200 dot per inch (dpi) resolution, linear array image sensor chip. The sensor chip is processed with AMI Semiconductor's proprietary CMOS image sensing technology. Designed for cascading multiple chips in a series, the image sensor chips, using chip-on-board process, are bonded end-to-end on a printed circuit board (PCB) in varying sensing array lengths. This CIS chip offers image reading widths to suit document scanners found in facsimile, scanner, check reader and office automation equipment.

Figure 1 is a block diagram of the imaging sensor chip. Each sensor chip consists of 64 detector elements, their associated multiplexing switches, buffers and a chip selector. The detector's element-to-element spacing is approximately 125um. The size of each chip without scribe lines is 7950um by 500um. Each sensor chip has eight bonding pads. Only seven are used to make the CIS modules. The pad symbols and functions are described in Table 1.

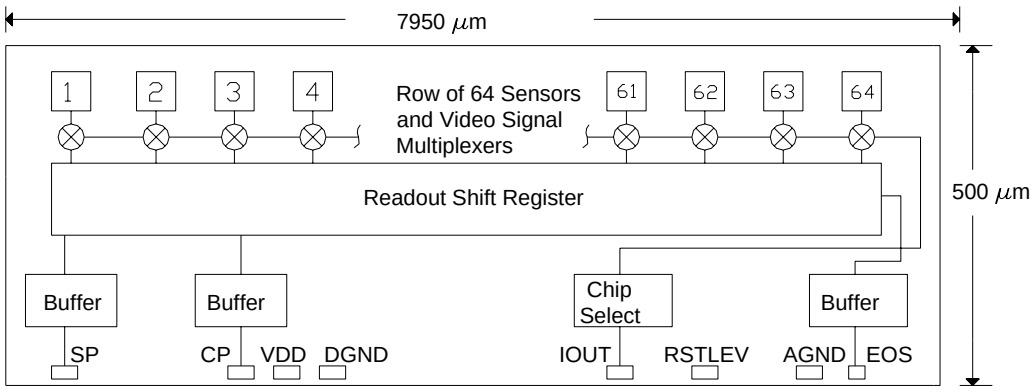


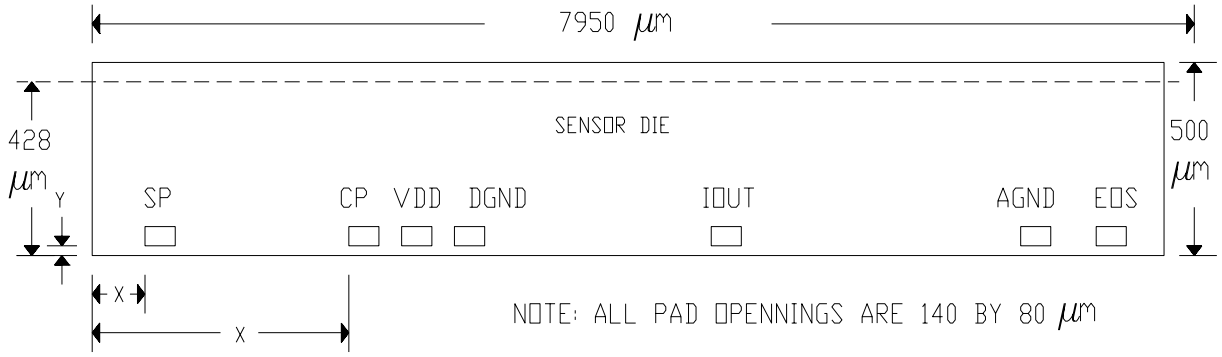
Figure 1: AMIS-720233-B Block Diagram

Table 1: Pad Symbols and Functions

Symbol	Function
SP	Start pulse: input to start the line scan
CP	Clock pulse: input to clock the shift register
VDD	Positive supply: +5V supply connected to substrate
DGND	Digital ground: connection topside common
RSTLEV	A bias pad: not used, left floating
IOUT	Signal current output: output for video signal current
AGND	Analog ground: connection topside common
EOS	End-of-scan pulse: output from the shift register at end-of-scan

2.0 Bonding Pad Outputs Locations and Die Dimensions

Figure 2 shows image sensors die dimension and the bonding pad locations for the AMIS-720233-B sensor chip. The location is referenced to the lower left corner of the die. Note RSTLV, bias pad is not used.



PAD	FUNCTION	Y	X
SP	START INPUT	27.5	858.0
CP	CLOCK INPUT	27.5	3143.0
VDD	+5 SUPPLY	27.5	3430.0
DGND	GROUND	27.5	3672.0
IOUT	VIDEO SIGNAL OUT	27.5	4852.0
AGND	ANALOG GROUND	27.5	6393.0
EOS	SCAN OUTPUT	27.5	6662.0

NOTES:
1. THE DRAWING IS NOT TO SCALE.
2. THE DIE LENGTH AND WIDTH ARE GIVEN AS SHOWN.
3. THE PAD LOCATION ARE GIVEN IN THE TABLE
4. THERE ARE TWO EXAMPLES OF THE X AND Y LOCATIONS SHOWN ON THE FIRST TWO PADS. THEY ARE MEASURED TO THE LEFT BOTTOM CORNER OF THE PAD OPENNING
5. ALL DIMENSIONS ARE IN µm.
6. SENSOR LINE IS INDICATED BY THE DOTTED LINE.

Figure 2: Bonding Pad and Chip Layout

3.0 Wafer Scribe Lines

Figure 3 shows the wafer scribe lines bordering the AMIS-720233-B sensor chip. The wafer thickness is 350µm.

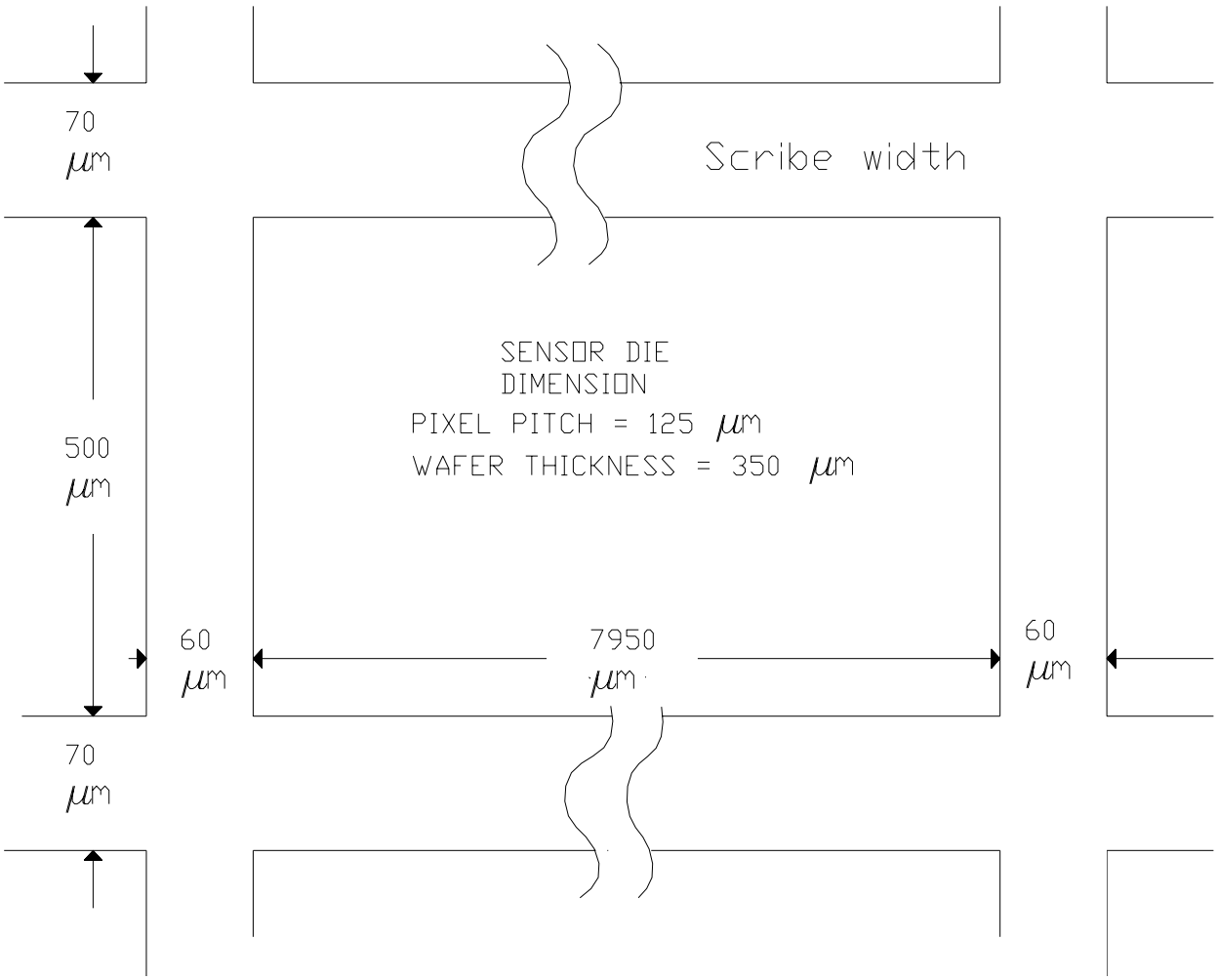


Figure 3: Wafer Scribe Lines

4.0 Electro-Optical Characteristics (25°C)

The electro-optical characteristics of AMIS-720233-B imaging sensor chip are listed in Table 2. These values are measured at 25°C.

Table 2: Electro-Optical Characteristics

Parameters	Symbols	Typical	Units	Notes
Number of photo-elements		64	Elements	
Pixel-to-pixel spacing		125	µm	
Line scanning rate	Tint (1)	864	µs/line	
Clock frequency	Fclk (2)	2.0	MHz	See Note 2 for higher clock speed. (maximum 5MHz)
Output voltage	Vpavg (3)	1.0	V	Exp = 1.8 X 10^{-2} µJ/cm^2
Output voltage non-uniformity	Up (4)	± 7.5	%	
Dark output voltage	Vd (5)	<20	mV	Notes 5 & 3
Dark output non-uniformity	Ud (6)	<10	mV	Notes 6 & 3
Adjacent pixel non-uniformity	Upadj (7)	<7.5	%	
Chip-to-chip non-uniformity	Ucc (8)	± 7.5	%	

Notes:

1. Tint stands for the line scanning rate or the integration time. It is determined by the time interval between two SPs.
2. Fclk stands for the input clock frequency. For Fclk > 2.0MHz see Note 3 and the Section 5.
3. Vpavg = ∑Vp(n)/Npixels (average level in one line scan).
   Where Vp(n) is the amplitude of n^{th} pixel in the sensor chip and Npixels is the total number of pixels in sensor chip. Vpavg is converted from impulse current video pixel into a voltage output (see Figure 4 and
4. Figure 5).
   Exp = LP x Tint, where LP is light power (Yellow-Green) and tint is as defined above (see Figure 6).
5. Up is the uniformity specification, measured under a uniform exposing light exposure. Up = [Vp(max) - Vpavg] / Vpavg x 100% or [Vpavg - Vp(min)] / Vpavg} x 100%, whichever is greater.
   Where Vp(max) is the maximum pixel output voltage in the light.
   Vp(min) is the minimum pixel output voltage in the light.
6. Vd = ∑Vp(n)/Npixels. Where Vp(n) is the pixels signal amplitude of the n^{th} pixel of the sensor. Dark is where the sensor is placed in the dark environment.
7. Ud = Vdmax – Vdmin. Dark is same definition as above.
8. Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)) x 100%. Upadj is the non-uniformity in percentage. It is the amplitude difference between two neighboring pixels.
9. Ucc is the uniformity specifications, measured among the good die on the wafer. Under uniform light exposure the sensors are measured and calculated with following algorithm: Vpavg of all the good dies on the wafer are averaged and assigned VGpavg. Then the die with maximum Vpavg is assigned Vpavg(max), and the one with minimum Vpavg is assigned Vpavg(min). Then UCC = {[Vpavg(max)-Vpavg(min)]/VGpavg}x100.

5.0 Output Circuit of the Image Sensor

The video signal from each photo-site is connected to a common video line on the sensor. Each photo-site is composed of a phototransistor with a series MOS switch connecting its emitter to a common video line. The video line is connected to the pad labeled IOUT. The photo-sensing element is the base of the phototransistor where it detects and converts the light energy to proportional charges and stores it in its base capacitance. When the MOS switch is activated, the emitter is connected to the video line and acts as source follower, producing an impulse current proportional to the stored charges in the base. This current is a discrete-time analog signal output called the video pixel. Accordingly, the video pixel is proportional to the light energy impinging in the neighborhood of its photo-sites. Figure 4, shows the output structure of four photo-sites out of 64. The multiplexing MOS switch in each photo-site terminates into the output pad, IOUT, through a common video line. The shift register sequentially accesses each photo-site by a activating the MOS switch. As they are accessed, a sequence of video pixels is sent to the IOUT where they are processed with an external signal conversion circuit.

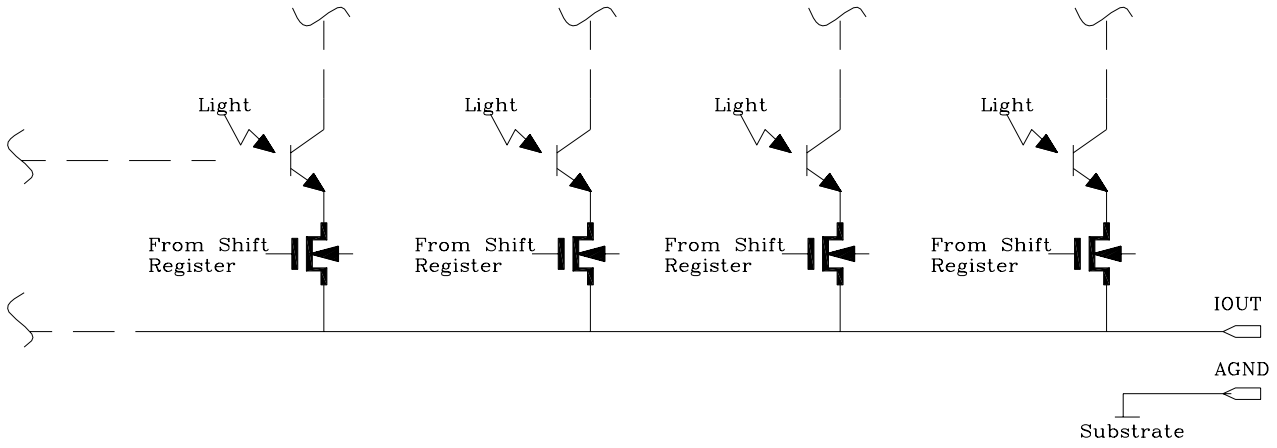


Figure 4: Video Pixel Output Structures

5.1 Signal Conversion Circuit

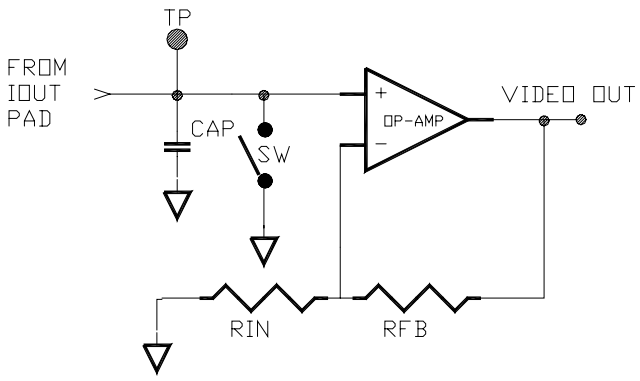


Figure 5: Video Output Test and Application Circuit

Figure 5 shows a simply circuit that provides the cleanest technique in processing the video output. It integrates all the currents from each pixel element onto a capacitor (CAP). Then the CAP is reset to zero volts by activating the shunt switch (SW) and connecting the video line to ground prior to accessing the following pixel element. Simultaneous to SW activation, the pixel element storage is reset to the dark level, hence initialized for the new pixel integration process. Since this process sums the switch edges and signal current pulses onto the CAP, it minimizes the switching patterns on the video pixels. The summed charges stored in the CAP produces a pixel voltage with amplitude proportional to the charge from the current pulse. Since switching energies are high frequencies components, they tend to integrate to a 0 value and the remainder adds a constant value to the dark level. The signal pixels Vp(n) is referenced to the dark level as it is seen in Figure 6, which depicts the typical pixel waveform.

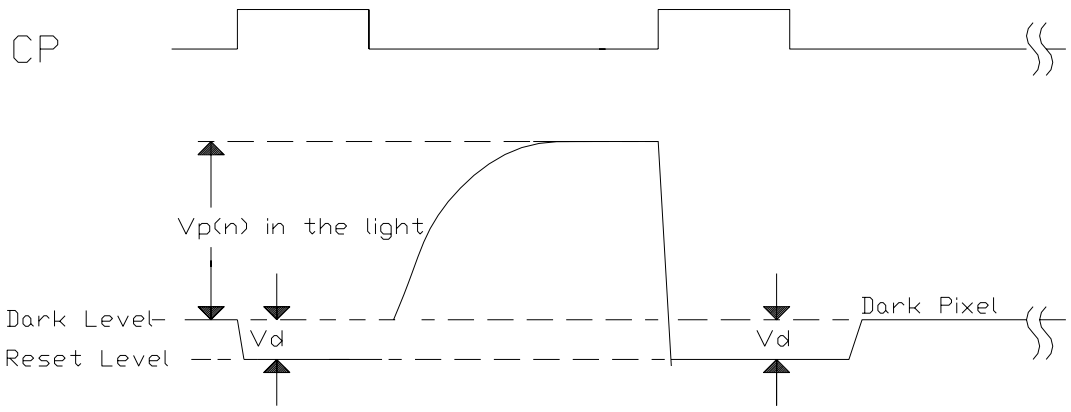


Figure 6: Single Pixel Video Output

To measure these device's parameters the value of the CAP is set to 100pf. This value includes the stray capacitance of the video line. The value of RIN in the amplifier circuit is set to infinity before it is removed and accordingly, the amplifier gain is one, therefore serving as a buffer amplifier, EL2044, AD8051 or its equivalent, to isolate the video line.

Since the output is specified with a light exposure, the video output is specified with a fixed exposure. However, exposure is a function of power and time, Exp = Light power x the tint, as well as its color. Accordingly, the AMIS-720233-B is measured with a Yellow-Green LED light source. See Figure 7.

Note: The value of 100pf is selected because the typical PCB layout of an A6 length module has a video line capacitance, including the stray, in the order of 100pf. The A6 length CIS module uses 13 sensor chips. See Figure 9.

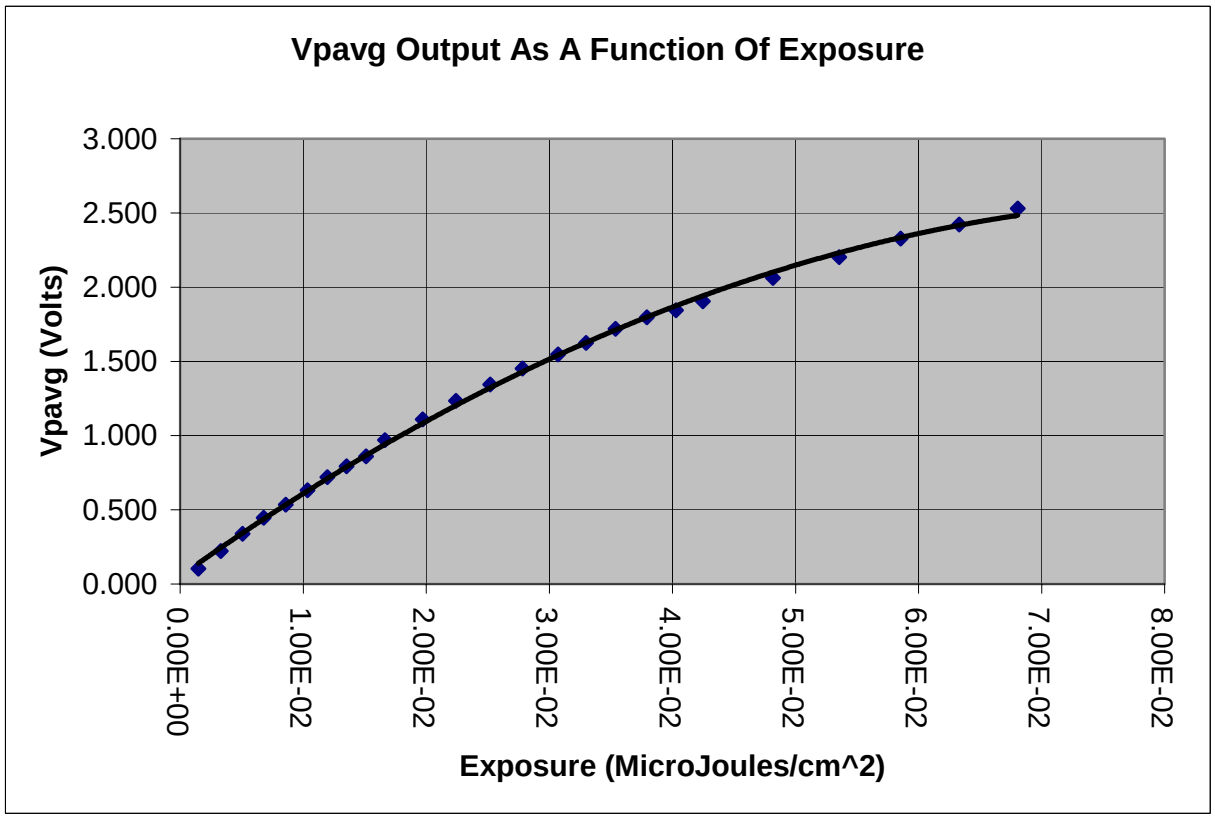


Figure 7: Vpavg as a Function of Exposure

6.0 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameters	Symbol	Maximum Rating	Units
Power supply voltage	VDD	10	V
Power supply current	IDD	<2.0	mA
Input clock pulse (high level)	Vih	Vdd + 0.5	V
Input clock pulse (low level)	Vil	-0.25	V
Operating temperature	Top	0 to 50	°C
Operating humidity	Hop	10 to 85	RH %
Storage temperature	Tstg	-25 to 75	°C
Storage humidity	Hstg	10 to 90	RH %

7.0 Recommended Operating Conditions at Room Temperature

Table 4: Recommended Operating Conditions at Room Temperature

Parameters	Symbol	Min.	Typ.	Max.	Units
Power supply	VDD	4.5	5.0	5.5	V
Input clock pulses high level	Vih (1)	3.0	5.0	VDD	V
Input clock pulse low level	Vil (1)	0	0	0.8	V
Operating high level exposed output	IOUT (2)		See Note 2		
Clock frequency	Fclk (3)	0.1	2.0	5.0	MHz
Clock pulse duty cycle	Duty (4)		25		%
Clock pulse high durations	tw		0.125		µsec
Integration time	Tint		0.864	10	ms
Operating temperature	Top		25	50	°C

Notes:

1. Applies to both CP and SP
2. The output is a current that is proportional to the charges, which are integrated on the phototransistor's base via photon-to-electron conversion. For its conversion to voltage pixels see Figure 4.
3. Although the clock frequency, Fclk, will operate the device at less than 100kHz, it is recommended that the device be operated above 500kHz to avoid complication of leakage current build-up. In applications using long CIS module length, such as an array of image sensor > 27, increases in the readout time, i.e., increases tint, hence, leakage current build-up occurs.
4. The clock duty cycle is normally set to 25 percent. However, it can operate with duty cycle as large as 50 percent, which will allow more reset time at the expense of video pixel readout time.

8.0 Switching Characteristics at 25°C

The timing relationships of the video output voltage and its two input clocks, the start pulse (SP) and the shift register clock (CP), along with the shift register EOS output clock, are shown in Figure 8. The switch timing specification for the symbols on the timing diagram is given in Table 5. The digital clocks' levels are +5V CMOS compatible. The video, IOUT, is specified in Figure 4.

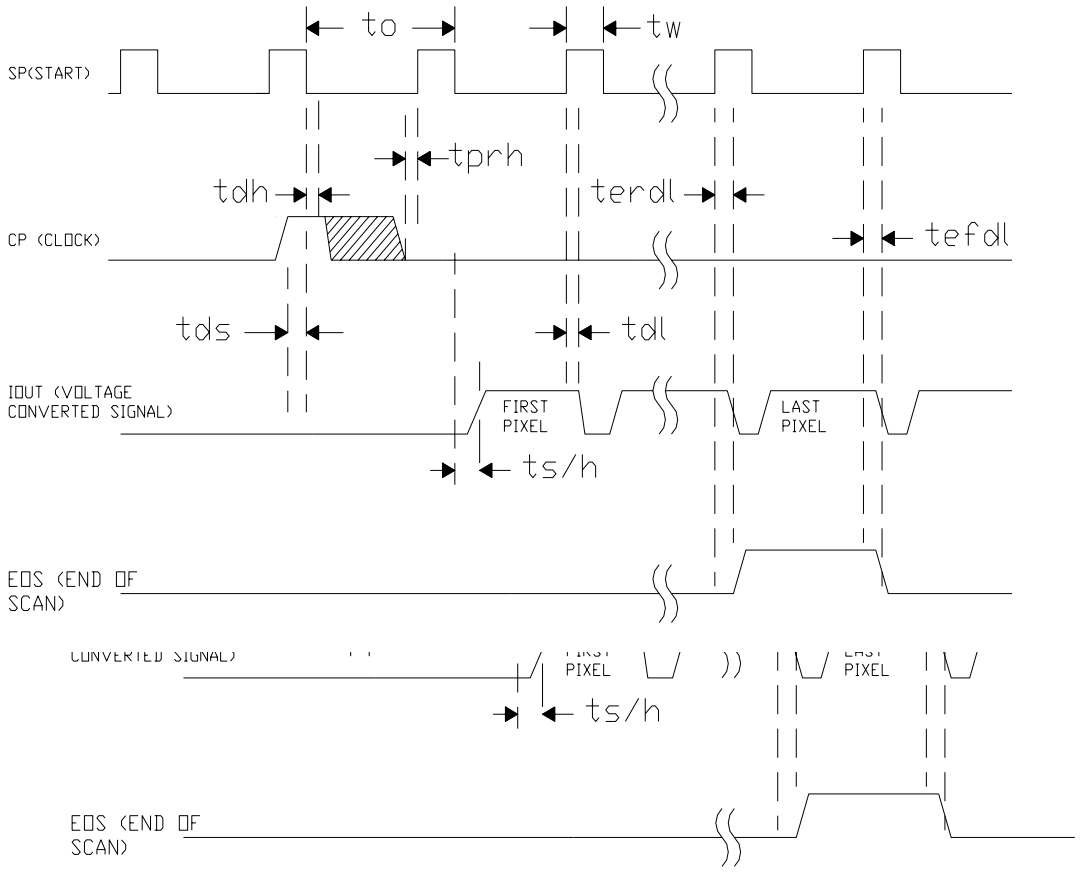


Figure 8: Timing Diagram of the AMIS-720233-B Sensor

Table 5: Timing Symbol's Definition

Item	Symbol	Min.	Mean	Max.	Units
Clock cycle time	to	200		10000	ns
Clock pulse width[1]	tw	50			ns
Clock duty cycle		25	50	75	%
Data setup time	tds	20			ns
Data hold time	tdh	20			ns
Prohibit crossing time[2]	tprh		20		ns
EOS rise delay	terdl		60		ns
EOS fall delay	tefdl		70		ns
Signal delay time[3]	tdl		20		ns
Signal settling time[3]	ts/h		120		ns

Notes:

1. Since the clock pulse width varies with the frequency, tw will vary according to duty cycle.
2. Prohibit crossing time is to insure that no two SPs are locked into the shift register for any single scan time. Since the SP is entered into the shift register during its active high level when the CP clock edges falls, the active high of the SP is permitted only during one falling, CP clock edges for any given scan. Otherwise, multiple SPs will load into the shift register.
3. Pixel delay times and settling time depend on the output amplifier, which is employed. These values, tdl and ts/h, are measured with the amplifier see in Figure 9 using the AMIS-720233-B sensors. Note: The impulse signal current out of the device has pulse width ~ 30ns. Hence, the faster the amplifier with a faster settling time will yield a signal video pulse with faster rise and settle times.

9.0 Typical A6 CIS Module Circuit

Figure 9 depicts a typical A6 CIS module circuit using the AMIS-720233-B sensors. The circuit is provided as a reference to illustrate the interconnection of the AMIS-720233-B with a serially cascaded line of image sensors. It is a typical A6 size CIS module produced by AMIS. It provides the first-time user with additional insight for designing a CIS module and supplements the circuit descriptions given in Section 5.

The difference is in the arrangement of the two shunt switches - U2D and U2A. U2D is a counterpart to SW in

Figure 5. A DC restoration capacitor, C20, with value of 100pf is added between the shunt's switch. The first, U2D, clamps the video line to ground to reset the image sensors. Simultaneously the second, U2A, clamps the node between C20 and amplifier input to an output reference bias voltage that is on the node between R4 and R9. These resistors are voltage dividers that set the DC operating level of the amplifier's output by applying same bias voltage to both inputs of the amplifier. See Figure 9.

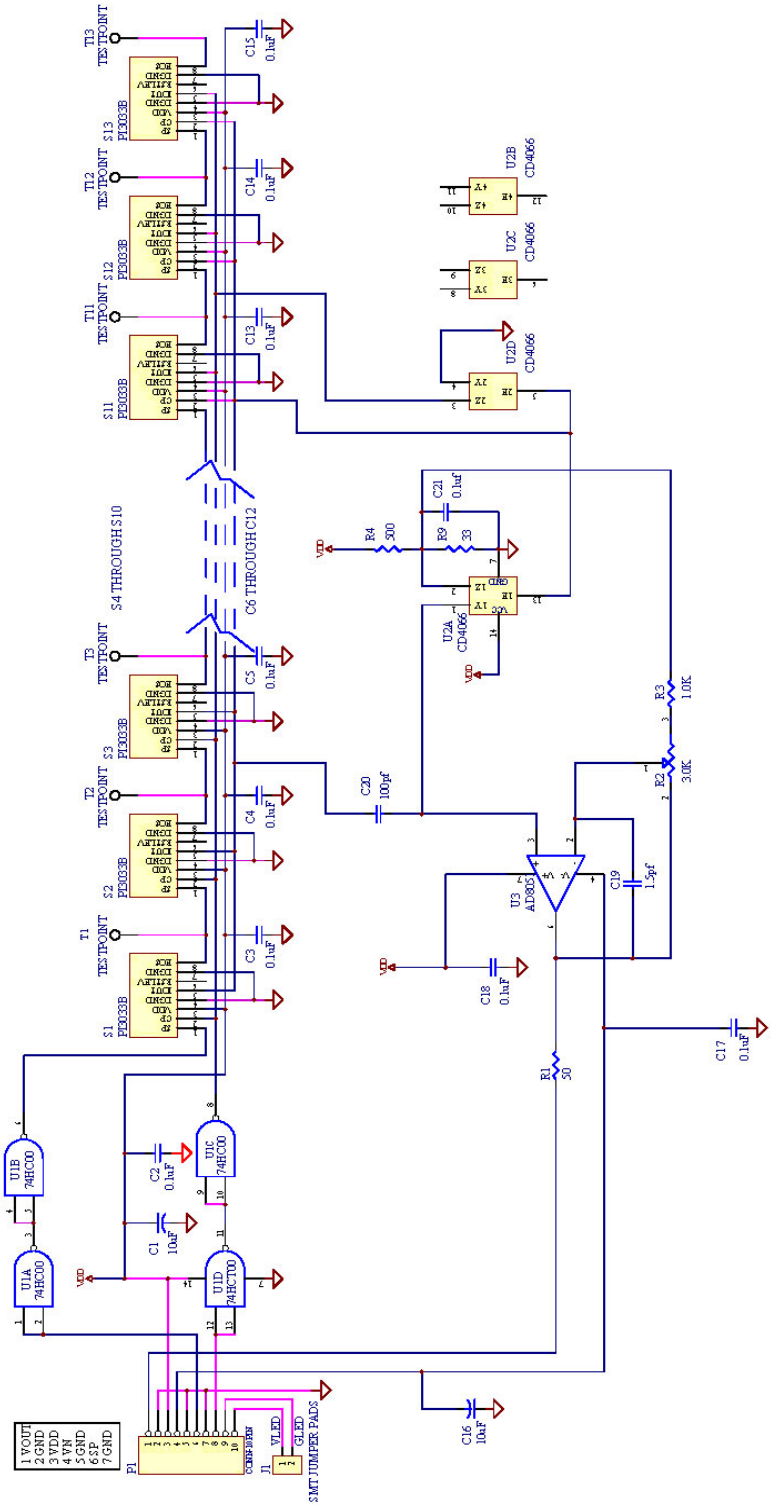


Figure 9: Typical A6 CIS Module Circuit

10.0 Company or Product Inquiries

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