

# AN5650

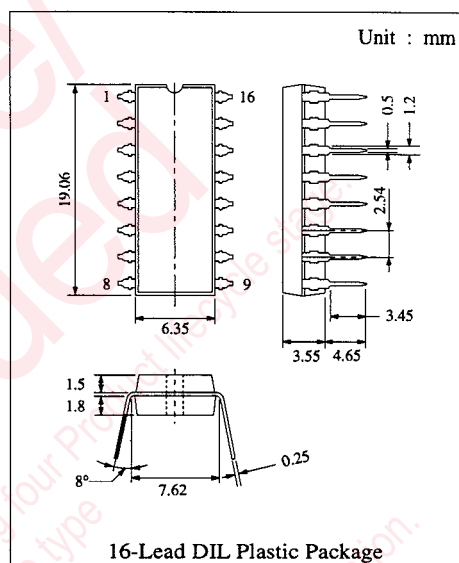
## Colour TV Synchronization Signal Processing Circuit

### ■ Description

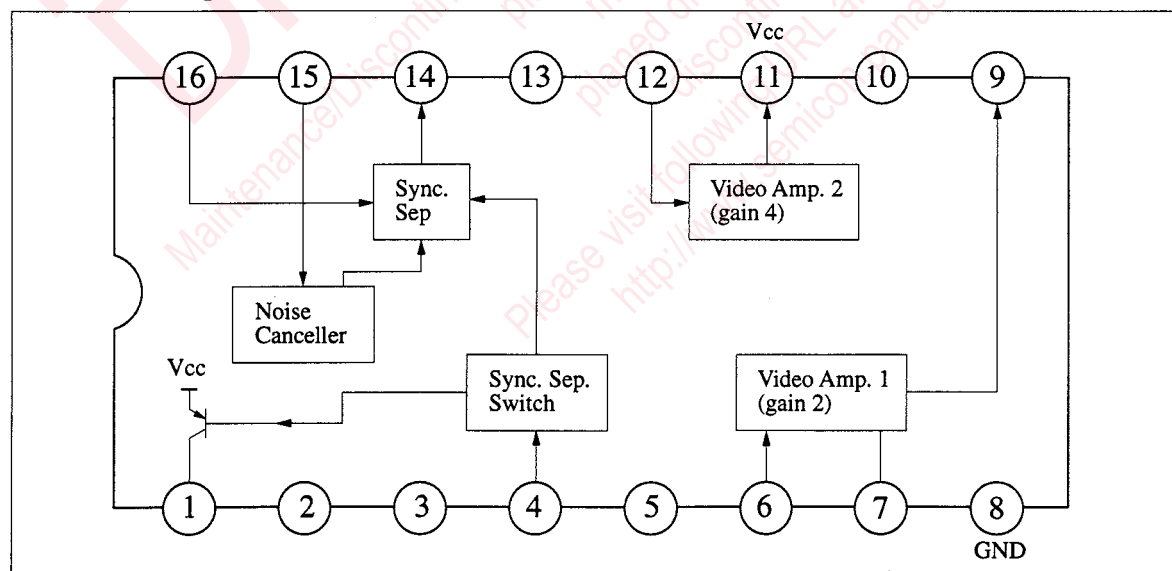
The AN5650 is an integrated circuit designed for colour TV synchronizing signal processing circuit.

### ■ Features

- Built-in video signal amplifier circuit
- A synchronizing separation circuit highly stable against noise
- Built-in synchronization signal output switching circuit



### ■ Block Diagram



### ■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit		
Voltage	Supply Voltage	V <sub>13-8</sub>	14.4	V	
	Circuit Voltage	V <sub>1-8</sub>	0	V <sub>13-8</sub>	V
		V <sub>4-8</sub>	0	V <sub>13-8</sub>	V
		V <sub>6-8</sub>	0	V <sub>13-8</sub>	V
		V <sub>7-8</sub>	0	V <sub>13-8</sub>	V
		V <sub>12-8</sub>	0	V <sub>13-8</sub>	V
		V <sub>14-8</sub>	0	V <sub>13-8</sub>	V
		V <sub>15-8</sub>	0	6	V
V <sub>16-8</sub>	-3	2	V		
Current	Supply Current	I <sub>13</sub>	40	mA	
	Circuit Current	I <sub>1</sub>	-2	0	mA
		I <sub>7</sub>	-3	0	mA
		I <sub>9</sub>	-5	0	mA
		I <sub>11</sub>	-5	0	mA
		I <sub>14</sub>	0	10	mA
		I <sub>16</sub>	-1	1	mA
Power Dissipation	P <sub>D</sub>	560	mW		
Operating Ambient Temperature	Topr	-20 ~ +70°C	°C		
Storage Temperature	Tstg	-55 ~ +150°C	°C		

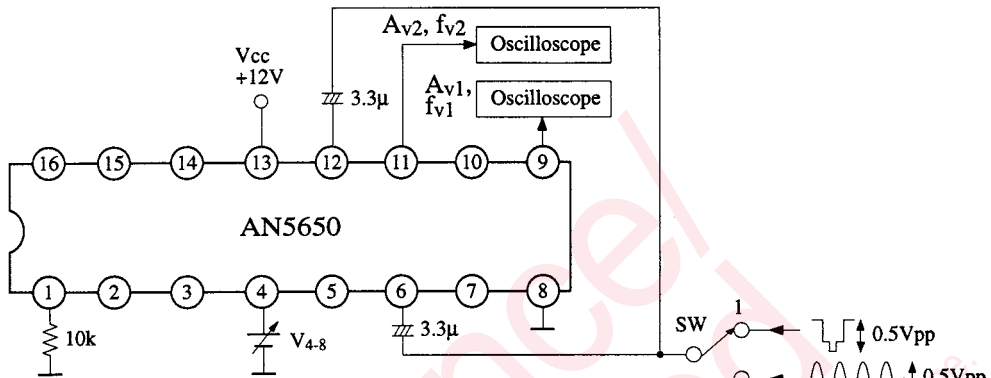
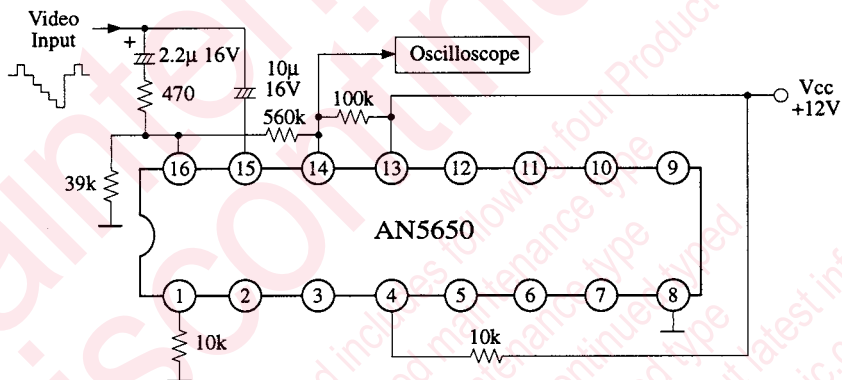
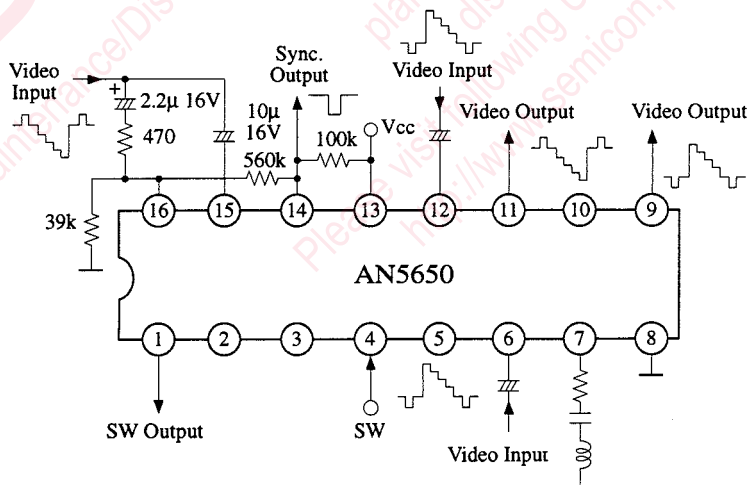
### ■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test Cct	Condition	min.	typ.	max.	Unit
Voltage Gain (Video Amp. 1)	A <sub>v1</sub>	1	Video signal input 0.5Vpp SW1	1.5	1.9	2.3	times
Voltage Gain (Video Amp. 2)	A <sub>v2</sub>	1	Video signal input 0.5Vpp SW2	3.4	3.9	4.3	times
Frequency Characteristics (Video Amp. 1)	f <sub>v1</sub>	1	Sine wave input 0.5Vpp SW2 input frequency when A <sub>v1</sub> becomes -3dB	5			MHz
Frequency Characteristics (Video Amp. 2)	f <sub>v2</sub>	1	Sine wave input 0.5Vpp SW2 input frequency when A <sub>v2</sub> becomes -3dB	5			MHz
Switch Operating Voltage	V <sub>4-8</sub>	1	Switch input voltage when switch output becomes 0.7V or more	1.5			V
Max. Allowable Input (Video Amp. 1)	V <sub>in(max).1</sub>	1	APL = 50%			1.9	Vpp
Max. Allowable Input (Video Amp. 2)	V <sub>in(max).2</sub>	1	APL = 50%			1.4	Vpp
Sync. Sep. Input*	V <sub>in3</sub>	2	V <sub>cc</sub> = 12V, APL = 50%	1.0		2.5	Vpp

\* Design reference value

### ■ Pin Description

Pin No	Pin Name	Pin No	Pin Name
1	Switch Output	9	Video Signal Output 1
2	NC	10	NC
3	NC	11	Video Signal Output 2
4	Sync. Sep. Switch Input	12	Video Signal Input 2
5	NC	13	V <sub>cc</sub>
6	Video Signal Input 1	14	Sync. Sep. Output
7	Gain Control	15	Noise Det. Input
8	GND	16	Video Signal Input 3

**Test Circuit 1** ( $A_{v1}$ ,  $A_{v2}$ ,  $f_{v1}$ ,  $f_{v2}$ ,  $V_{4-8}$ ,  $V_{in(max.)1}$ ,  $V_{in(max.)2}$ )

**Test Circuit 2** ( $V_{in3}$ )

**Application Circuit**


(When input is high, Sync. Sep. and SW Output Operates.)

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