# Low-Power Universal-Input Power Supply Achieves High Efficiency

Expanding global markets have created a demand for what have become known as universal-input power supplies — that is, power supplies that allow devices to be plugged into wall outlets anywhere in the world. These power supplies must be able to operate directly from 100-, 110-, and 220-V ac power lines without the use of selector switches or jumpers. A power supply with the ability to operate under such conditions while remaining cost-effective is now becoming a necessity.

In the under 30-W power range, meeting the above requirements while maintaining high efficiency has been a challenge. Add to this the need to meet various international safety standards, and the circuit designer has his hands full.

The demands of low-power universal-input power supplies are met by the Si9120 pulse width modulation (PWM) controller from Vishay Siliconix. Using the Si9120, the flyback circuit presented in this application note demonstrates that designing universal-input supplies can be a simple task.

## CIRCUIT TOPOLOGY

For the low power levels that are of interest here (under 30 W), the discontinuous-mode (DCM) flyback converter is the preferred topology. The biggest advantage of this topology is simplicity. The parts count in the power path cannot get any lower.

The peak-to-average primary current ratio in a DCM flyback is high relative to other topologies; however, at low power levels, this is not a serious drawback. On-state losses are minimal. Magnetics are small. Also, the transformer reset voltage is set by the minimum input voltage and remains fairly constant as the line voltage changes. As a result, a 600-V MOSFET proves adequate, even with ac inputs up to 300 V RMS.

The DCM flyback converter, when operated under current-mode control, provides a natural input volt-second limit, which helps keep the drain voltage from getting out of control during line or load transient conditions. Also, today's power MOSFETs are able to withstand avalanche current many times greater than a low power circuit can typically deliver (see appendix A). As such, the MOSFET will serve as a clamp for the occasional spike which may result from a short circuit or extreme load transient.

Cross regulation is fairly good, especially if leakage inductance between windings can be kept low.[1] In a universal-input application, meeting VDE input-to-output isolation requirements is essential. Depending on the end product, this can be as high as 3750-V RMS, primary to

secondary — a figure that is totally inconsistent with the desire to achieve low leakage inductance. As a result, cross regulation between primary and secondary- referenced windings will be poor. This complicates the regulation of the primary-side bootstrap winding used to avoid secondary-to-primary feedback across the isolation boundary. The addition of a simple spike-blanking circuit solves the problem (see AN707, "Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC").

When using the Si9120 for universal-input applications, it is recommended that a bootstrap winding be employed. While not strictly necessary, the power dissipation and chip temperature are higher if bootstrapping is not utilized. As an example, at $V_{IN}$ = 400 V dc and $I_{CC}$ = 1.5 mA, the power dissipation on the chip without a bootstrap is 600 mW. If a 10 V bootstrap supply is used, the dissipation is only 15 mW. This becomes more of a concern as the gate charge requirements of the power MOSFET increase, since the value of $I_{CC}$ for the controller is largely dependent on gate drive demands.

Another advantage of the DCM flyback converter is its single-pole loop response. This makes compensating the feedback loop comparatively simple. In addition, transient response can be quite good in DCM flyback converters. It is possible (though not practical in a closed-loop system) to slew the power stage from no load to full load in only one switching cycle.

## DESIGN EXAMPLE

The circuit shown in Figure 1 is an 11.1-W, 3-output off-line supply. The input voltage is specified from 90- to 260-V ac. Outputs are +5 V at 1.5 A, +12 V at 150 mA, and –12 V at 150 mA. The design features full VDE isolation, primary side regulation, and true foldback current limiting. Operating frequency is 100 kHz.

DCM flyback operating principles are generally well understood and will not be presented here. Refer to Vishay Siliconix Application Note AN707 for a detailed design example. References 2 and 3 are also recommended.

Sizing the input capacitor and rectifiers for universal input requires more thought than for comparable single-input converters. Keep in mind that while the maximum input voltage occurs at high-input line, the maximum current stresses will occur at low line. This implies that the input capacitor value must be sized at low line while the voltage rating is dictated by the high-line condition. The bridge rectifier should be rated at 600-V dc minimum. The RMS current rating is calculated below.
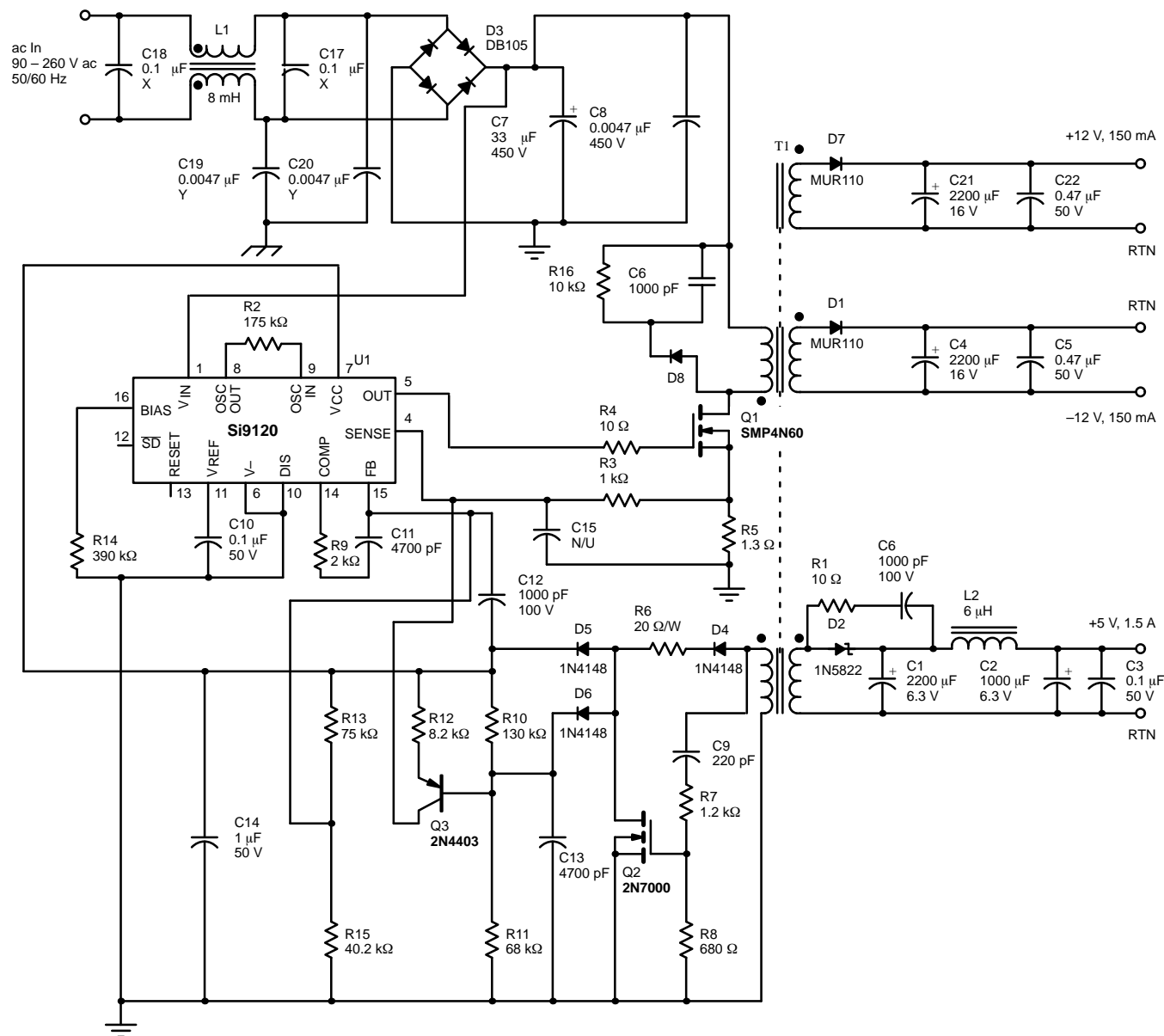
**FIGURE 1.** Schematic for Universal-Input Power Supply

For the present example:

Output power = 5.0 V x 1.5 A + 12 V x 0.15 A x 2 = 11.1 W

If efficiency is assumed to be 70%,

Input power = 11.1 W/0.7 = 15.86 W

For a little cushion, assume a low-input line voltage of 85 V ac.

Thus,

$$V_{dc} = 85\sqrt{2} = 120V \ dc.$$

Assuming a 20-V pk-pk input-capacitor ripple voltage the minimum voltage is

$V_{min}$ = 120 V – 20 V = 100 V.

$I_{in} = P_{in}/V_{DC}$

= 15.86 W/ 100 V = 0.1586 A

$$C = I\frac{dt}{dv}$$

$$= \frac{0.1586 \ A \ x \ 0.01 \ s}{20 \ V}$$

= 79 μF

68 μF is a standard value. With 68 μF, the ripple voltage is

$$V_{pp} = I\frac{dt}{C}$$

$$= \frac{0.16 \ A \ \times \ 0.01 \ s}{68E–6F}$$

= 23.5 V, an acceptable value.

The capacitor voltage rating is calculated:

$$V_{max} = 260 \ V \ ac \ x \ \sqrt{2} = 368 \ V \ dc.$$

A 400-V capacitor is acceptable. A rating of 450-V dc is preferable if high reliability is required or significant line transients are expected.

Assuming a power factor of 0.65, the RMS input current is

$$I_{ac} = \frac{P_o}{h_{ac} \ (PF)}$$

$$= \frac{11.1 \ W}{(0.7) \ (85 \ V) \ (0.65)}$$

= 0.287 A

A 1-A bridge rectifier is more than adequate.

The primary inductance value is chosen by analyzing the lowest input voltage case. For a given load, the value of the peak transformer primary current will remain constant regardless of the input voltage. Since the primary inductance is fixed, the time to ramp to a given value of current is inversely proportional to input voltage (V = Ldi/dt). Therefore, low line is where the most time is needed to ramp to the desired primary current. The duty factor limit dictates an on-time limit. After

choosing an operating frequency and calculating the peak primary current, a value for primary inductance, $L_P$, can be determined as follows:

For 100 kHz, period = 10 μs.

At 50% duty factor, $t_{on(max)}$ = 5 μs.

$I_{pk} = I_{in}$ x 4

= (0.1586 A) (4)

= 0.634 A pk.

For $V_{IN}$ (dc) = 100 V

$$L = V\frac{dt}{I_{pk}}$$

$$= \frac{(100 \ V) \ (5E–6 \ s)}{0.634 \ A}$$

= 788 μH.

The actual inductance used was 735 μH. [For high-volume production applications, the design engineer should consider the worst case tolerances for clock frequency and inductor value.]

See AN707 for transformer design equations and a fully worked example.

The biggest considerations for universal input are related to the additional insulation required to comply with VDE isolation specifications. The physical space occupied by the insulation typically reduces the useable fill factor to 25%. Furthermore, the increase in leakage inductance caused by large physical separation of the windings has the undesirable effects of creating large voltage spikes on the power MOSFET drain, contributing to power losses, and degrading load regulation.

Barrier tape at window ends will take up a lot of useable space, so a core geometry with a long, low window should be selected to minimize wasted area. This has the added benefit of reducing leakage inductance. (See equation 6.4 of reference 4.)

Wind the primary first. Apply the required insulation, and then wind the secondaries. All secondaries should be wound together with no intervening insulation, if voltage levels allow. Optimal cross regulation is achieved in this way.

Further reductions in leakage inductance can be realized by using interleaved windings. First wind one half of the primary, followed by the secondaries and remaining primary turns. The multiple primaries are usually connected in parallel. The spike blanking circuit described in AN707 virtually eliminates the primary-to-secondary leakage inductance problems, at least from the standpoint of the regulation effects.

In selecting a power MOSFET, the main concerns will be the $r_{DS(on)}$ and the drain voltage ratings. The transformer primary voltage during the off time is $V_P = (V_O + V_D) N_P/N_S$. Using the 5-V winding,

$V_P = (5.0\ V + 0.4\ V)(45\ T/3\ T) = 81$

Therefore,

$V_{DS(off)} = V_{IN(max)} + V_P = 368\ V + 81\ V = 449\ V.$

A 600 V MOSFET allows for a 150 V spike due to leakage inductance at high line. The RC snubber was sized empirically to keep the peak drain voltage below 600 V.

The SMP4N60 is the smallest 600-V device available. At 25°C the $r_{DS(on)}$ is 2.0 Ω. At 100°C, $r_{DS(on)} = 1.75 \times 2\ \Omega = 3.5\ \Omega$. The peak drain current was previously calculated at 0.634 A. The maximum RMS drain current is given by

$$I_{RMS} = I_{pk}\left(\frac{D}{3}\right)^{\frac{1}{2}} = 0.634A\left(\sqrt{\frac{0.5}{3}}\right) = 0.26\ A$$

On-state losses are given by

$P_{on} = I_{RMS}^2 \times r_{DS(on)}$

$\quad = (0.26\ A)^2 \times 3.5\ \Omega$

$\quad = 237\ mW.$

Switching losses are estimated at 350 mW. Since the thermal resistance is specified at 80°C/W, a total temperature rise of 47°C is expected. This permits operation up to approximately 50°C ambient temperature, while holding the maximum junction temperature to 100°C.

Something of more concern for universal-input than for a single-input voltage supply is the range of duty factor to be expected. Since the on time varies inversely with input voltage, the high-line on-time can become quite small in a high-frequency converter. For this kind of application, try to keep the minimum on time to not much less than 1 μs. This will help minimize noise problems with the current sense.

Also, be sure to use a non-inductive resistor for the current sense (carbon composition or film type). Use of a wire-wound resistor will produce large spikes which have to be filtered out. The dual-delay current-limit comparators of the Si9120 will frequently eliminate the need for a current-sense filter altogether. The magnitude of the noise on the current sense voltage will be affected by transformer parasitic capacitances and PCB layout. As such, every design will exhibit slightly different characteristics. Careful attention to detail in the magnetics design and construction as well as the board layout is a must.

For designs using current-sense resistors in the power MOSFET's source leg, note that the gate drive current is "seen" by the sense resistor. In very low-power designs, this can easily exceed the full load sense voltage causing severe noise problems. Adding a fairly large-value gate resistor will help in this case. Also, an RC current-sense filter becomes much more important.

## FOLDBACK CIRCUIT

Foldback current limiting is provided by Q3 and its associated components. Under normal operating conditions, diode D6

keeps C13 charged to $V_{CC}$. Hence, Q3 is biased off. In the event of a short circuit on any output, all winding voltages are clamped low. This causes the voltage on C13 to drop to a level set by divider R10 and R11. $V_{CC}$ is held at 8.6 V by the Si9120's start-up regulator. The current set by the value of R12 flows through Q3 and R3, and causes the voltage on pin 4 to rise. Since a peak threshold of 1.2 V is internally set on pin 4, the voltage required across R5 to terminate a pulse is reduced by an amount equal to the drop on R3.

$I_D = \{1.2 - (I_{Q3})(R3)\}/R5.$

Thus as $I_{Q3}$ increases, $I_D$ decreases.

See Figure 2a for foldback operating waveforms.

The foldback circuit will not perform correctly without the spike blanking circuit. The leakage spike will peak charge C13 even with a shorted load. However, the foldback function is completely optional and all associated components can be eliminated if a lower cost supply is desired.

## TEST RESULTS

Data compiled on the test circuit appear in Table 1. Combined line and load regulation measures ±2.7%, well within a ±5% specification. Measured efficiency is 73.4% with no effort at optimization. A detailed loss assessment could, no doubt, offer some improvements. Pulse load tests show reasonable transient response, and phase margin is measured at 60 degrees. For details on how to close the feedback loop, refer to Vishay Siliconix application notes AN713 and AN707.

All data taken with dc input source to ensure stable readings.

### TABLE 1. UNIVERSAL-INPUT SUPPLY TEST DATA

| Full Load: | | | | |
|---|---|---|---|---|
| $V_{IN}$ (dc) | $I_{in}$ (mA) | +5 V | +12 V | −12 V |
| 100 V | 143.9 | 4.974 | 12.64 | 12.50 |
| 200 V | 72.3 | 5.014 | 12.76 | 12.61 |
| 300 V | 48.9 | 5.027 | 12.79 | 12.65 |
| 385 V | 39.4 | 5.049 | 12.81 | 12.67 |
| Half Load: | | | | |
| 100 V | 78.0 | 5.153 | 12.99 | 12.83 |
| 200 V | 40.3 | 5.205 | 13.10 | 12.96 |
| 300 V | 27.9 | 5.235 | 13.12 | 12.97 |
| 385 V | 23.0 | 5.254 | 13.14 | 13.01 |

### PK-PK OUTPUT RIPPLE VOLTAGES (SPIKES NOT INCLUDED)

| 5 V | +12 V | −12 V |
|---|---|---|
| 60 mV | 45 mV | 40 mV |

Note: Worst case over full line-voltage range.

a)

Short Circuit On 5 V Output

Q1 Drain Voltage (100 V/Div)

Voltage On U1, Pin 4 (Current Sense)
(0.5 V/Div)

NOTE: 0.8 V dc pedestal caused by
the foldback circuit.

b)

Q1 Drain Voltage (100 V/Div)

Q1 Gate Voltage (100 V/Div)

c)

Q1 Gate Drive (5 V/Div)
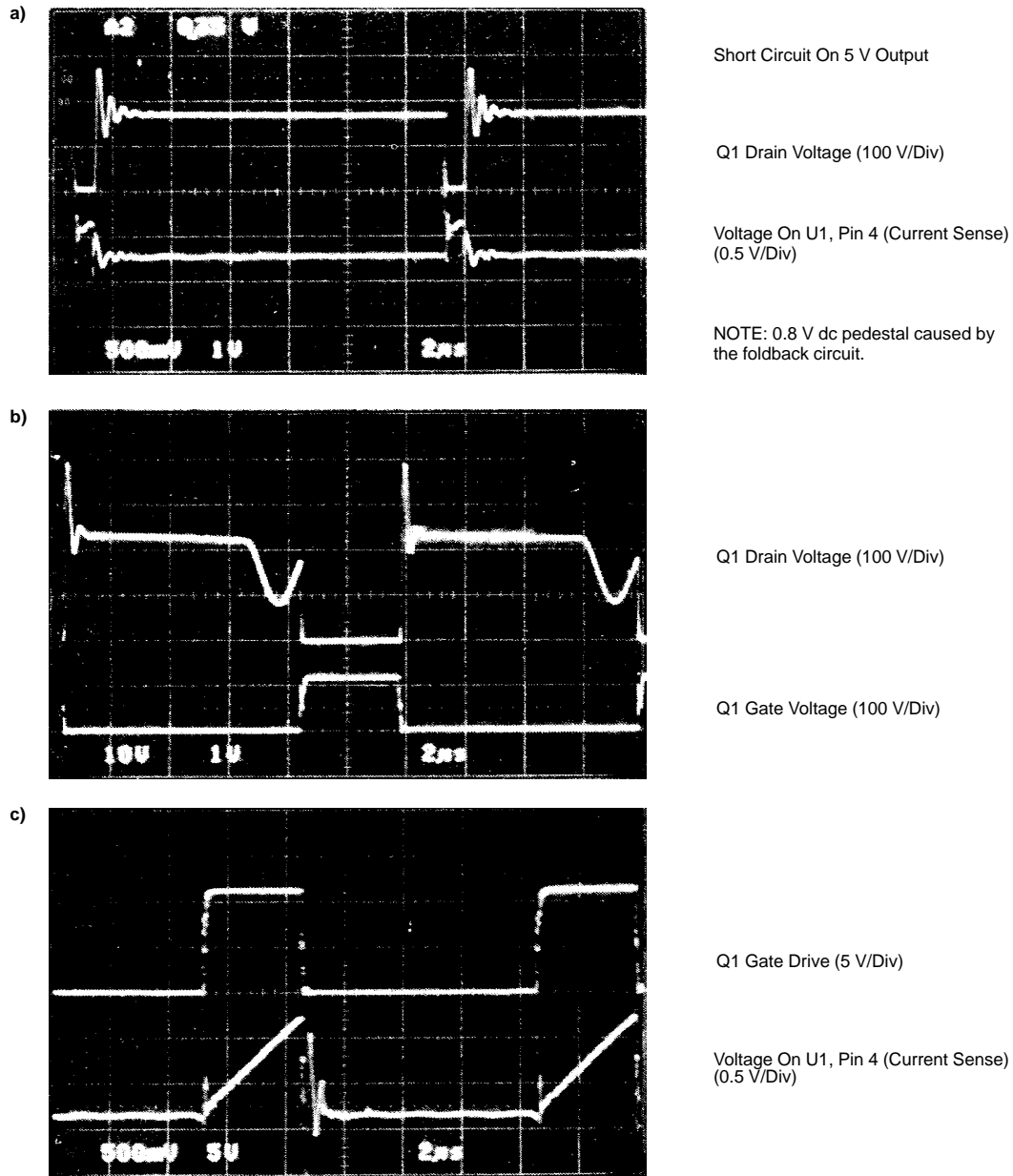
Voltage On U1, Pin 4 (Current Sense)
(0.5 V/Div)

**FIGURE 2.** Operating Waveforms (all photos full load, $V_{IN}$ = 150 V dc)

Measured efficiency at $V_{IN}$ = 300 $V_{DC}$ was 73.4%.

During testing, an input capacitor value of as little as 33 $\mu$F proved adequate versus the design value of 68 $\mu$F. The low-value capacitor produces an input ripple voltage of 30 V pk-pk. Since the primary inductance is slightly lower than the design maximum value, the circuit is still able to maintain regulation with the higher input ripple voltage value. This is a

good example of where trade-offs can be made during development programs. By using the larger input capacitance and primary inductance, the peak input current could be reduced slightly, and a slight improvement in efficiency should result. However, a larger input capacitance will decrease the conduction angle of the input rectifiers, and consequently will reduce the input power factor. The priorities of a particular application will determine the optimal approach.

## CONCLUSION

The simple universal-input power supply design that has been presented combines economy and performance which should prove more than adequate for the majority of applications. The overall cost of the supply should rival linear regulators of similar power level if heatsink cost is considered. Good regulation has been achieved while maintaining the 3750-V ac input-to-output isolation mandated by VDE. The Si9120 eliminates the need for any external start-up circuitry. Also, foldback current-limiting is demonstrated which requires no feedback across the isolation boundary.

## APPENDIX A

The SMP4N60 was tested for ability to withstand repetitive avalanche currents and for non-repetitive capability. Inductance values of 12 $\mu$H and 94 $\mu$H were used. Repetitive tests were run at 3 A, with 94 $\mu$H at 25°C. Failure current was measured at 25°C and 100°C. Results were as follows:

| L = 94 $\mu$H | | L = 12 $\mu$H | |
|---|---|---|---|
| 25°C | 100°C | 25°C | 100°C |
| 4.25 A | 2.40 A | 7.28 A | 6.40 A |

For the 11.1-W flyback supply presented here, the leakage inductance is specified at 60 $\mu$H maximum. The maximum drain current is set to approximately 1.0 A. Therefore, based on the above data, adequate margin is present to prevent avalanche failure.

## APPENDIX B

A number of performance parameters of the Si9120 can be altered by setting $I_{bias}$ to a value other that 15 $\mu$A. At lower $I_{bias}$, higher efficiency can be obtained. At higher $I_{bias}$, lower propagation delays and a wider error amplifier bandwidth are possible. Also, if a $V_{CC}$ supply other than 10 V is used, $R_{bias}$ should be something other than 390 k$\Omega$. Figure 3 below relates $V_{CC}$ to $R_{bias}$ and typical $I_{bias}$. The equation given can be used for points not on the graph.
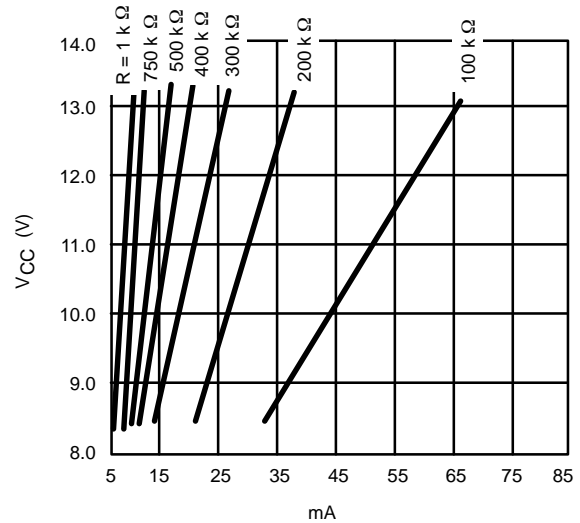


$$R_{bias} = \frac{V_{CC} - 2.3\ V - 484\ \sqrt{I_{bias}}}{I_{bias}}$$

**FIGURE 3.** Relationship of $V_{CC}$ to $R_{bias}$ an Typical $I_{bias}$

### REFERENCES

1) Liu, K.H., "Effects of Leakage Inductance on the Cross Regulation in a Discontinuous-Mode Flyback Converter," Proceedings, 1989 High Frequency Power Conference, Naples, Florida.

2) Chryssis, G., "High Frequency Switching Power Supplies," McGraw Hill 1984.

3) Billings, K., "Switchmode Power Supply Handbook," McGraw Hill 1989.

4) McLyman, Col. W.T., "Transformer and Inductor Design Handbook," McGraw Hill 1988.

## UNIVERSAL INPUT POWER SUPPLY PARTS LIST

C1 . . . . . . . . . . . . . 2200 µF, 6.3 V Al. Electrolytic – United Chemicon SXC

C2 . . . . . . . . . . . . . 1000 µF, 6.3 V Al. Electrolytic – United Chemicon SXC

C3, C10 . . . . . . . . 0.1 µF, 50 V Ceramic, Vishay Vitramon VJ1206Y104KXAAT

C4, C21 . . . . . . . . 2200 µF, 16 V Al. Electrolytic – United Chemicon SXC

C5, C22 . . . . . . . . 0.47 µF, 50 V Ceramic, Vishay Vitramon VJ1210Y474KXAAT

C6, C12 . . . . . . . . 1000 pF, 100 V Ceramic. Vishay Vitramon VJ1206Y102KXBAT

C7 . . . . . . . . . . . . . 33 µF, 450 V Al Electrolytic (400 V ok)

C9 . . . . . . . . . . . . . 220 pF, 100 V Ceramic, Vishay Vitramon VJ1206A221KXBAT

C11, C13 . . . . . . . . 4700 pF, 100 V Ceramic, Vishay Vitramon VJ1206Y472KXBAT

C14 . . . . . . . . . . . . 1 µF, 50 V Ceramic, Vishay Vitramon VJ1812Y105KXAAT

C16 . . . . . . . . . . . 75 pF, 500 V Ceramic or Mica, Vishay Vitramon VJ1206A750KXEAT

C17, C18 . . . . . . . 0.1 µF, 250 V,ac VDE Class X2 Wima MKS 4-R, Vishay Roederstein F17724102000

C8, C19, C20 . . . . 0.0047 µF, 250 V,ac VDE Class Y Wima MP3-Y, Vishay Roederstein F17724102000

D1, D7 . . . . . . . . . MUR 110 Motorola 1 A 100 V

D2 . . . . . . . . . . . . . 1N5822 3 A, 40 V Schottky

D3 . . . . . . . . . . . . . Bridge 1 A, 600 V DB105

D4, D5, D6 . . . . . . 1N4148

L1 . . . . . . . . . . . . . Common mode choke Renco 1361-2

L2 . . . . . . . . . . . . . Inductor 6 µH, 1.5 A, Vishay Dale ILS-1206-6 µH ± 10%

Q1 . . . . . . . . . . . . FET N-channel SMP4N60 Vishay Siliconix

Q2 . . . . . . . . . . . . FET N-channel 2N7000 Vishay Siliconix

Q3 . . . . . . . . . . . . 2N4403 PNP (or 2N2907)

R1, R4 . . . . . . . . . 10 Ω, $^1/_8$ Carbon Film or Metal Film, Vishay Dale TNPW120610R0FT2

R2 . . . . . . . . . . . . . 175 kΩ, $^1/_8$ W Carbon Film or Metal Film, Vishay Dale TNPW12061753FT2

R3 . . . . . . . . . . . . . 1 kΩ, $^1/_8$ W Carbon Film or Metal Film, Vishay Dale TNPW12061001FT2

R5 . . . . . . . . . . . . . 1.3 Ω, $^1/_4$ W Metal Film

R6 . . . . . . . . . . . . . 20 Ω, $^1/_2$ W Metal Film

R7 . . . . . . . . . . . . . 1.2 kΩ, $^1/_8$ W Metal Film, Vishay Dale TNPW12061201FT2

R8 . . . . . . . . . . . . . 680 Ω, $^1/_8$ W Metal Film, Vishay Dale TNPW12066800FT2

R9 . . . . . . . . . . . . . 2 kΩ, $^1/_8$ W Metal Film, Vishay Dale TNPW12062001FT2

R10 . . . . . . . . . . . 130 kΩ, $^1/_8$ W Metal Film, Vishay Dale TNPW12061303FT2

R11 . . . . . . . . . . . . 68 kΩ, $^1/_8$ W Metal Film, Vishay Dale TNPW12066802FT2

R12 . . . . . . . . . . . 8.2 kΩ, $^1/_8$ W Metal Film, Vishay Dale TNPW12068201FT2

R13 . . . . . . . . . . . 75 kΩ, $^1/_8$ W 1% Metal Film, Vishay Dale TNPW12067502FT2

R14 . . . . . . . . . . . 390 kΩ, $^1/_8$ W Metal Film, Vishay Dale TNPW12063903FT2

R15 . . . . . . . . . . . 40.2 kΩ, $^1/_8$ W 1% Metal Film, Vishay Dale TNPW12064022FT2

R16 . . . . . . . . . . . 330 Ω, $^1/_2$ W 5% Carbon Composition

T1 . . . . . . . . . . . . . Schott Corp. #67122700