

Single-Channel 1206A ChipFET™ Power MOSFET Recommended Pad Pattern and Thermal Performance



ON Semiconductor™

<http://onsemi.com>

APPLICATION NOTE

INTRODUCTION

New ON Semiconductor ChipFETs in the leadless 1206A package feature the same outline as popular 1206A resistors and capacitors but provide all the performance of true power semiconductor devices. The 1206A ChipFET has the same footprint as the body of the TSOP-6 and can be thought of as a leadless TSOP-6 for purposes of visualizing board area, but its thermal performance bears comparison with the much larger SO-8.

This technical note discusses the single-channel ChipFET 1206A pin-out, package outline, pad patterns, evaluation board layout and thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the single-channel 1206A ChipFET device. The pin-out is similar to the TSOP-6 configuration, with two additional drain pins to enhance power dissipation and thermal performance. The legs of the device are very short, again helping to reduce the thermal path to the external heatsink/pcb and allowing a larger die to be fitted in the device if necessary.

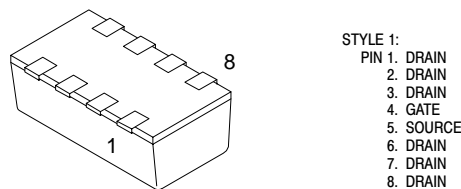


Figure 1. Single 1206A ChipFET

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 2. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern, shown in Figure 3, improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is

0.0054 sq. in. or 3.51 sq. mm. This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further. An example of this method is implemented on the Evaluation Board described in the next section (Figure 4).

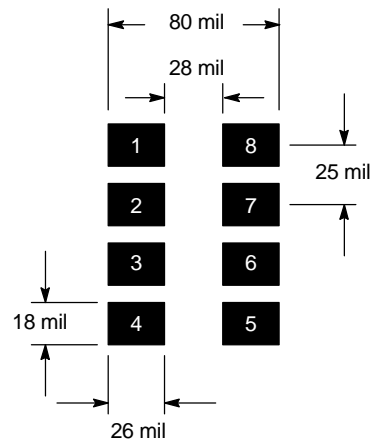


Figure 2. Basic Pad Layout

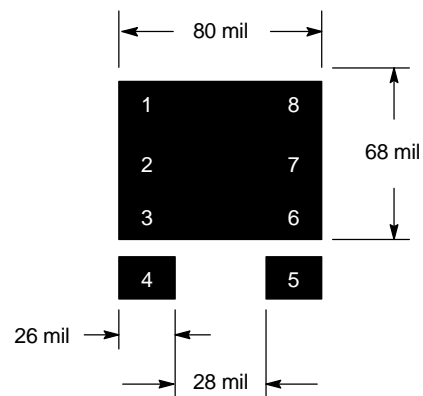


Figure 3. Minimum Recommended Pad Pattern

EVALUATION BOARD FOR THE SINGLE 1206A

The ChipFET 1206A evaluation board measures 0.6 in by 0.5 in. Its copper pad pattern consists of an increased pad area around the six drain leads on the top-side – approximately 0.0482 sq. in. 31.1 sq. mm – and vias added through to the underside of the board, again with a maximized copper pad area of approximately the board-size dimensions. The outer package outline is for the

8-pin DIP, which will allow test sockets to be used to assist in testing.

The thermal performance of the 1206A on this board has been measured with the results following on the next page. The testing included comparison with the minimum recommended footprint on the evaluation board-size pcb and the industry standard one-inch square FR4 pcb with copper on both sides of the board.

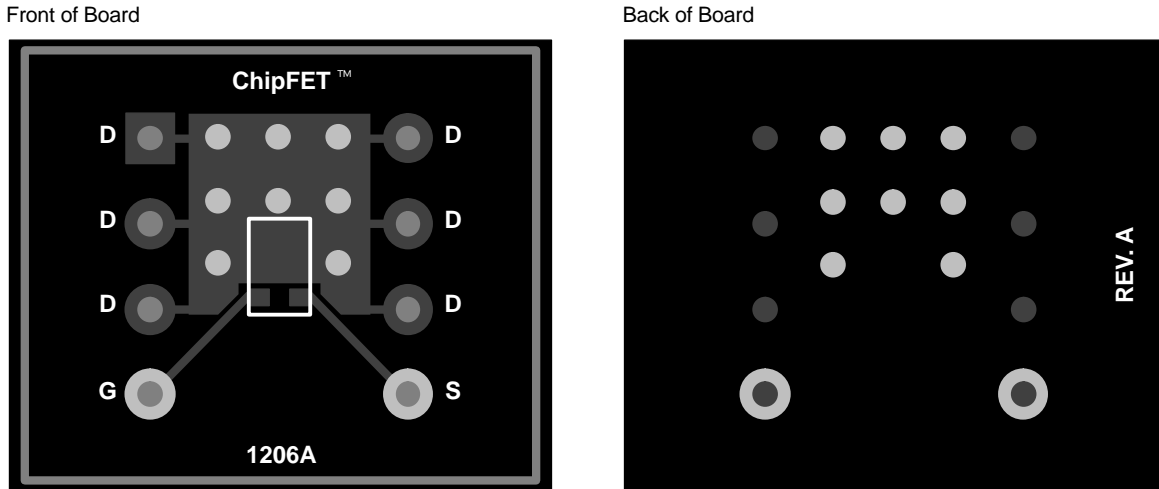


Figure 4. Evaluation Board

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the 1206A ChipFET measured as junction-to-foot thermal resistance is 15°C/W typical, 20°C/W maximum for the single device. The “foot” is the drain lead of the device as it connects with the body. This is identical to the SO-8 package $R_{\theta JF}$ performance, a feat made possible by shortening the leads to the point where they become only a small part of the total footprint area.

Junction-to-Ambient Thermal Resistance (dependent on pcb size)

The $R_{\theta JA}$ typical for the single-channel 1206A ChipFET is 80°C/W steady state, compared with 68°C/W for the SO-8. Maximum ratings are 95°C/W for the 1206-8 versus 80°C/W for the SO-8.

Testing

To aid comparison further, Figure 5 illustrates ChipFET 1206A thermal performance on two different board sizes and three different pad patterns. The results display the

thermal performance out to steady state and produce a graphic account of how an increased copper pad area for the drain connections can enhance thermal performance. The measured steady state values of $R_{\theta JA}$ for the single 1206A ChipFET are:

Minimum recommended pad pattern (see Figure 3) on the evaluation board size of 0.5 in. x 0.6 in.	156°C/W
The evaluation board with the pad pattern described on Figure 4	111°C/W
Industry standard 1" square pcb with maximum copper both sides.	78°C/W

The results show that a major reduction can be made in the thermal resistance by increasing the copper drain area. In this example, a 45°C/W reduction was achieved without having to increase the size of the board. If increasing board size is an option, a further 33°C/W reduction was obtained by maximizing the copper from the drain on the larger 1" square pcb.

AND8044/D

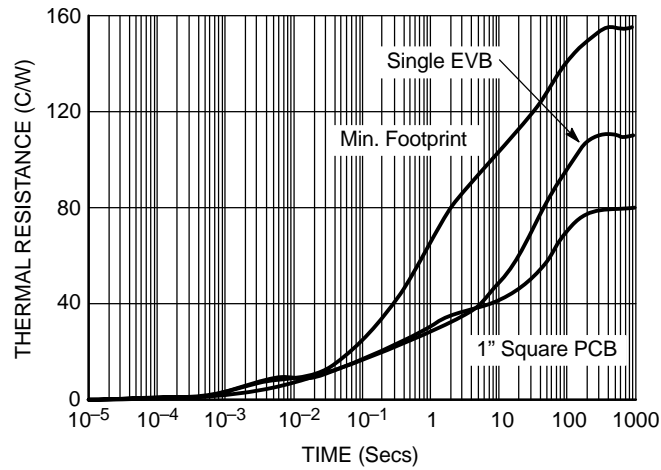


Figure 5. Single 1206A ChipFET

SUMMARY

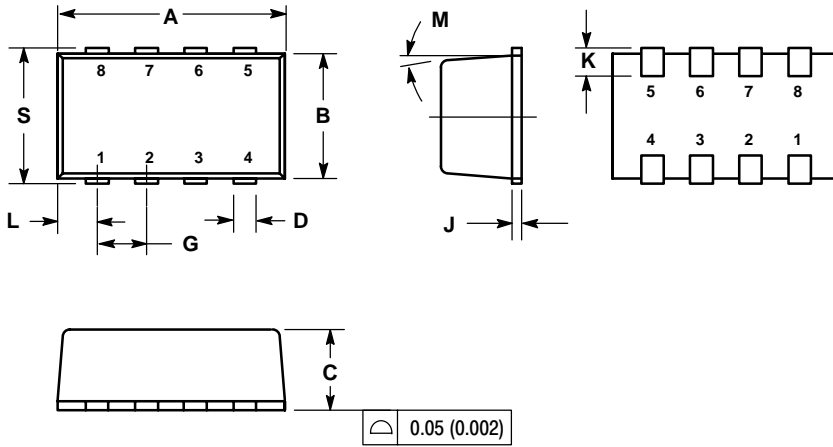
The thermal results for the single-channel 1206A ChipFET package display similar power dissipation performance to the SO-8 with a footprint reduction of 80%.

Careful design of the package has allowed for this performance to be achieved. The short leads allow the die size to be maximized and thermal resistance to be reduced within the confines of the TSOP-6 body size.

AND8044/D

PACKAGE DIMENSIONS

ChipFET
CASE 1206A-02
ISSUE B




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 126A-01 OBSOLETE. NEW STANDARD IS 1206A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.90 BSC		0.076 BSC	

ChipFET is a trademark of Vishay Siliconix.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.