A Low Cost DDR Memory Power Supply Using the NCP1571 Synchronous Buck Converter and a LM358 Based Linear Voltage Regulator

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APPLICATION NOTE

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INTRODUCTION

This application note describes a low cost power supply circuit for a DDR (Double Data Rate) memory system. The design is based on the NCP1570/NCP1571 low voltage synchronous buck converter. The reference design created to evaluate the system uses a 3.80″ by 2.15″ two layer printed circuit board, optimized for a small solution size at an economical cost.

DDR memories bring new challenges to the power supply by requiring an efficient main power of 2.5 V (V_{dd}) and a second voltage (V_{tt}) that accurately tracks one half of V_{dd} (i.e. 1.25 V) that is capable of both sourcing and sinking current. In addition, a third voltage is required (V_{REF}) that also tracks $V_{dd}/2$. A low voltage synchronous buck converter is used to create an 8.0 A output at 2.5 V, while the V_{tt} and V_{REF} voltages are created using a unique operational amplifier linear regulator circuit. The demonstration circuit is designed for low power DDR systems such as desktop PCs, but the circuit's output power capability can be increased with the selection of the external inductor and capacitors for high power systems such as PC workstations.

DDR Memory Power Supply Requirements

Figure 1 shows a simplified schematic of the DDR memory system. Voltage V_{dd} powers the memory ICs, in addition to the buffer interface circuits. The termination voltage V_{tt} is used for the pull-up resistors and must be able to either sink or source current. For example, if all of the driver circuits are at a logic high state (i.e. $V_{OH} = V_{dd} =$ 2.5 V), the Vtt supply will have to sink current in order to maintain its 1.25 V. In contrast, if all of the driver circuits are at a logic low state (i.e. $V_{OL} = V_{ss} = 0$ V), the Vtt supply will have to source current because the termination resistors will be effectively connected to ground.

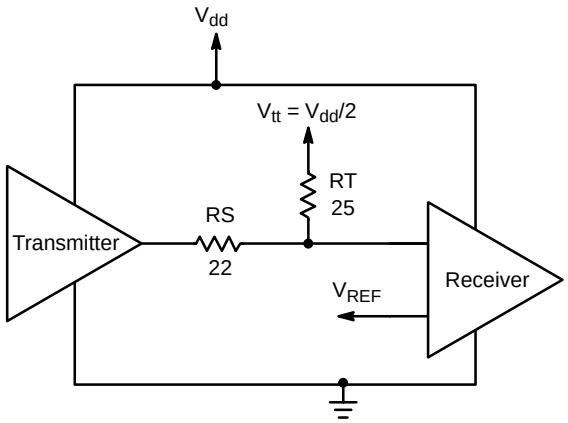


Figure 1. DDR Memory Simplified Schematic

V_{tt} is equal to $V_{dd}/2$ instead of V_{dd} in order to save power. The power dissipated in the resistors is equal to voltage squared divided by the bus resistance, thus a termination voltage of $V_{dd}/2$ provides a factor of four power savings. The third voltage is used as a reference voltage to the differential amplifier input section of the receiver ICs.

A summary of the specifications for the DDR memory system is listed below. The transient requirements are not defined in the industry JEDEC standards.

DDR Voltage	Output Voltage	Tolerance	Output Current
V_{dd}	2.5 V	±200 mV	8.0 A
V_{tt}	$V_{dd}/2$ (≅1.25 V)	$V_{dd}/2$ ± 3% (1.250 V ± 37.5 mV)	±2.0 A (Sink and Source)
V_{REF}	$V_{dd}/2$	V_{tt} ± 40 mV	5.0 mA

Many industry experts have predicted that DDR memory will soon become the standard for desktop computers, with notebooks shortly behind. Next generation DDR-II generation systems are likely to have a lower V_{dd} voltage of 1.8 V with a V_{tt} and V_{REF} voltage equal to 900 mV. This lower voltage will be required to satisfy the consumer's requirement for more memory without a large increase in required power.

Supply Voltage (V_{dd})

The V_{dd} 2.5 V power supply is created with the NCP1571 low voltage synchronous buck controller. The NCP1571 controller contains the required circuitry for a synchronous N-channel MOSFET buck regulator. The $V^{2™}$ control method is used to achieve a fast 200 ns transient response and an output regulation of ±1.0%. The IC operates at a fixed internal frequency of 200 kHz. In addition, the NCP1571 provides the following features: undervoltage lockout protection, programmable soft start, power good signal with delay and overvoltage protection. Note the NCP1570 and NCP1571 are functionally and pin for pin equivalent. The NCP1571's under voltage lockout operation (UVLO) feature has been modified for applications that require a parallel standby power supply in addition to the main power supplied by the buck converter.

Termination Supply Voltage (V_{tt}) and Reference Voltage (V_{REF})

The V_{tt} supply voltage is equal to one half of the Vdd voltage, or approximately 1.25 V. Operational amplifiers U_{2A} and U_{2B} function as voltage followers to create the V_{tt} voltage. The input to U_{2B} is created by the resistive voltage divider formed by R_5 and R_6 and divides the 2.5 V V_{dd} supply by two to form the V_{REF} reference voltage. Also, U_{2B} provides filtering to remove any of the high frequency switching noise that is results from the synchronous buck converter. The V_{tt} output of the circuit formed by U_{2A} and transistors Q_4 and Q_5 tracks the voltage at the non-inverting terminal by virtue of the voltage follower circuit configuration. Thus, the output of voltage of the V_{tt} supply is referenced to 50% of the 2.5 V V_{dd} supply, rather than an absolute 1.25 V reference.

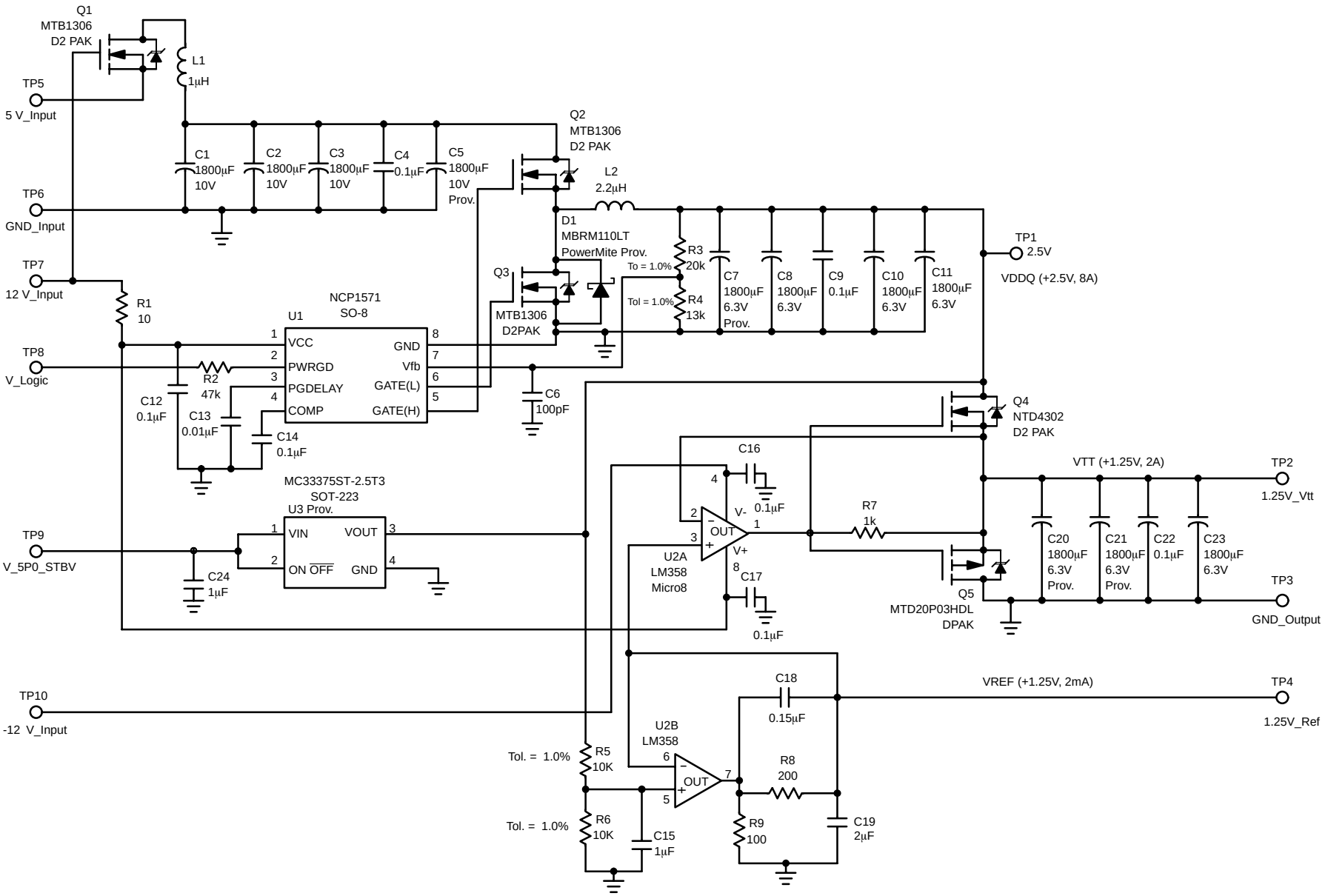
The sink and source ability of the V_{tt} supply is provided by MOSFETs Q_4 and Q_5 which are used to extend the current capability of the operational amplifier circuit. When the V_{tt} supply is in the current sinking mode of operation, Q_4 is "OFF" and Q_5 is "ON". The output of U_{2A} will be at a negative voltage (i.e. –5.0 V) to control the V_{gs} of the P-channel MOSFET (Q_5) in order to maintain the V_{tt} voltage of 1.25 V. In a similar manner, when the V_{tt} supply is in the current sourcing mode of operation, Q_4 is "ON" and Q_5 is "OFF". The output of U_{2A} will reach a positive voltage (i.e. + 4.5 V) to control the V_{gs} of the N-channel MOSFET (Q_5) in order to maintain the V_{tt} voltage of 1.25 V. Resistor R_7 is used to isolate the output of U_{2B} from V_{tt} and the bulk capacitor C_{20}.

The slew rate of the operational amplifier and the ability of the bulk capacitors to hold the voltage at 1.25 V under the load conditions control the transient response of the V_{tt} control loop. Note that the bulk capacitors maintain the V_{tt} voltage at approximately 1.25 V; therefore, the operational amplifier is only required to slew its output a relatively small amount; therefore, the relatively slow slew rate of the LM358 operational amplifiers is not a limiting factor in the design.

Standby Power Operation

The demonstration PCB has the provision of providing a low power standby mode of operation to the DDR memory system. This mode could be used to provide a 2.5 V low current standby voltage to the memory ICs when the main 5.0 V input power is not available. A MC33375 (U_3) 300 mA low dropout voltage regulator (LDO) was chosen for the design to provide the 2.5 V standby power. The MC33375 has an ON/OFF enable pin and is available in a SOT-223 package. The performance of the standby regulator was not verified.

Q_1, a N-Channel MOSFET, serves as a diode to prevent current flow back to the main 5.0 volt input power supply during the standby mode. The MOSFET was chosen instead of a Schottky diode in order to minimize the voltage drop and power consumption of the diode.



Note: The provisional components were not used in the verification of the reference design.

Figure 2. DDR Memory Reference Design

Component Selection

Input Inductor

The input inductor (L_{IN}) is used to isolate the input power supply from the switching portion of the buck regulator. L_{IN} also limits the inrush current into the bulk input capacitors and limits the input current slew rate that results from the transient load. The inductor blocks the ripple current and transfers the transient current requirement to the bulk input capacitor bank.

The design equations for L_{IN} are listed below and for connivance an inductance of 1.0 μH is chosen. The cut-off frequency of the second order LC filter provides adequate attenuation for the 200 kHz switching frequency of the NCP1571.

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{Max}} = \frac{5\ V - 2.5\ V}{10\ A} \times 5\ \mu s = 1.25\ \mu H$$

$$f - 3db = \frac{1}{2\pi \times \sqrt{L_{IN}\ C_{IN}}} = \frac{1}{2\pi \times \sqrt{1\ \mu H \times 5400\ \mu F}} = 216\ Hz$$

where:
L_{IN} = input inductor
C_{IN} = bulk input capacitor(s)
dI/dt = 10 A in 5.0 μs

Input Capacitors

The input filter capacitors provide a charge reservoir that minimizes the supply voltage variations due to the pulsating current through the MOSFETs. The input capacitors are chosen primarily to meet the ripple current rating of the capacitors.

The design equation is listed below.

$$I_{Cin(RMS)} = \sqrt{D \times (1 - D) \times I_{out}^2} = \sqrt{.5 \times (1 - .5) \times 10^2} = 5\ A$$

where:
D = duty cycle = V_{OUT}/V_{IN} = 2.5 V/5.0 V = 0.5
I_{OUT} = maximum output current

The Rubycon 10 V 1800 μf capacitors have a ripple current rating of 2.55 A. Thus only 2 of the capacitors are needed to meet the ripple requirements; however, 3 capacitors were chosen to be conservative.

Output Inductance

The main criterion in selecting the output filter inductance (L_{OUT}) is to provide a satisfactory response to the load transients. The inductance affects the output voltage ripple by limiting the rate at which the current can either increase or decrease. The design equation used for selecting L_{OUT} is listed below. A 2.2 μH inductor was chosen for the design.

$$L_{OUT} = \frac{(V_{IN} - V_{OUT}) \times tr}{\Delta I} = \frac{(5\ V - 2.5\ V) \times 10\ \mu s}{10\ A} = 2.5\ \mu H$$

where:
tr = output transient load time

Output Capacitors

The output capacitors are selected to meet the desired output ripple requirements. The key specifications for the capacitors are their ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance). In order to obtain a good transient response, a combination of low value/high frequency ceramic capacitors and bulk electrolytic capacitors are placed as close to the load as possible.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{tr}{C_{OUT}}\right) \cong \Delta I_{OUT} \times ESR$$

Empirical data indicates that most of the output voltage change that results from the load current transients is determined by the capacitor ESR; therefore, the maximum allowable ESR can be approximated from the following equation.

$$ESR_{max} \cong \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{75\ mV}{10\ A} = 7.5\ m\Omega$$

The number of capacitors is calculated by using the equation listed below.

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{max}} = \frac{19\ m\Omega}{7.5\ m\Omega} = 2.5$$

The ESR of the Rubycon 6.3 V 1800 μF capacitors is specified at 19 mΩ; therefore, 3 capacitors are used in the design.

MOSFET Selection

The output switch MOSFETs are chosen based on the gate charge/gate-source threshold voltage, gate capacitance, on resistance, current rating and the thermal capacity of the package. In this DDR design, the MOSFETs were chosen for economical reasons and have a current and power rating that is much better than needed for this design. In addition, the MOSFETs selected were verified by measuring the thermal characteristics of the devices on the PCB.

The power dissipation design equation for selecting the MOSFETs is given below.

$$P = I_{MAX}^2 \times R_{DS(ON)} \times D + \frac{I_{MAX} \times V_{DS} \times T_r \times F_S}{2} + \frac{I_{MAX} \times V_{DS} \times T_f \times F_S}{2}$$

where:
T_r = rise time or turn-on time of MOSFET
T_f = fall time or turn-off time of MOSFET
F_S = switching frequency

Schottky Diode for Synchronous MOSFET

The efficiency of the buck converter can be improved slightly by placing a Schottky diode (D_1) in parallel with the bottom MOSFET (Q_3). The body diode of Q_3 is used to conduct current during the non-overlap time when both the top (Q_2) and bottom (Q_3) MOSFETs are turned OFF. But because the non-overlap time is only approximately 50 ns for the NCP1571's 200 kHz switching speed, the efficiency savings will be only approximately 1.0%. The demonstration board included a provision for D_1; however, the performance of the circuit was not testing with this diode.

Experimental Results

The experimental results of the demonstration PCB are shown in Figures 4 through 20. Figure 3 shows the test setup used to create the current load transients for the V_{tt} supply voltage. The transient current load tests for the V_{dd} and V_{tt} supply voltages were created using a Kikusui Electronic Load Controller. Unless noted, the standard test conditions are as listed below:

1. Ambient Temperature = 23°C
2. V_{dd} Current Load (I_{Vdd}) = 8.0 A
3. V_{tt} Current Load (I_{Vtt}) = 1.25 A source load
4. V_{REF} Current Load (I_{REF}) = 2.5 mA
5. 5.0 V Input Voltage = 5.00 V
6. 12 V Input Voltage = 12.00 V
7. -12 V Input Voltage = -12.00 V

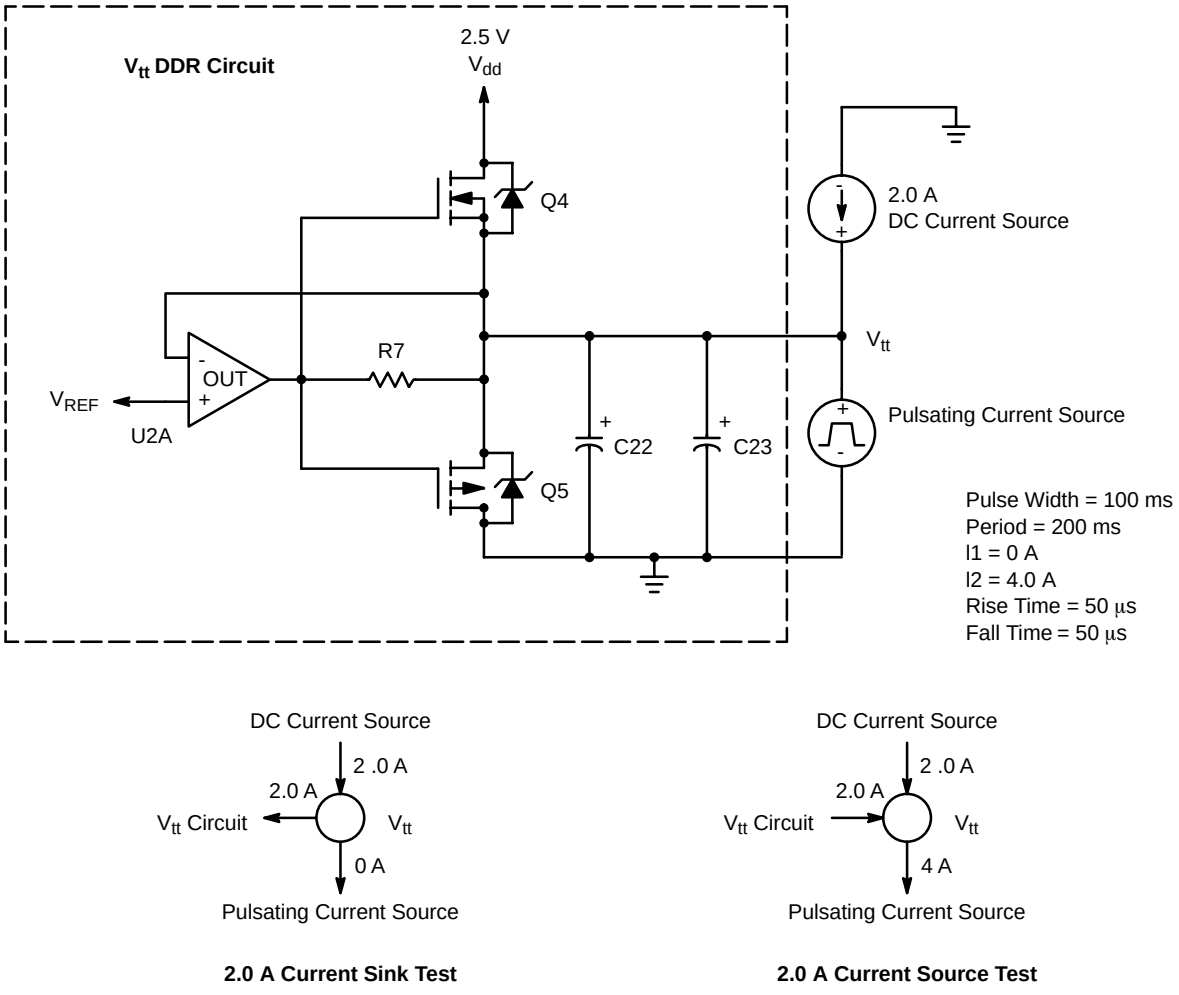


Figure 3. V_{tt} Transient Load Test Setup for a 2.0 A Sink to 2.0 A Source Test

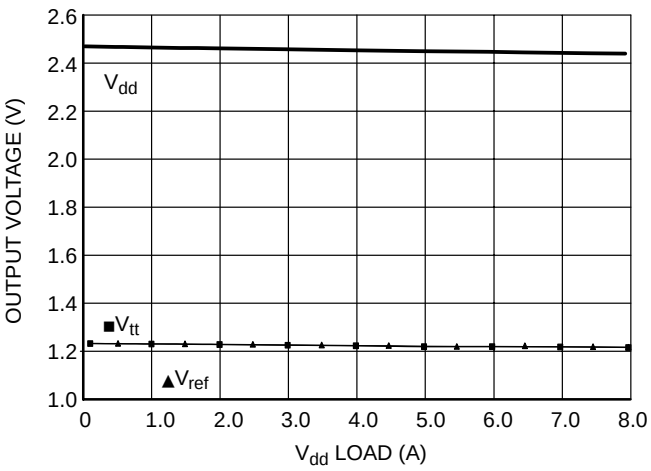


Figure 4. Output Voltage vs. V_{dd} Load

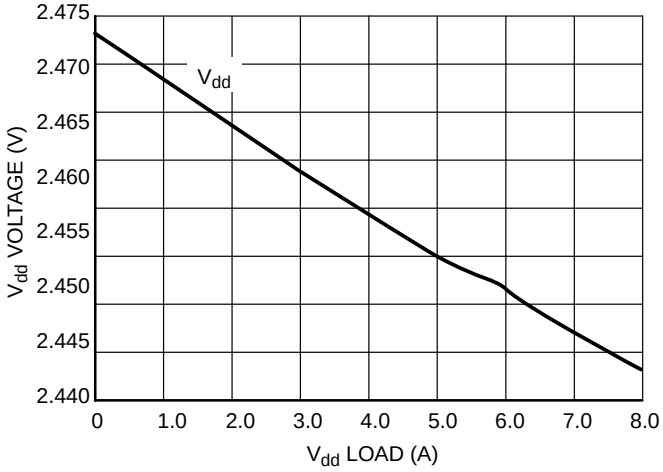


Figure 5. V_{dd} Voltage vs. V_{dd} Load

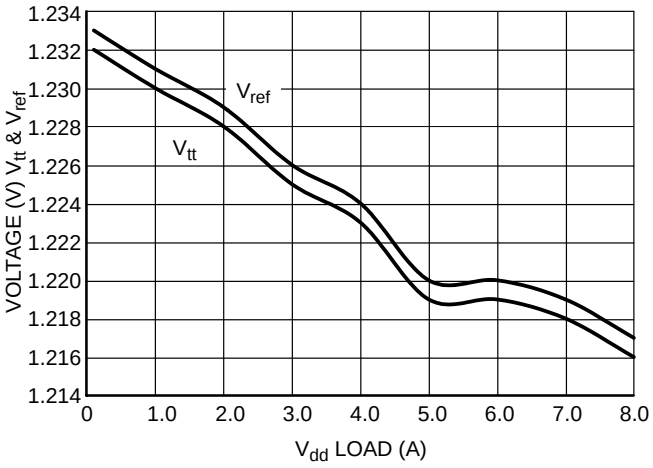


Figure 6. V_{tt} and V_{ref} vs. V_{dd} Load

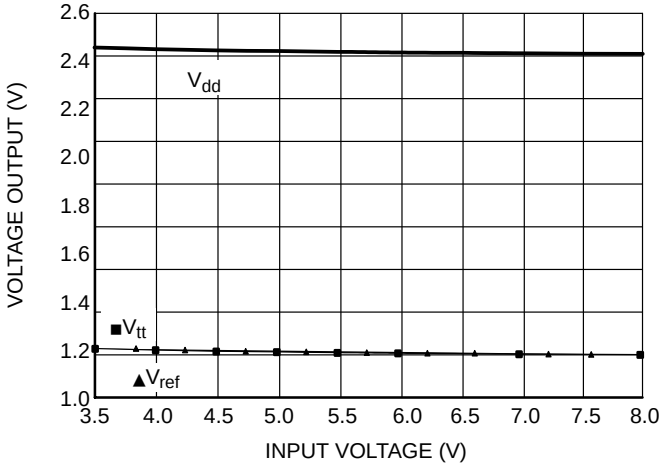


Figure 7. Output Voltage vs. Input Voltage

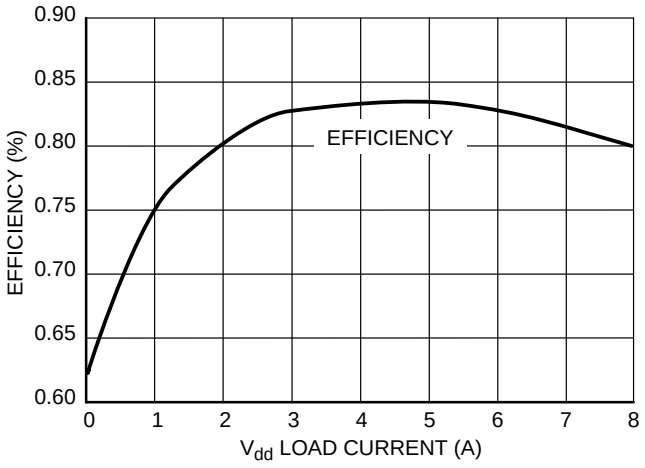


Figure 8. Efficiency vs. V_{dd} Load

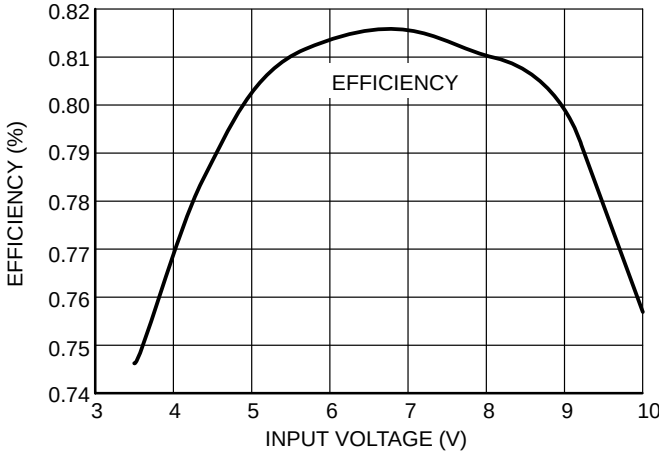
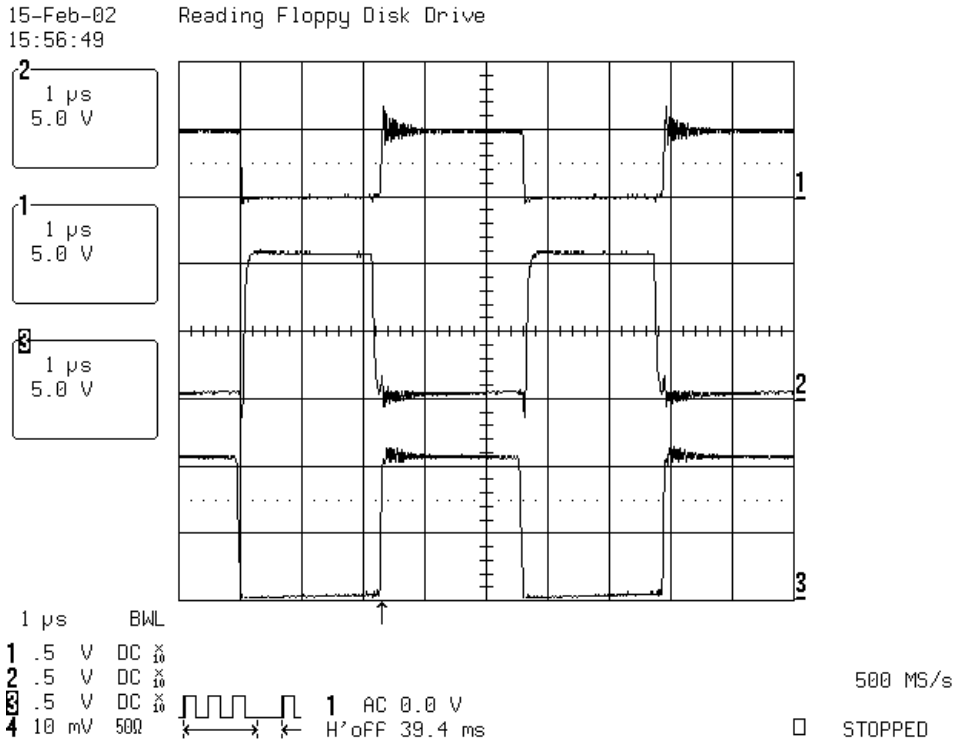
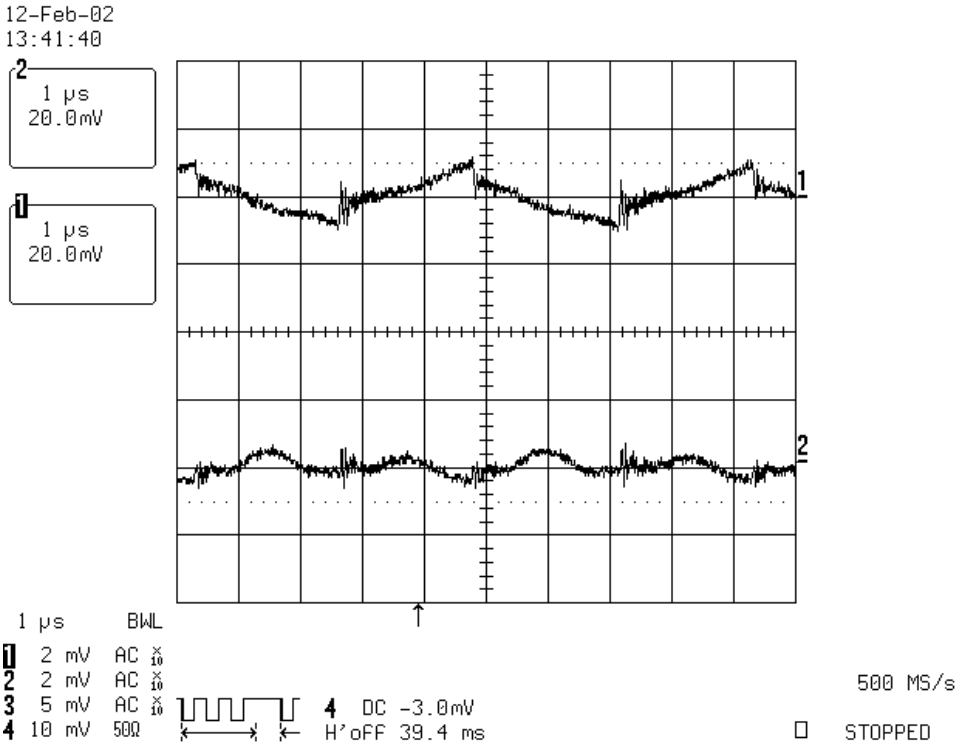


Figure 9. Efficiency vs. Input Voltage



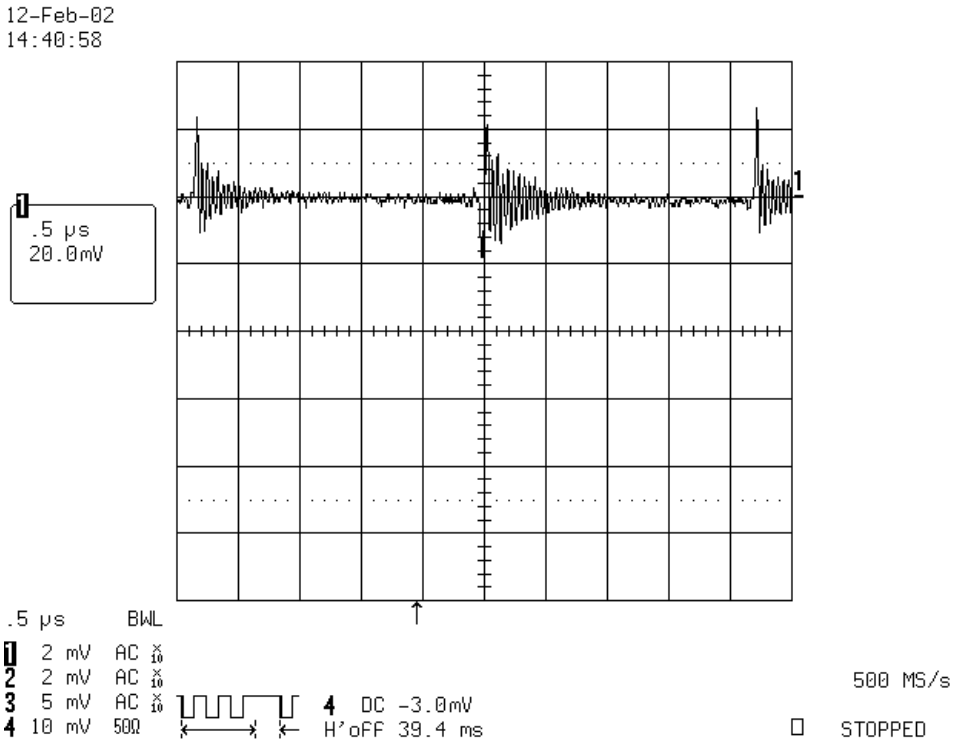
Channel 1: L_2 Inductor Voltage
Channel 2: Bottom (Q_3) Buck MOSFET Gate Drive
Channel 3: Top (Q_2) Buck MOSFET Gate Drive

Figure 10. L_2 Inductor Voltage, Top (Q_2) and Bottom (Q_3) Buck MOSFET Gate Drive



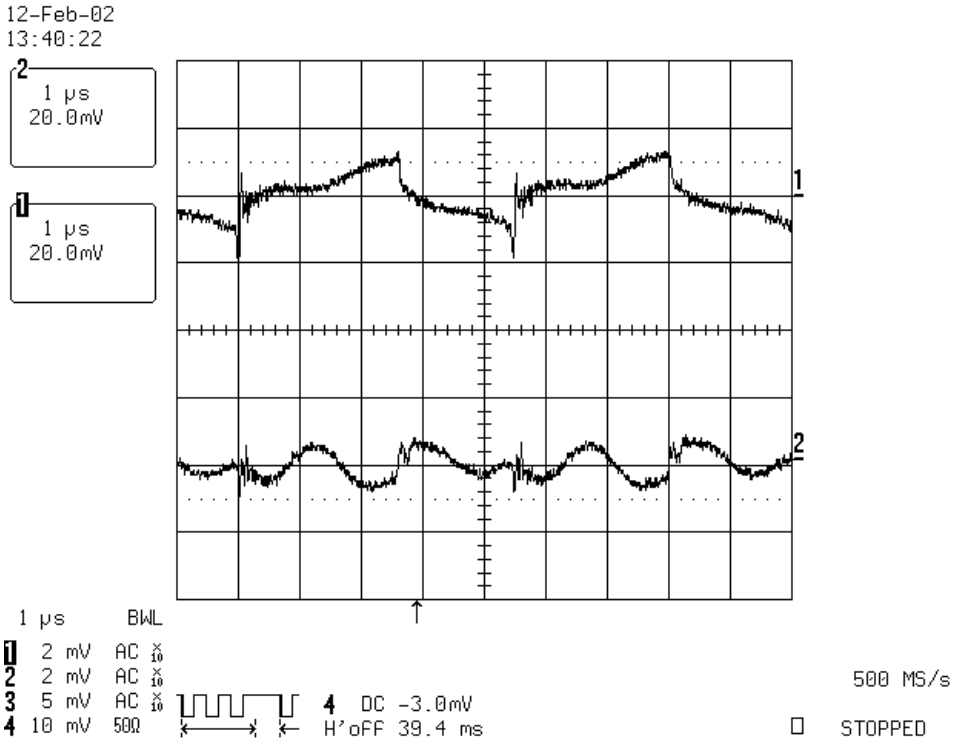
Channel 1: V_{dd} ripple voltage
Channel 2: V_{tt} ripple voltage

Figure 11. Steady-State V_{dd} and V_{tt} with I_{Vdd} = 0.1 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



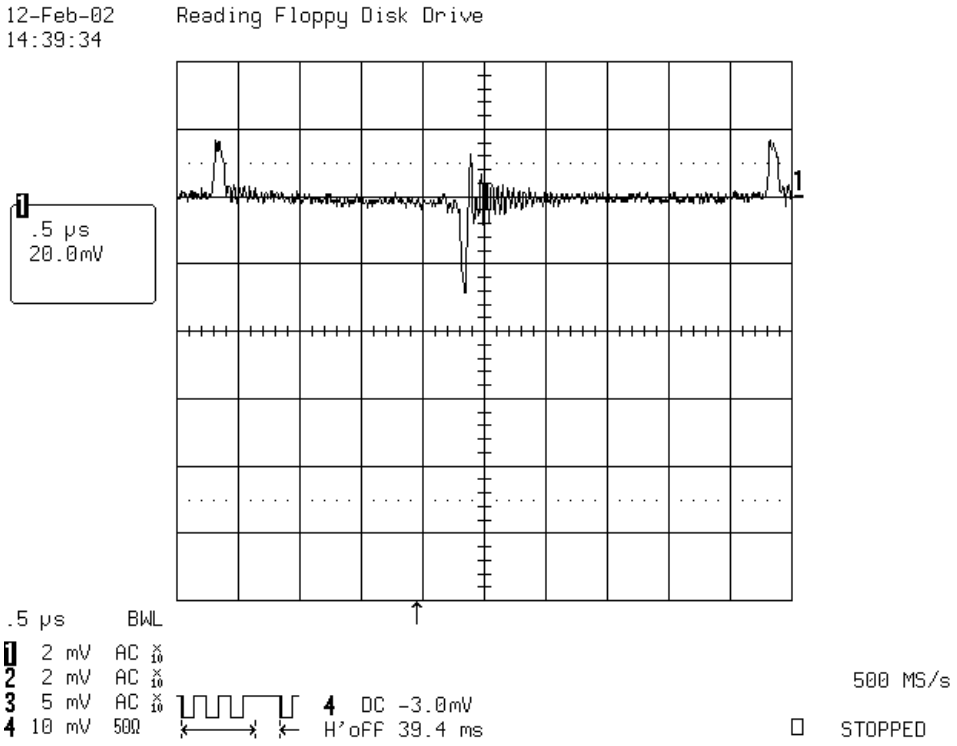
Channel 1: V_{REF} ripple voltage

Figure 12. Steady-State V_{REF} with I_{Vdd} = 0.1 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



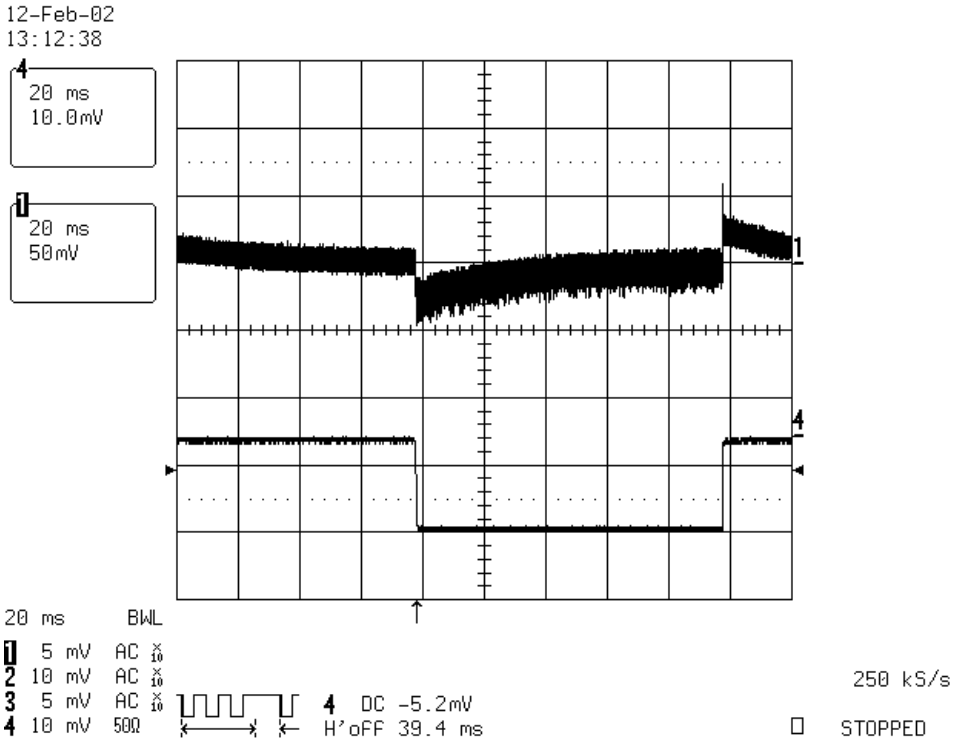
Channel 1: V_{dd} ripple voltage
Channel 2: V_{tt} ripple voltage

Figure 13. Steady-State V_{dd} and V_{tt} with I_{Vdd} = 8.0 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



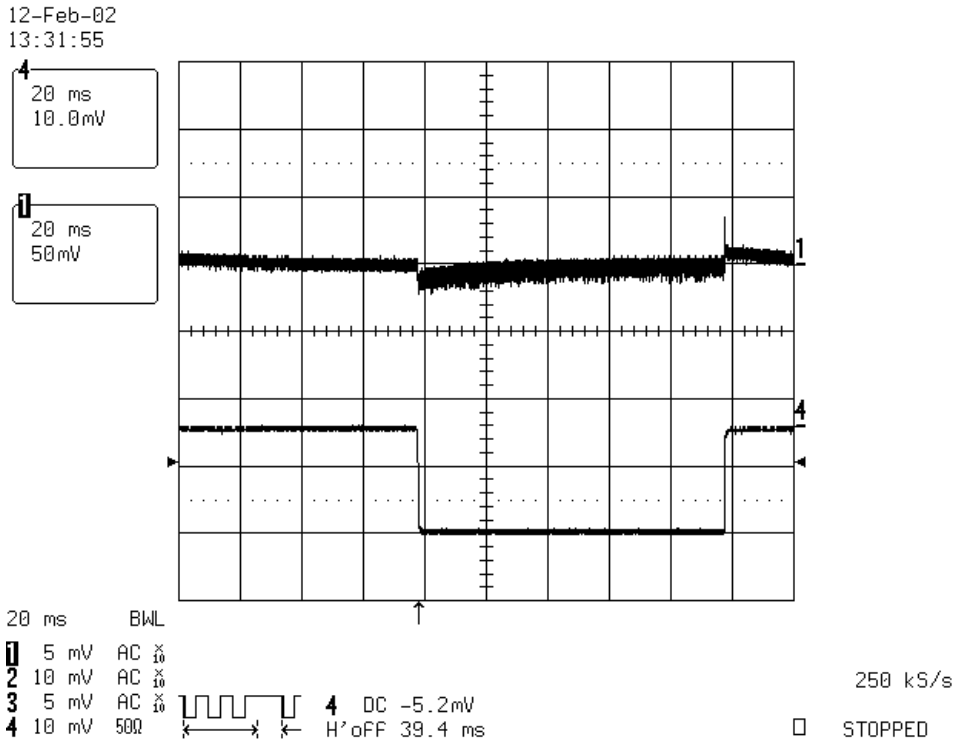
Channel 1: V_{REF} ripple voltage

Figure 14. Steady-State V_{REF} with I_{Vdd} = 8.0 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



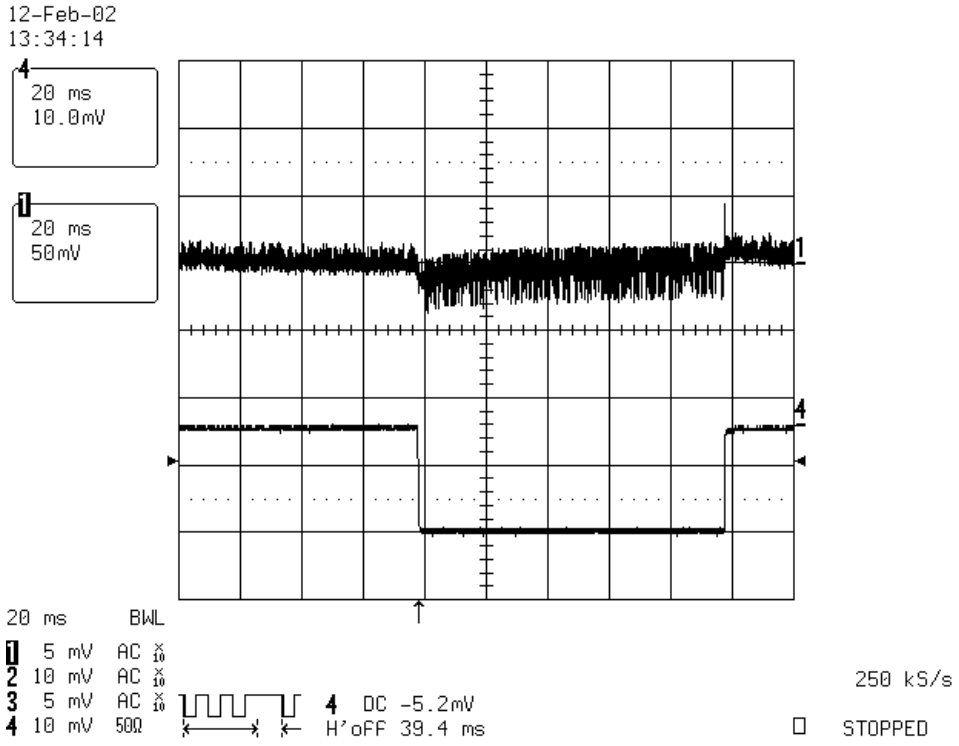
Channel 1: V_{dd} ripple voltage
Channel 2: Transient current load I_{Vdd} = 0 to 8.0 A

Figure 15. V_{dd} with a Transient Load I_{Vdd} = 0 to 8.0 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



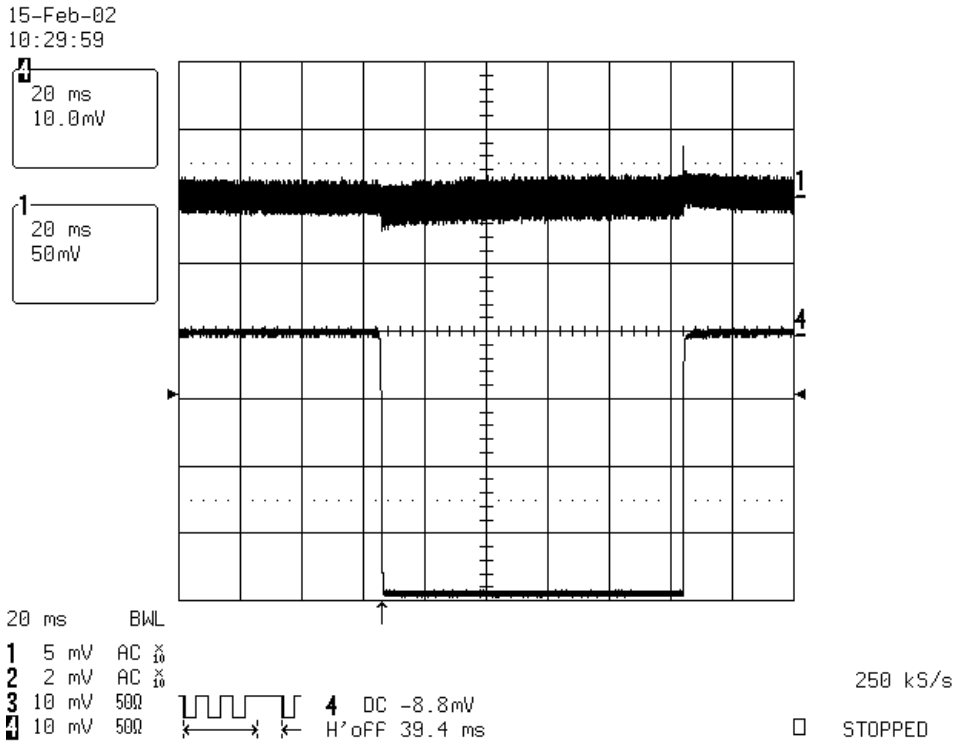
Channel 1: V_{tt} ripple voltage
Channel 2: Transient current load I_{Vdd} = 0 to 8.0 A

Figure 16. V_{tt} with a Transient Load I_{Vdd} = 0 to 8.0 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



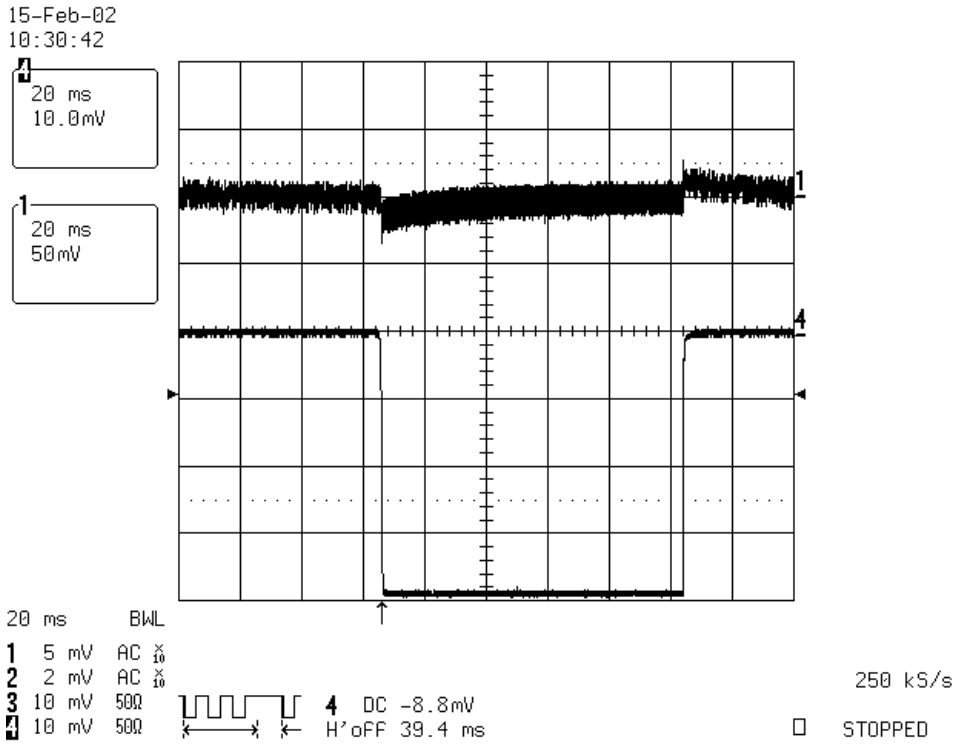
Channel 1: V_{REF} ripple voltage
Channel 2: Transient current load I_{Vdd} = 0 to 8.0 A

Figure 17. V_{REF} with a Transient Load I_{Vdd} = 0 to 8.0 A, I_{Vtt} = 1.25 A Sourcing and V_{REF} = 2.45 mA



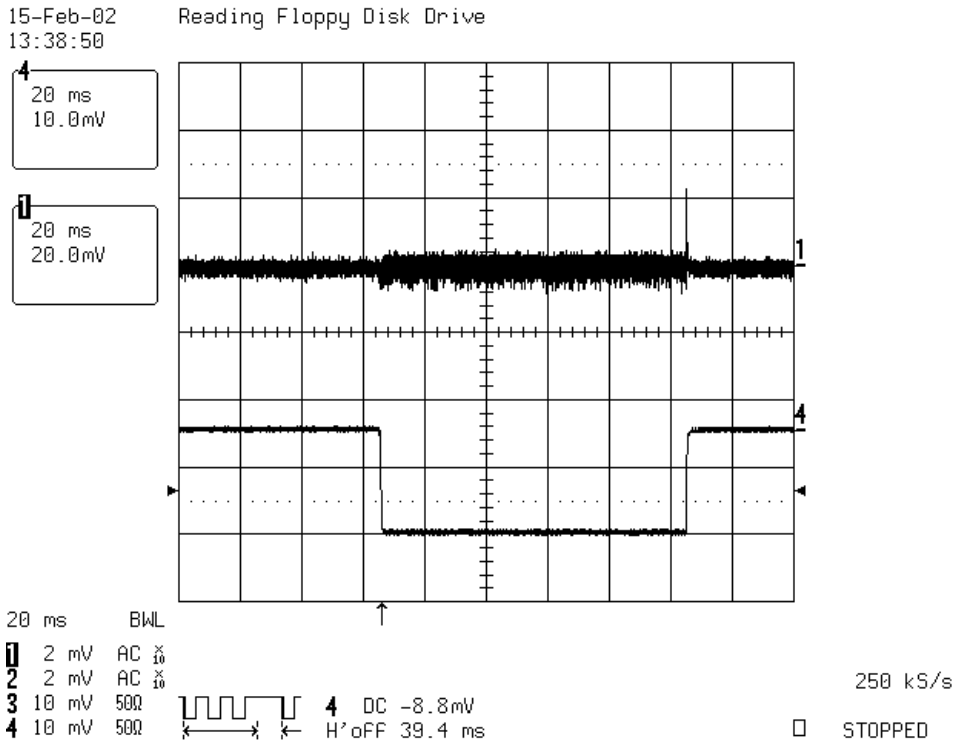
Channel 1: V_{dd} ripple voltage
Channel 2: Transient current load I_{Vtt} = 0 to 4.0 A sourcing
(i.e. –2.0 A sinking to +2.0 A sourcing transient current load)

Figure 18. V_{dd} with a Transient Load I_{Vtt} = -2.0 to +2.0 A, I_{Vdd} = 8.0 A and V_{REF} = 2.45 mA



Channel 1: V_{tt} ripple voltage
Channel 2: Transient current load I_{Vtt} = 0 to 4.0 A sourcing
(i.e. –2.0 A sinking to +2.0 A sourcing transient current load)

Figure 19. V_{tt} with a Transient Load I_{Vtt} = -2.0 to +2.0 A, I_{Vdd} = 8.0 A and V_{REF} = 2.45 mA



Channel 1: 5.0 V Input Voltage
Channel 2: Transient current load of I_{Vdd} = 0 to 8.0 A

Figure 20. Switching Noise Reflected to the 5.0 V Input Power Supply with a Transient Load I_{Vdd} = 0 to 8.0 A, I_{Vtt} = 0 to 4.0 A Sourcing (i.e. –2.0 A Sinking to +2.0 A Sourcing Transient Current Load) and V_{REF} = 2.45 mA

Table 1: Component temperature measured in still air at an ambient temperature of 23°C. The load conditions were:

1. V_{dd} Transient current load I_{Vdd} = 0 to 8.0 A
2. V_{tt} Transient current load I_{Vtt} = 0 to 4.0 A sourcing (i.e. –2.0 A sinking to +2.0 A sourcing transient current load)
3. Steady state V_{REF} current load I_{REF} = 2.5 mA

Table 1.

Circuit	Component	Temperature (°C)
V_{dd}	FET Diode (Q_1)	41.6
V_{dd}	Top FET (Q_2)	54.2
V_{dd}	Bottom FET (Q_3)	56.4
V_{dd}	Input Inductor (L_1)	42.1
V_{dd}	Output Inductor (L_2)	57.9
V_{dd}	Input Capacitor (C_2)	33.0
V_{dd}	Output Capacitor (C_{10})	31.2
V_{dd}	NCP1571 (U_1)	55.0
V_{tt}	LM358 (U_2)	46.2
V_{tt}	Top FET (Q_4)	42.1
V_{tt}	Bottom FET (Q_5)	49.3

DEMONSTRATION DESIGN PCB

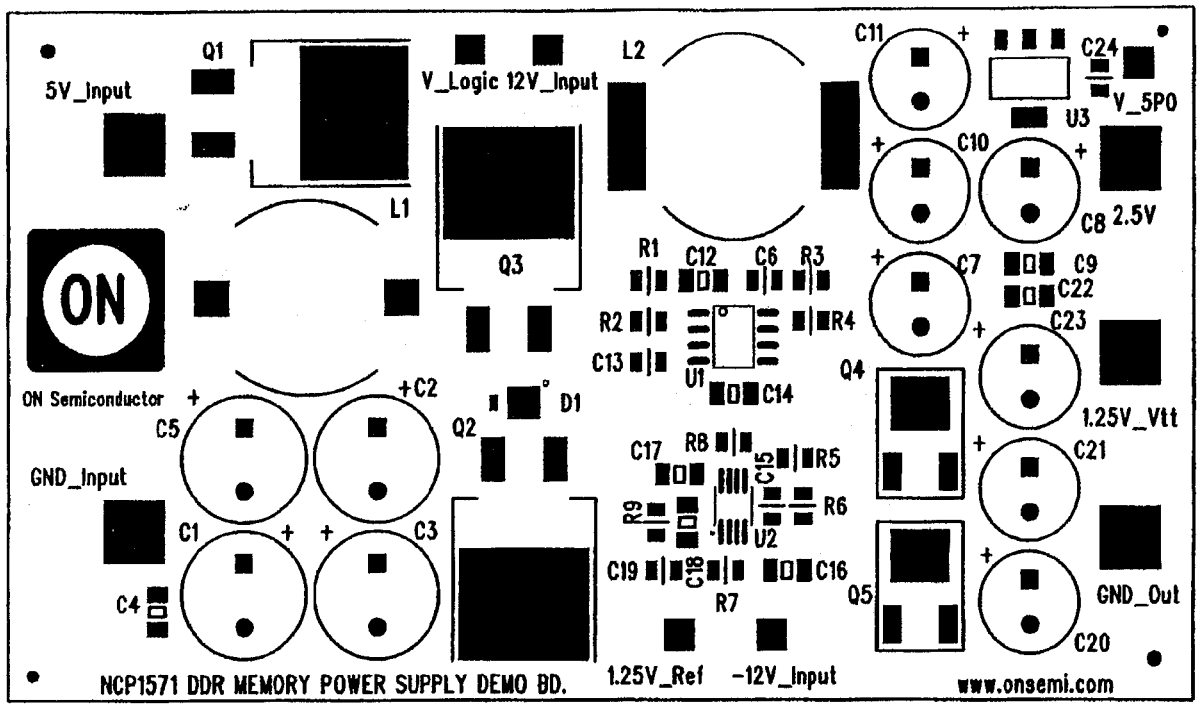


Figure 21. Component Layout

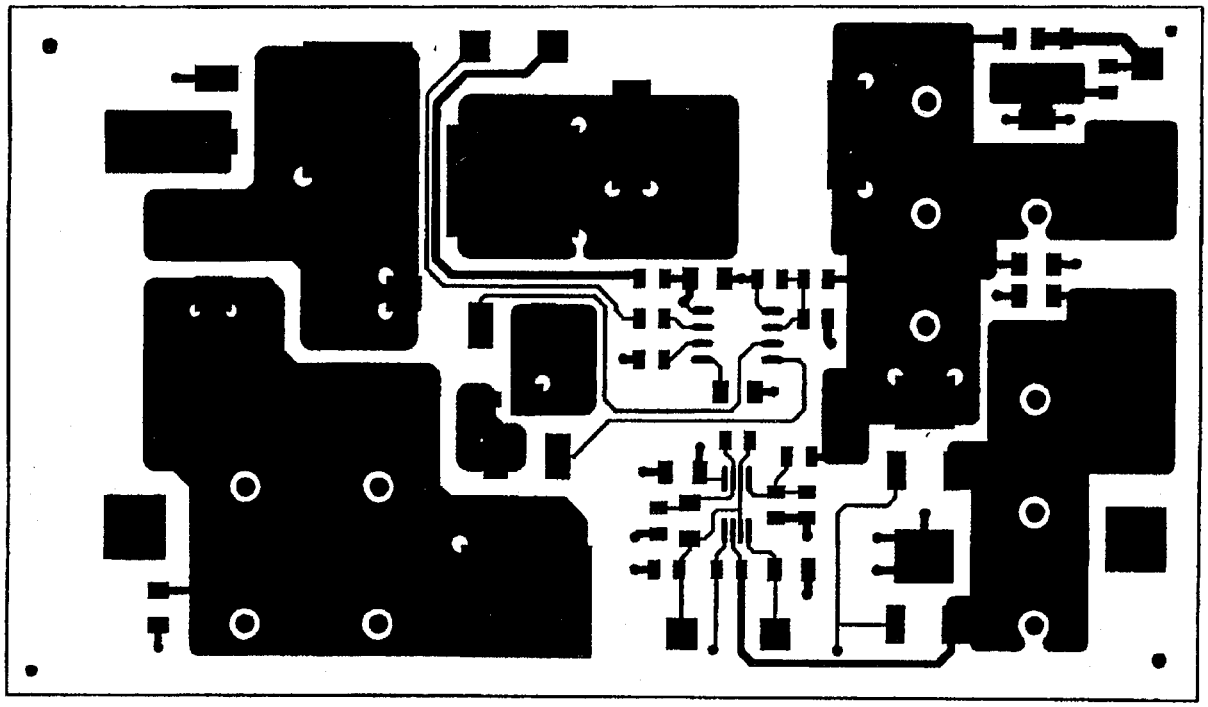


Figure 22. TopSide of PCB (layer 1)

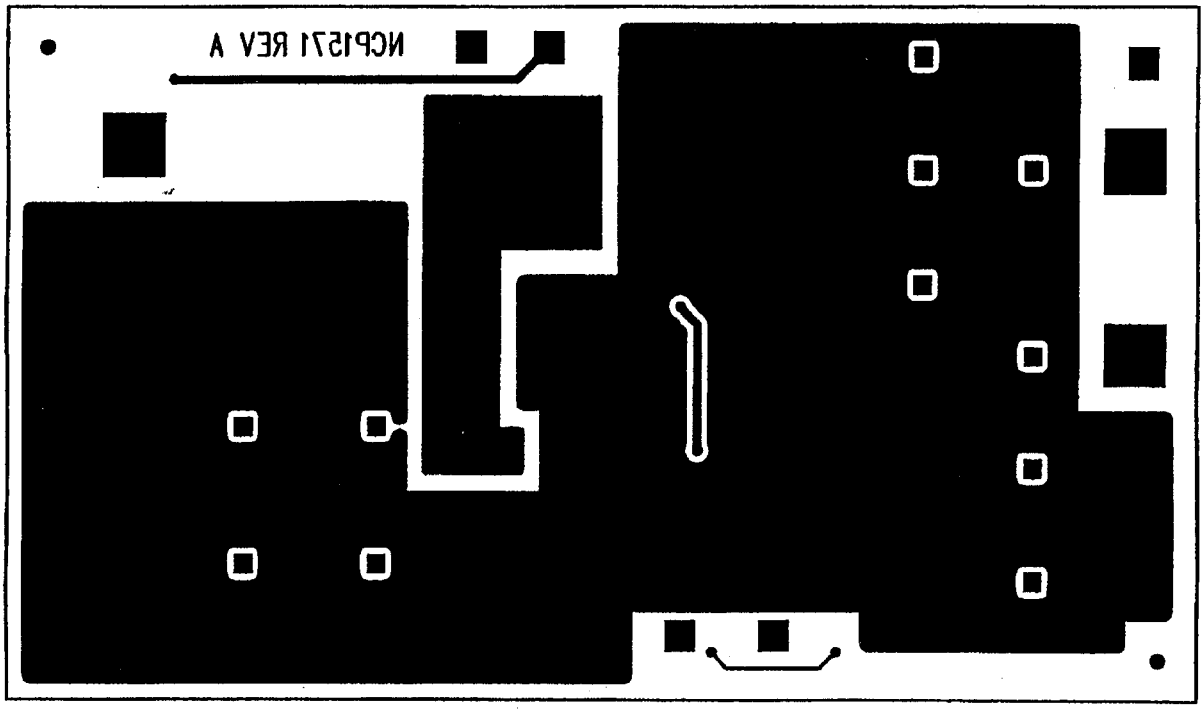


Figure 23. Bottom Side of PCB (layer 2)

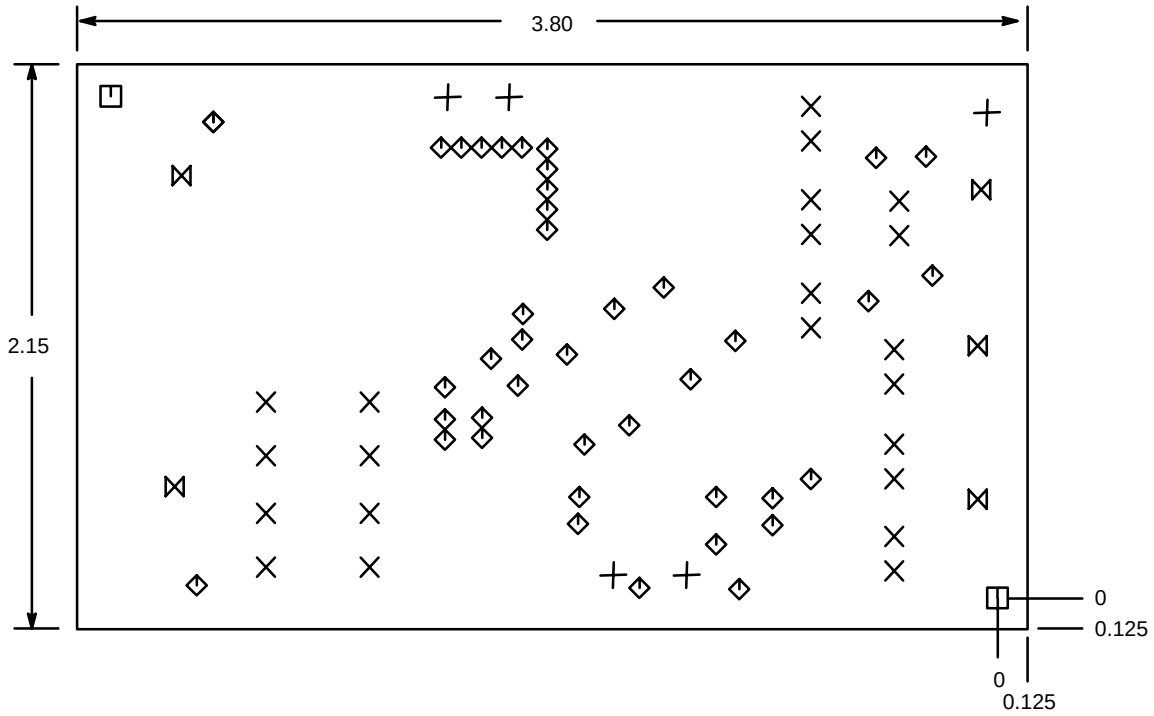


Figure 24. Drill Plot

Size	Qty.	Symbol
62	5	+
38	22	×
62	2	⊓
18	41	◇
125	5	⋈

Table 2. Demonstration Board Bill of Materials

Item	Quantity	Reference	Part	Part No.	Package	Mfg.	Comments
1	4	C1, C2, C3, C5	1800 μF, 10 V	MBZ Series	see data sheet	Rubycon	C5 is provisional
2	7	C7, C8, C10, C11, C20, C21, C23	1800 μF, 6.3 V	MBZ Series	see data sheet	Rubycon	C7, C20 and C21 are provisional
3	7	C4, C9, C12, C14, C16, C17, C22	0.1 μF	-	SMT 1206	-	-
4	1	C6	100 pF	-	SMT O805	-	-
5	1	C18	0.15 μF	-	SMT 1206	-	-
6	1	C13	0.01 μF	-	SMT O805	-	-
7	1	C15	1.0 μF	-	SMT O805	-	-
8	1	C19	2.0 μF	-	SMT O805	-	-
9	1	L1	1.0 μH	DO3316P-102HC	see data sheet	Coilcraft	-
10	1	L2	2.2 μH	DO5022P-222HC	see data sheet	Coilcraft	-
11	3	Q1, Q2, Q3	N-Channel Mosfet	MTB1306	D2PAK	ON Semiconductor	-
12	1	Q4	N-Channel Mosfet	NTD4302	DPAK Bent Lead	ON Semiconductor	-
13	1	Q5	P-Channel Mosfet	MTD20P03HDL	DPAK Bent Lead	ON Semiconductor	-
14	1	R1	10 ohm	-	SMT O805	-	-
15	1	R2	47 Kohm	-	SMT O805	-	-
16	1	R3	20 Kohm	-	SMT O805	-	-
17	1	R4	13 Kohm	-	SMT O805	-	-
18	2	R5, R6	10 Kohm	-	SMT O805	-	-
19	1	R7	1.0 Kohm	-	SMT O805	-	-
20	1	R8	200 ohm	-	SMT O805	-	-
21	1	R9	100 ohm	-	SMT O805	-	-
22	1	U1	Sync. Buck Controller	NCP1571	SO-8	ON Semiconductor	-
23	1	U2	Op-Amp	LM358DMR2	Micro-8	ON Semiconductor	-
24	1	U3	LDO Regulator	MC33375ST-2.5T3	SOT-223	ON Semiconductor	U3 is provisional
25	1	D1	Schottky Diode	MBRM110LT	PowerMite	ON Semiconductor	D1 is provisional

NOTE: The provisional components were not used in the verification of the reference design.

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Notes

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