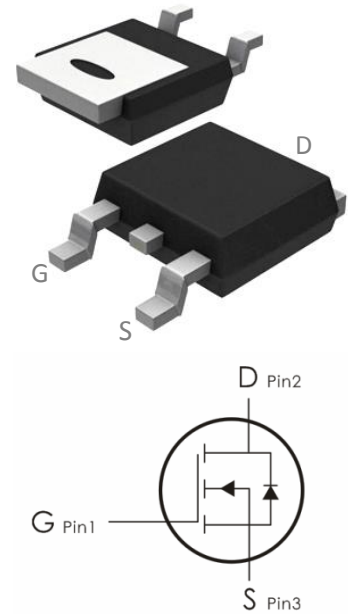


## Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent  $R_{DS(on)}$  with low gate charge. It can be used in a wide variety of applications.

## Features:

- 1)  $V_{DS}=30V, I_D=55A, R_{DS(on)} < 10m\ \Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low  $R_{DS(on)}$ .
- 5) Excellent package for good heat dissipation.



## Absolute Maximum Ratings: ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current- $T_C=25^\circ C^1$	55	A
	Continuous Drain Current- $T_C=100^\circ C$	30	
	Pulsed Drain Current <sup>2</sup>	112	
$E_{AS}$	Single Pulse Avalanche Energy <sup>3</sup>	24.2	mJ
$I_{AS}$	Avalanche Current	22	A
$P_D$	Power Dissipation, $T_C=25^\circ C^4$	37.5	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ C$

## Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case <sup>1</sup>	4	$^\circ C/W$

$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	°C/W
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## Electrical Characteristics: ( $T_C=25^\circ\text{C}$ unless otherwise noted)

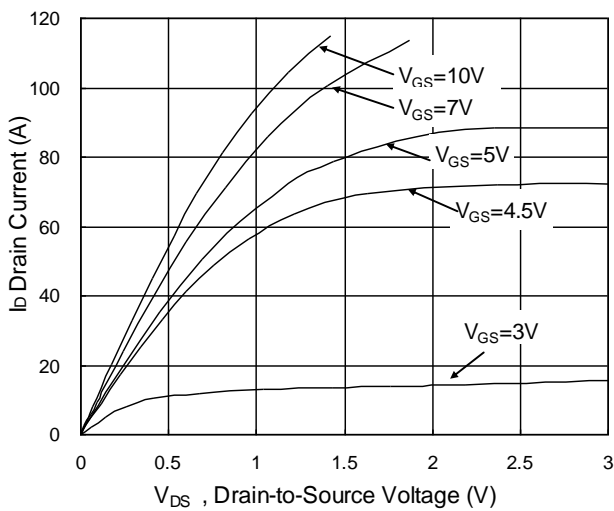
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu\text{A}$	30	---	---	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS}=0V, V_{DS}=30V$	---	---	1	$\mu\text{A}$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0A$	---	---	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	GATE-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\ \mu\text{A}$	1.2	---	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance <sup>2</sup>	$V_{GS}=10V, I_D=30A$	---	7.5	10	m $\Omega$
		$V_{GS}=4.5V, I_D=15A$	---	11	18	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	940	---	pF
$C_{oss}$	Output Capacitance		---	131	---	
$C_{riss}$	Reverse Transfer Capacitance		---	109	---	
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, I_D=15A,$ $V_{GS}=10V, R_{GEN}=3.3\Omega$	---	4	---	ns
$t_r$	Rise Time		---	8	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	31	---	ns
$t_f$	Fall Time		---	4	---	ns
$Q_g$	Total Gate Charge	$V_{GS}=4.5V, V_{DS}=15V,$ $I_D=15A$	---	9.8	---	nC
$Q_{gs}$	Gate-Source Charge		---	4.2	---	nC
$Q_{gd}$	Gate-Drain "Miller" Charge		---	3.6	---	nC
<b>Drain-Source Diode Characteristics</b>						

<b>V<sub>SD</sub></b>	Source-Drain Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A	---	---	1	V
<b>I<sub>S</sub></b>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	43	A
<b>I<sub>SM</sub></b>	Pulsed Source Current <sup>2,5</sup>		---	--	112	Ns
<b>T<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =30A, di/dt=100A/μs, T <sub>J</sub> =25°C	---	8.5	---	
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge		---	2.2	---	

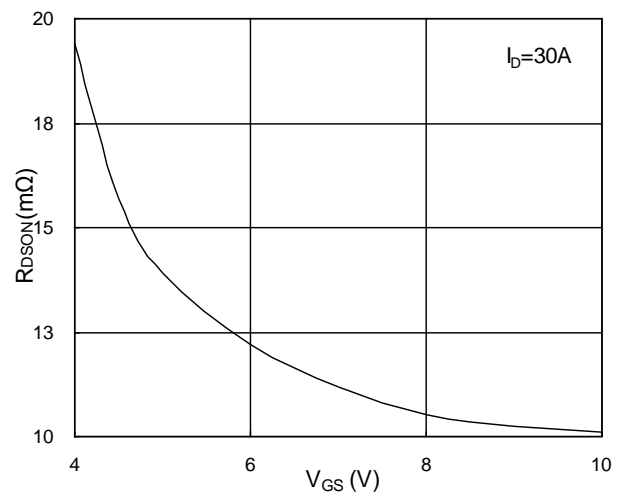
### Notes:

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=22A
- 4.The power dissipation is limited by 175°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

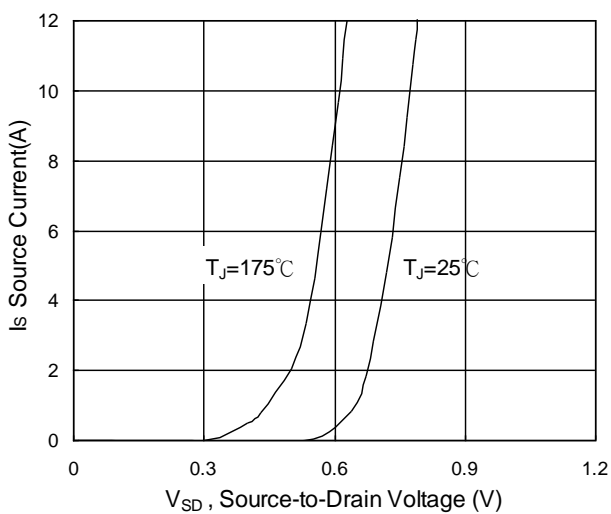
### Typical Characteristics: (T<sub>C</sub>=25°C unless otherwise noted)



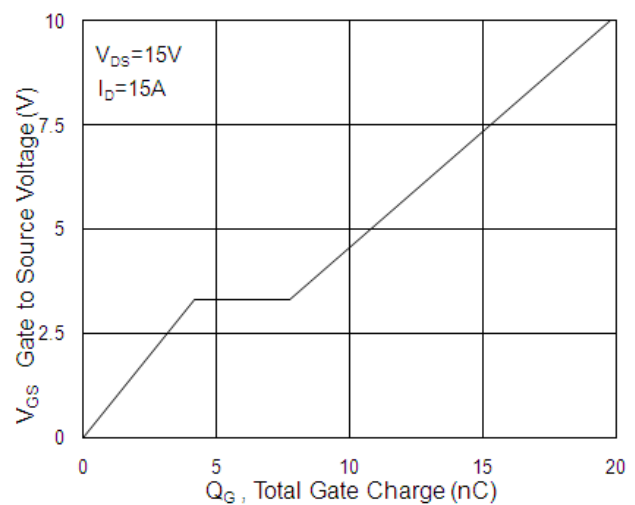
**Fig.1 Typical Output Characteristics**



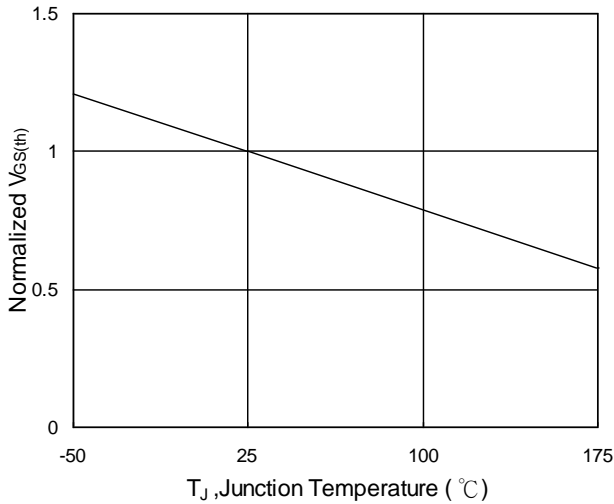
**Fig.2 On-Resistance vs. G-S Voltage**



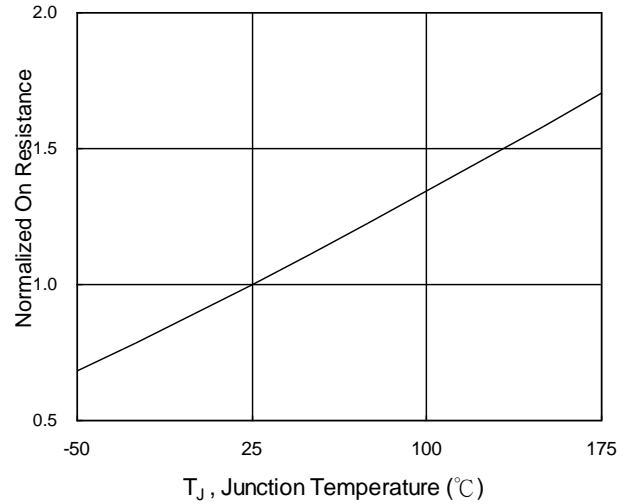
**Fig.3 Forward Characteristics of Reverse**



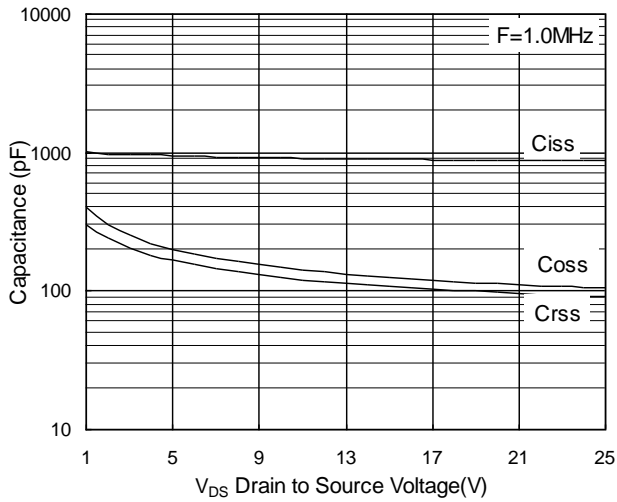
**Fig.4 Gate-Charge Characteristics**



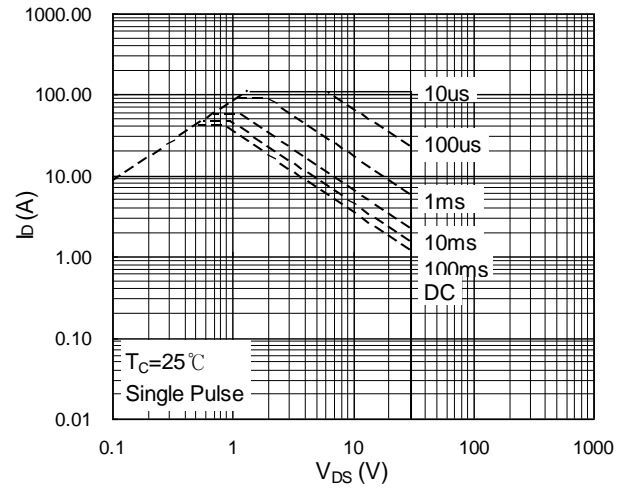
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



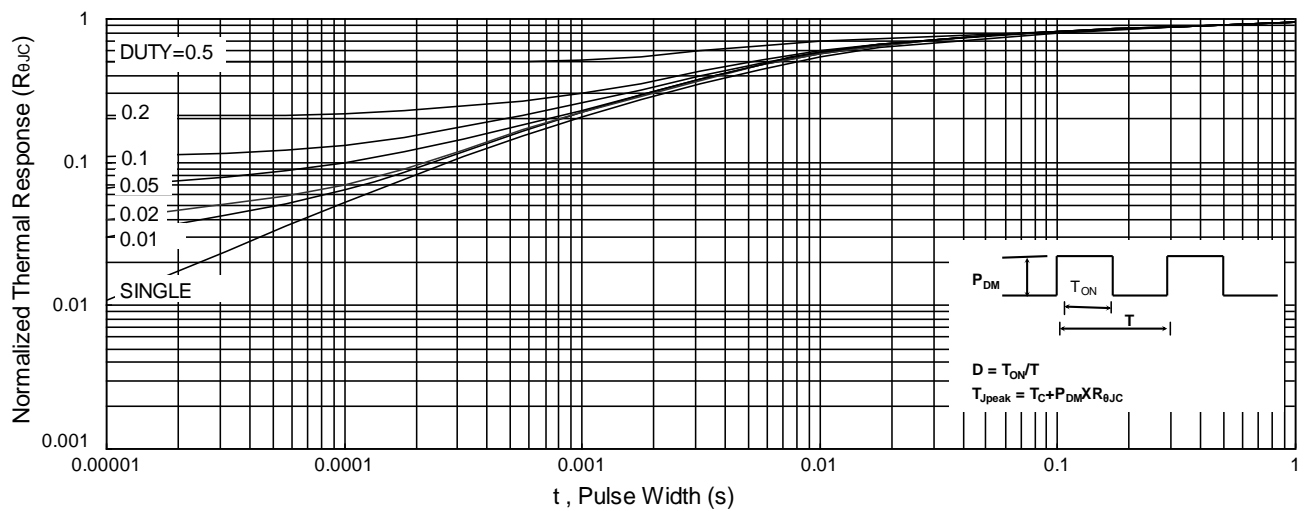
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



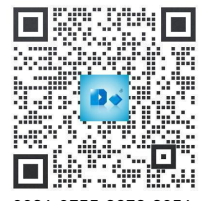
**Fig.7 Capacitance**



**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



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