AP393

Low Power Low Offset Voltage Dual Comparators

■ Features

- Wide supply
  Voltage range: 2.0V to 36V
  Single or dual supplies: ±1.0V to ±18V
- Very low supply current drain (0.4 mA) –
  independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Maximum offset voltage: ±3 mV
- Input common-mode voltage range includes
  ground
- Differential input voltage range equal to the power
  supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL,
  MOS and CMOS logic systems
- 8-pin PDIP and SOP **Pb-Free** packages

■ Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation
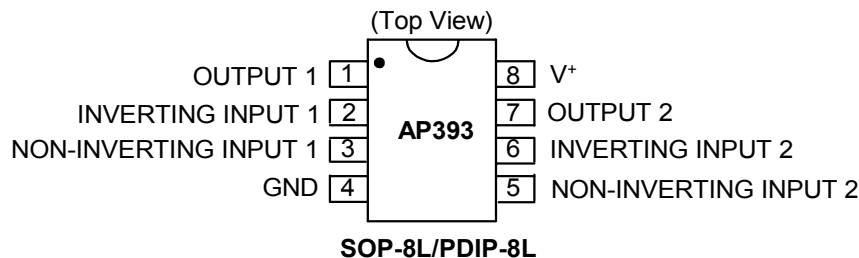
■ General Description

The AP393 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The AP393 is designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AP393 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.
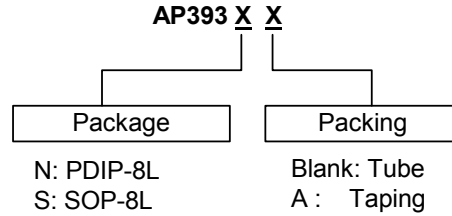
■ Pin Assignment

(Top View)

OUTPUT 1	1	8	V⁺
INVERTING INPUT 1	2	7	OUTPUT 2
NON-INVERTING INPUT 1	3	6	INVERTING INPUT 2
GND	4	5	NON-INVERTING INPUT 2

AP393

SOP-8L/PDIP-8L

■ Pin Descriptions

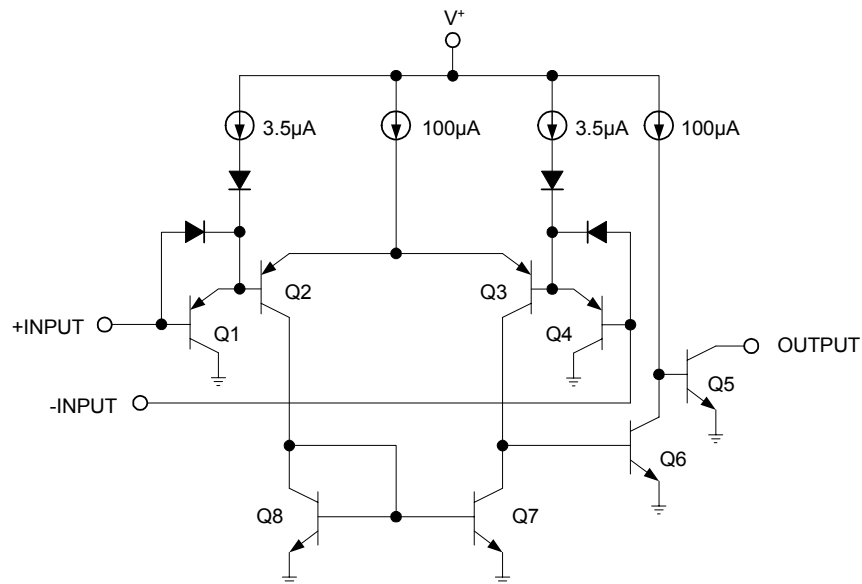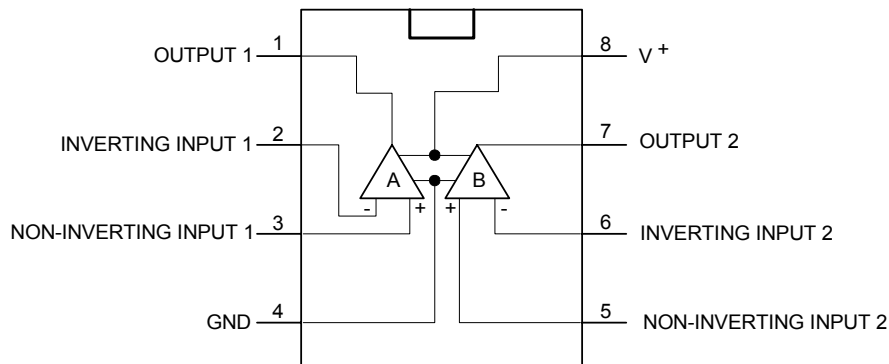| Pin Name	Pin No.	Description
OUTPUT 1	1	Channel 1 Output
INVERTING INPUT 1	2	Channel 1 Negative Input
NON-INVERTING INPUT 1	3	Channel 1 Positive Input
GND	4	Ground

Pin Name	Pin No.	Description
NON-INVERTING INPUT 2	5	Channel 2 Positive Input
INVERTING INPUT 2	6	Channel 2 Negative Input
OUTPUT 2	7	Channel 2 Output
V⁺	8	Vcc

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■ **Ordering Information**

AP393 X X

Package	Packing
N: PDIP-8L S: SOP-8L	Blank: Tube A : Taping

■ **Block Diagram**

OUTPUT 1 — 1

INVERTING INPUT 1 — 2

NON-INVERTING INPUT 1 — 3

GND — 4

8 — V $^+$

7 — OUTPUT 2

6 — INVERTING INPUT 2

5 — NON-INVERTING INPUT 2

A

B

V $^+$

3.5μA   100μA   3.5μA   100μA

+INPUT

-INPUT

Q1   Q2   Q3   Q4

Q5   OUTPUT

Q6

Q8   Q7

Rev. 1.0   Sep 7, 2004

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■ **Absolute Maximum Ratings** (Note 10)

Symbol	Parameter		Rating	Unit
V_{CC}	Supply Voltage		36	V
V_{IN}	Differential Input Voltage (Note 8)		36	V
V_{IN}	Input Voltage		-0.3 to +36	V
I_{CC}	Input Current (V_{IN}-0.3V) (Note 3)		50	mA
P_D	Power Dissipation (Note 1)	Molded DIP	780	mW
		Metal Can	660	
		Small Outline Package	510	
	Output Short-Circuit to Ground (Note 2)		Continuous	
T_{OP}	Operating Temperature Range		0 to +70	^{o}C
T_{ST}	Storage Temperature Range		-65 to +150	^{o}C
T_{Lead}	Lead Temperature Range (Soldering, 10 sec)		+260	^{o}C
	Soldering Information	PDIP Soldering (10 sec)	+260	^{o}C
		SOP Vapor Phase (60 sec)	+215	
		Infrared (15 sec)	+220	
	ESD rating (1.5kΩ in with 100pF)		1300	V

■ **Electrical Characteristics** (V_{CC}=5V, T_A=25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage	(Note 9)	-	1.0	5.0	mV
I_{BIAS}	Input Bias Current	I_{IN}(+) or I_{IN}(-) with Output In Linear Range, V_{CM}=0V (Note 5)	-	25	250	nA
I_{OFFSET}	Input Offset Current	I_{IN}(+) - I_{IN}(-) V_{CM}=0V	-	5.0	50	nA
	Input Common Mode Voltage Range	V^+=30V (Note 6)	0	-	V^+-1.5	V
I_{CC}	Supply Current	R_L=∞ V^+=5V	-	0.4	1	mA
		R_L=∞ V^+=36V	-	1	2.5	
	Voltage Gain	$R_L \geq$ 15kΩ, V^+=15V V_O=1V to 11V	50	200	-	V/mV
	Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V, V_{RL}=5V, R_L=5.1kΩ	-	300	-	ns
	Response Time	V_{RL}=5V, R_L=5.1kΩ (Note 7)	-	1.3	-	µs
$I_{O(Sink)}$	Output Sink Current	V_{IN}(-)=1V, V_{IN}(+)=0, $V_O \leq$1.5V	6.0	16	-	mA
V_{SAT}	Saturation Voltage	V_{IN}(-)=1V, V_{IN}(+)=0, $I_{SINK} \leq$ 4mA	-	250	400	mV
$I_{O(Leak)}$	Output Leakage Current	V_{IN}(-)=0, V_{IN}(+)=1V, V_O=5V	-	0.1	-	nA

■ **Electrical Characteristics** (V_{CC}=5V) (Note 4)

| Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage	(Note 9)	-	-	9	mV
I_{OFFSET}	Input Offset Current	I_{IN}(+) -I_{IN}(-), V_{CM}=0V	-	-	150	nA
I_{BIAS}	Input Bias Current	I_{IN}(+) or I_{IN}(-) with Output In Linear Range, V_{CM}=0V (Note 5)	-	-	400	nA
	Input Common Mode Voltage Range	V^+=30V (Note 6)	0	-	V^+-2.0	V
V_{SAT}	Saturation Voltage	V_{IN}(-)=1V, V_{IN}(+)=0, $I_{SINK} \leq$ 4mA	-	-	700	mV
$I_{O(Leak)}$	Output Leakage Current	V_{IN}(-)=0, V_{IN}(+)=1V, V_O=30V	-	-	1.0	µA
	Differential Input Voltage	Keep All V_{IN}'s $\geq$ 0V (or V^-, if Used), (Note 8)	-	-	36	V

Low Power Low Offset Voltage Dual Comparators

Note 1: For operating at high temperatures, the AP393 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The AP393 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \le 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than -0.3V.

Note 4: The AP393 temperature specifications are limited to $0°C \le T_A \le +70°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+-1.5V at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \simeq 1.4V$, $R_S=0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+-1.5V), at 25°C.

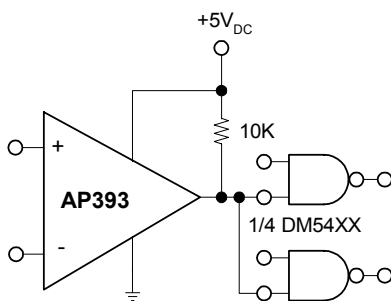**Note 10:** Refer to RETS193AX for AP393 military specifications.
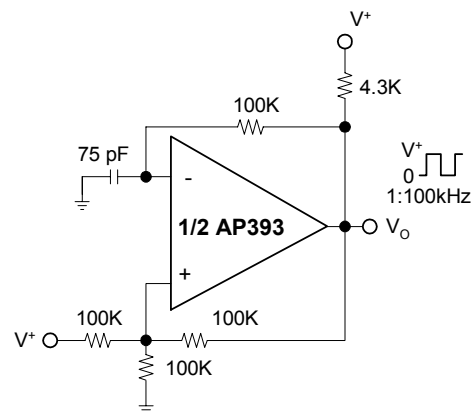
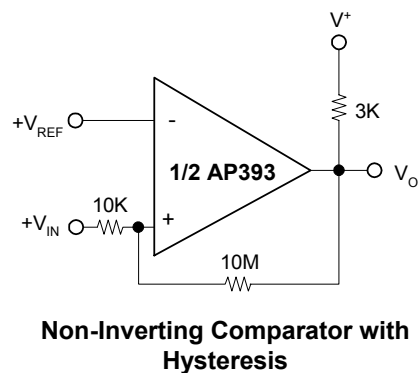## ■ Typical Circuit ($V_{CC} = 5.0V_{DC}$)
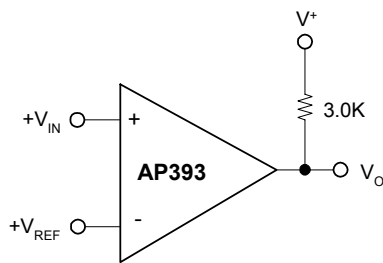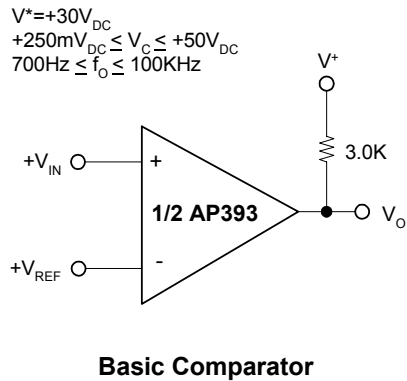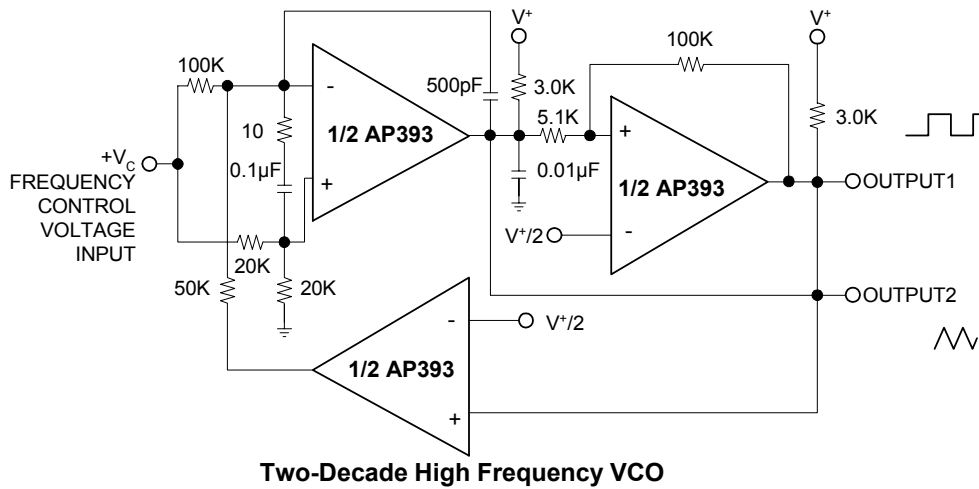

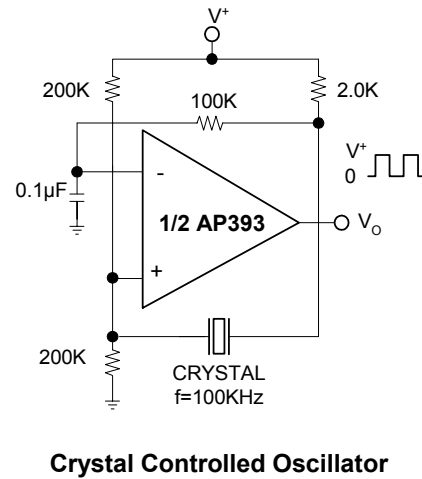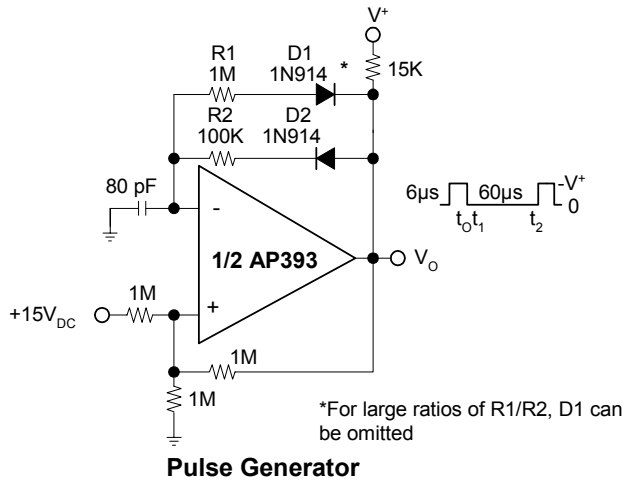**Basic Comparator**
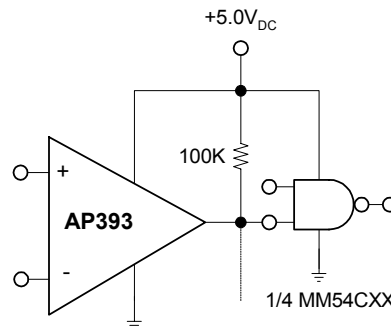
Driving CMOS

Driving TTL

Squarewave Oscillator

Low Power Low Offset Voltage Dual Comparators
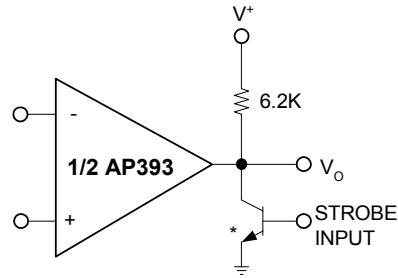
■ **Typical Circuit (Continued)** ($V_{CC} = 5.0V_{DC}$)

Pulse Generator

*For large ratios of R1/R2, D1 can be omitted

Crystal Controlled Oscillator

Two-Decade High Frequency VCO

$V^* = +30V_{DC}$
$+250mV_{DC} \leq V_C \leq +50V_{DC}$
$700Hz \leq f_O \leq 100KHz$

Basic Comparator

Non-Inverting Comparator with Hysteresis

Low Power Low Offset Voltage Dual Comparators

■ Typical Circuit (Continued) (V_{CC} =5.0V_{DC})
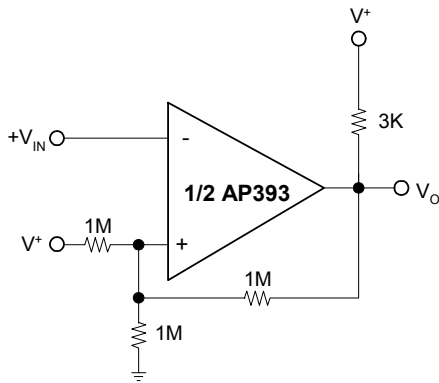
Inverting Comparator with Hysteresis

Output Strobing

* OR LOGIC GATE WITHOUT PULL-UP RESISTOR
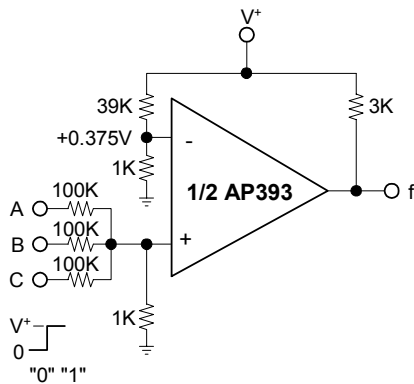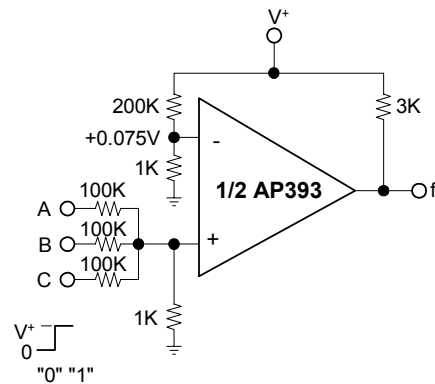
AND Gate

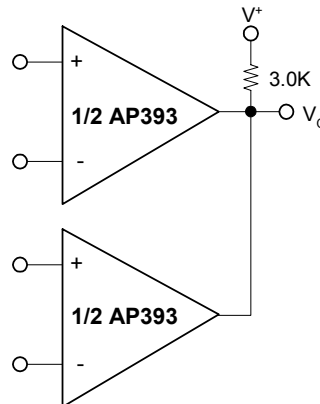**Or Gate**
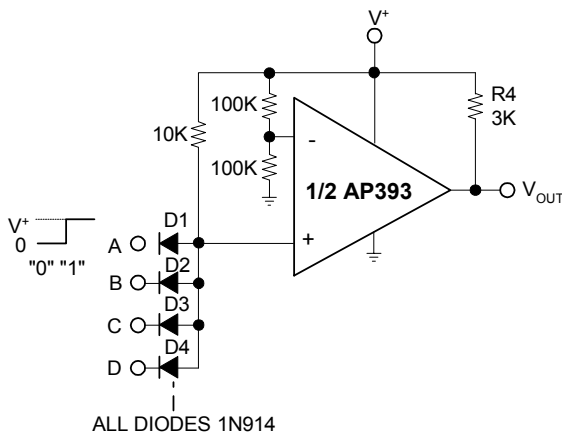
Large Fan-in AND Gate

ALL DIODES 1N914
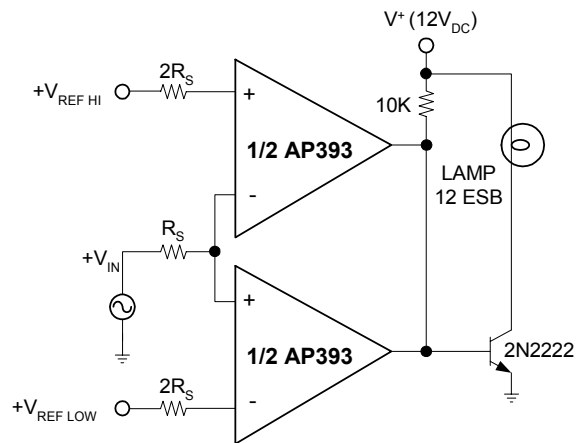
Limit Comparator

Low Power Low Offset Voltage Dual Comparators

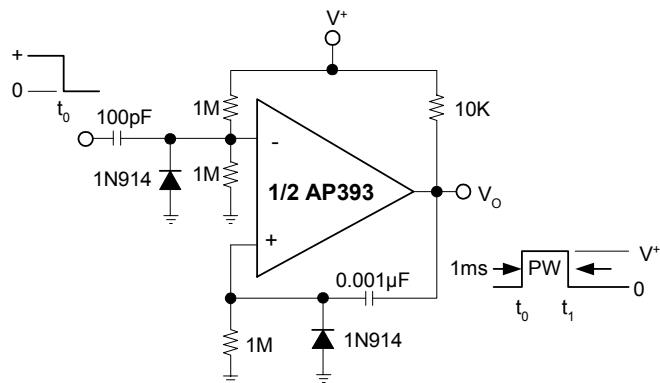## ■ Typical Circuit (Continued) (V_{CC} = 5.0V_{DC})
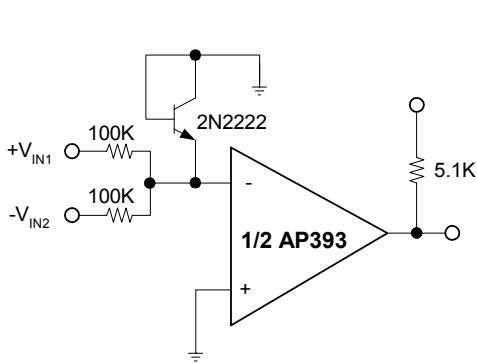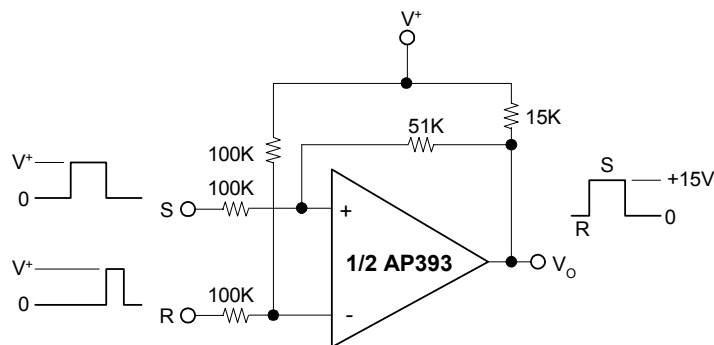
**Comparing Input Voltages of
Opposite Polarity**

ORing the Outputs
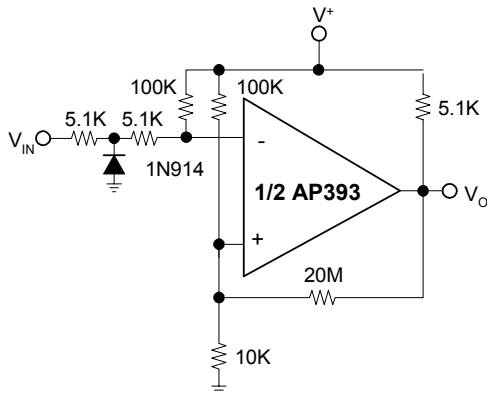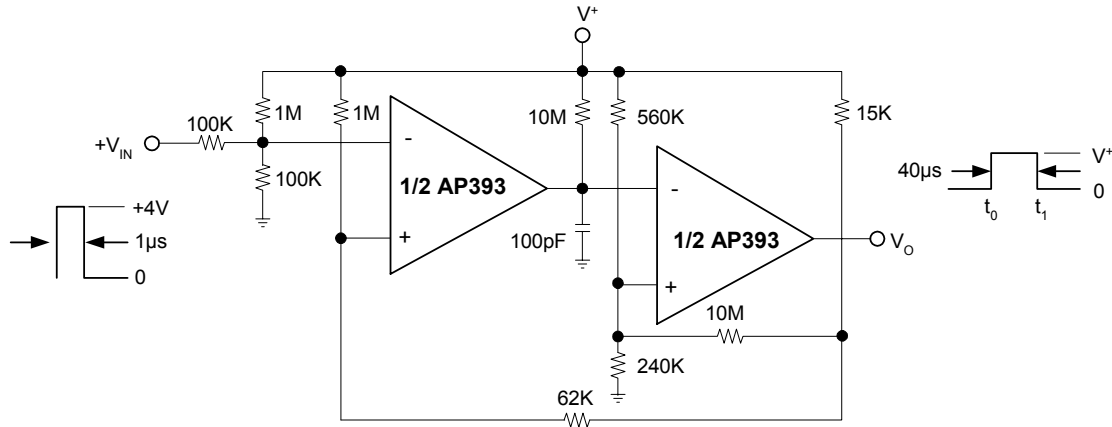
**Zero Crossing Detector
(Single Power Supply)**

One-Shot Multivibrator

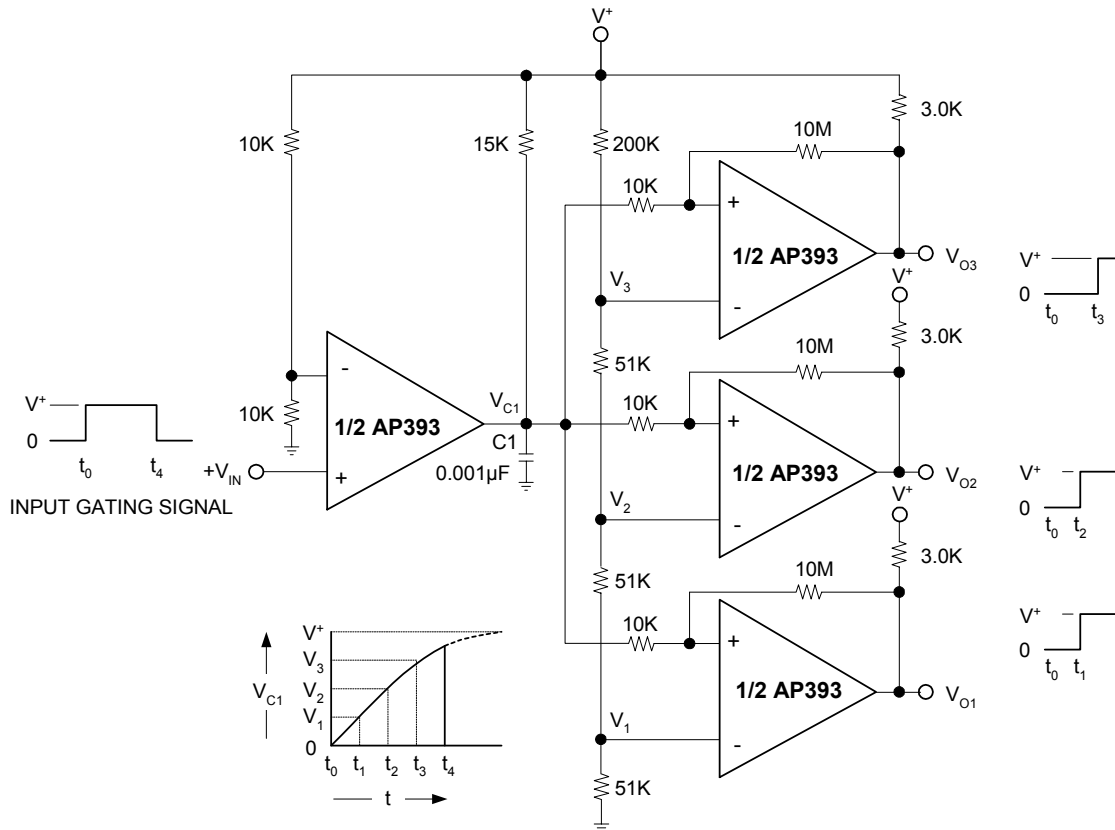**Bi-Stable Multivibrator**

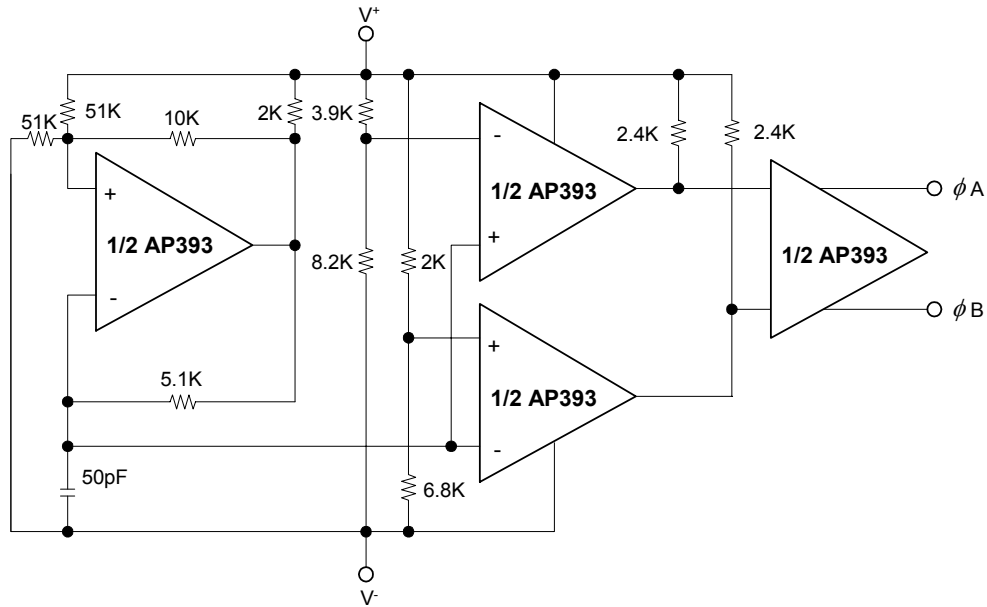■ **Typical Circuit (Continued)** ($V_{CC} = 5.0V_{DC}$)

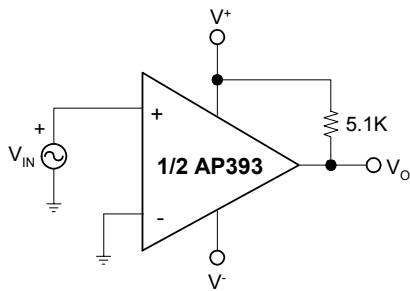**One-Shot Multivibrator with Input Lock Out**

Time Delay Generator

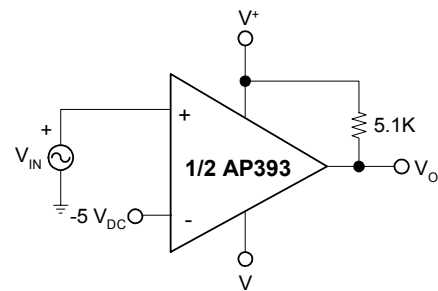**Low Power Low Offset Voltage Dual Comparators**

■ **Split-Supply Applications** (V⁺=+15V$_{DC}$ and V⁻ =-15 V$_{DC}$)

MOS Clock Driver

Zero Crossing Detector

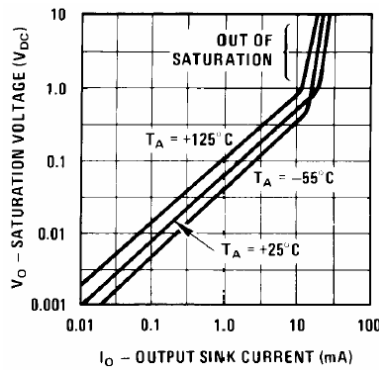**Comparator With a
Negative Reference**

■ Typical Characteristics
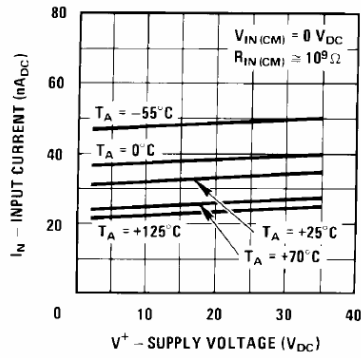
Supply Current
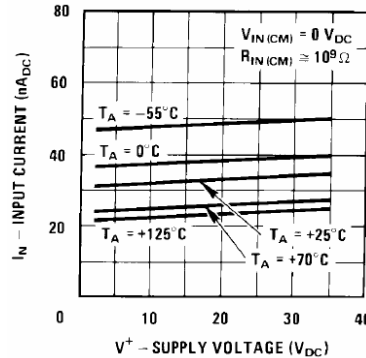
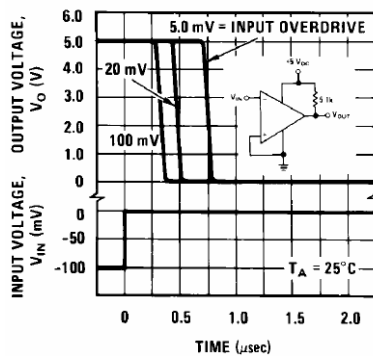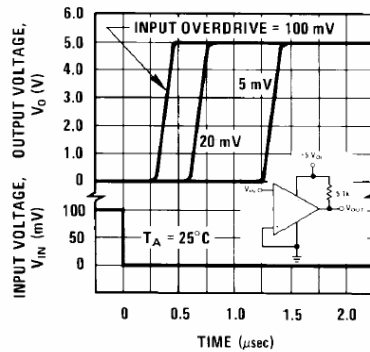**Input Current**

Output Saturation Voltage

Response Time for Various Input Overdrives—Negative Transition

Response Time for Various Input Overdrives—Positive Transition

■ Application Information

The AP393 is high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required. All input pins of any unused comparators should be tied to the negative supply.

The bias network of the AP393 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}. It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device (Note 8). Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the AP393 is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the AP393 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.
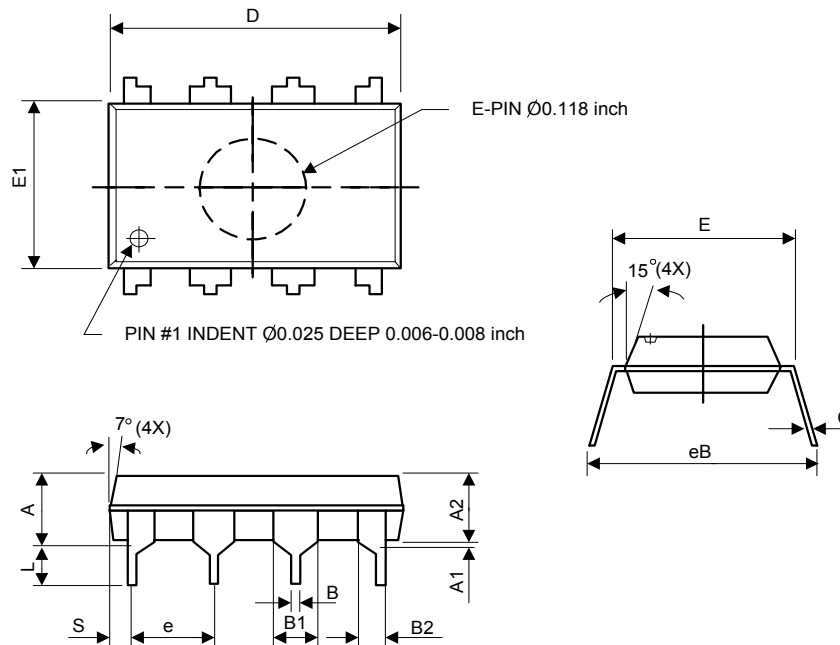
■ Marking Information

SOP-8L/PDIP-8L
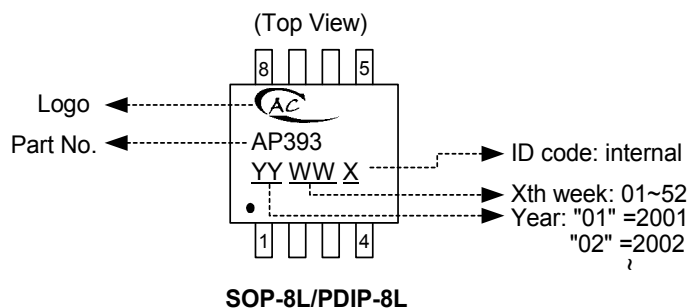
Low Power Low Offset Voltage Dual Comparators

■ Package Information

(1) PDIP-8L (Plastic Dual-in-line Package)

E-PIN Ø0.118 inch

PIN #1 INDENT Ø0.025 DEEP 0.006-0.008 inch

15°(4X)

7° (4X)

Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

■ Package Information (Continued)

(2) SOP- 8L(JEDEC Small Outline Package)

VIEW "A"

VIEW "A"

0.015x45°

7°(4X)

7°(4X)
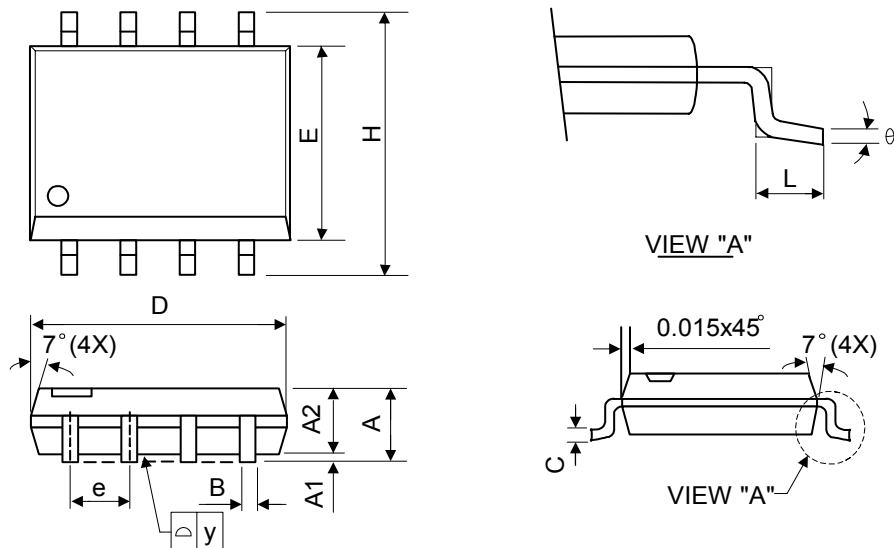
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°